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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	A/D 32x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f38a-gqr

Table 5.3. Port I/O DC Electrical Characteristics

V_{DD} = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Output High Voltage	I_{OH} = –3 mA, Port I/O push-pull I_{OH} = –10 µA, Port I/O push-pull I_{OH} = –10 mA, Port I/O push-pull	V_{DD} – 0.7 V_{DD} – 0.1 —	— — V_{DD} – 0.8	— — —	V
Output Low Voltage	I_{OL} = 8.5 mA I_{OL} = 10 µA I_{OL} = 25 mA	— — —	— — 1.0	0.6 0.1 —	V
Input High Voltage		2.0	—	—	V
Input Low Voltage		—	—	0.8	V
Input Leakage Current	Weak Pullup Off Weak Pullup On, V_{IN} = 0 V	— —	— 15	±1 50	µA
INT2 Detection Input Low Voltage		—	—	1.0	V
INT2 Detection Input High Voltage		3.0	—	—	V

Table 5.4. Reset Electrical Characteristics

–40 to +85 °C unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
$\overline{RST}$ Output Low Voltage	I_{OL} = 8.5 mA, V_{DD} = 2.7 V to 3.6 V	—	—	0.6	V
$\overline{RST}$ Input High Voltage		0.7 x V_{DD}	—	—	V
$\overline{RST}$ Input Low Voltage		—	—	0.3 x V_{DD}	V
$\overline{RST}$ Input Pullup Current	$\overline{RST}$ = 0.0 V	—	15	40	µA
V_{DD} Monitor Threshold (V_{RST})		2.60	2.65	2.70	V
Missing Clock Detector Time-out	Time from last system clock rising edge to reset initiation	80	580	800	µs
Reset Time Delay	Delay between release of any reset source and code execution at location 0x0000	—	—	250	µs
Minimum $\overline{RST}$ Low Time to Generate a System Reset		15	—	—	µs
V_{DD} Monitor Turn-on Time		—	—	100	µs
V_{DD} Monitor Supply Current		—	15	50	µA

Table 5.7. Internal High-Frequency Oscillator Electrical Characteristics

V_{DD} = 2.7 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	IFCN = 11b	47.3	48	48.7	MHz
Oscillator Supply Current (from V_{DD})	25 °C, V_{DD} = 3.0 V, OSCICN.7 = 1, OCSICN.5 = 0	—	900	—	µA
Power Supply Sensitivity	Constant Temperature	—	110	—	ppm/V
Temperature Sensitivity	Constant Supply	—	25	—	ppm/°C

Table 5.8. Internal Low-Frequency Oscillator Electrical Characteristics

V_{DD} = 2.7 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	OSCLD = 11b	75	80	85	kHz
Oscillator Supply Current (from V_{DD})	25 °C, V_{DD} = 3.0 V, OSCLCN.7 = 1	—	4	—	µA
Power Supply Sensitivity	Constant Temperature	—	0.05	—	%/V
Temperature Sensitivity	Constant Supply	—	65	—	ppm/°C

Table 5.9. External Oscillator Electrical Characteristics

V_{DD} = 2.7 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
External Crystal Frequency		0.02	—	30	MHz
External CMOS Oscillator Frequency		0	—	48	MHz

6.4. Programmable Window Detector

The ADC Programmable Window Detector continuously compares the ADC0 output registers to user-programmed limits, and notifies the system when a desired condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD0WINT in register ADC0CN) can also be used in polled mode. The ADC0 Greater-Than (ADC0GTH, ADC0GTL) and Less-Than (ADC0LTH, ADC0LTL) registers hold the comparison values. The window detector flag can be programmed to indicate when measured data is inside or outside of the user-programmed limits, depending on the contents of the ADC0 Less-Than and ADC0 Greater-Than registers.

SFR Definition 6.5. ADC0GTH: ADC0 Greater-Than Data High Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTH[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC4; SFR Page = All Pages

Bit	Name	Function
7:0	ADC0GTH[7:0]	**ADC0 Greater-Than Data Word High-Order Bits.**

SFR Definition 6.6. ADC0GTL: ADC0 Greater-Than Data Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTL[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC3; SFR Page = All Pages

Bit	Name	Function
7:0	ADC0GTL[7:0]	**ADC0 Greater-Than Data Word Low-Order Bits.**

SFR Definition 6.7. ADC0LTH: ADC0 Less-Than Data High Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0LTH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC6; SFR Page = All Pages

Bit	Name	Function
7:0	ADC0LTH[7:0]	**ADC0 Less-Than Data Word High-Order Bits.**

SFR Definition 6.8. ADC0LTL: ADC0 Less-Than Data Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0LTL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC5; SFR Page = All Pages

Bit	Name	Function
7:0	ADC0LTL[7:0]	**ADC0 Less-Than Data Word Low-Order Bits.**

SFR Definition 6.10. AMX0N: AMUX0 Negative Channel Select

Bit	7	6	5	4	3	2	1	0
Name			AMX0N[5:0]					
Type	R	R	R/W					
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBA; SFR Page = All Pages

Bit	Name	Function
7:6	Unused	Read = 00b; Write = don't care.
5:0	AMX0N[5:0]	**AMUX0 Negative Input Selection.**

AMX0N	32-pin Packages	48-pin Packages	AMX0N	32-pin Packages	48-pin Packages
000000:	P1.0	P2.0	010010:	P0.1	P0.4
000001:	P1.1	P2.1	010011:	P0.4	P1.1
000010:	P1.2	P2.2	010100:	P0.5	P1.2
000011:	P1.3	P2.3	010101:	Reserved	P1.0
000100:	P1.4	P2.5	010110:	Reserved	P1.3
000101:	P1.5	P2.6	010111:	Reserved	P1.6
000110:	P1.6	P3.0	011000:	Reserved	P1.7
000111:	P1.7	P3.1	011001:	Reserved	P2.4
001000:	P2.0	P3.4	011010:	Reserved	P2.7
001001:	P2.1	P3.5	011011:	Reserved	P3.2
001010:	P2.2	P3.7	011100:	Reserved	P3.3
001011:	P2.3	P4.0	011101:	Reserved	P3.6
001100:	P2.4	P4.3	011110:	VREF	VREF
001101:	P2.5	P4.4	011111:	GND (Single-Ended Measurement)	GND (Single-Ended Measurement)
001110:	P2.6	P4.5	100000:	Reserved	P4.1
001111:	P2.7	P4.6	100001:	Reserved	P4.2
010000:	P3.0	Reserved	100010:	Reserved	P4.7
010001:	P0.0	P0.3	100011 - 111111:	Reserved	Reserved

8.1. Comparator Multiplexers

C8051F388/9/A/B devices include an analog input multiplexer to connect Port I/O pins to the comparator inputs. The Comparator inputs are selected in the CPTnMX registers (SFR Definition 8.5 and SFR Definition 8.6). The CMXnP2–CMXnP0 bits select the Comparator positive input; the CMXnN2–CMXnN0 bits select the Comparator negative input.

Important Note About Comparator Inputs: The Port pins selected as comparator inputs should be configured as analog inputs in their associated Port configuration register, and configured to be skipped by the Crossbar (for details on Port configuration, see Section “20.3. General Purpose Port I/O” on page 155).

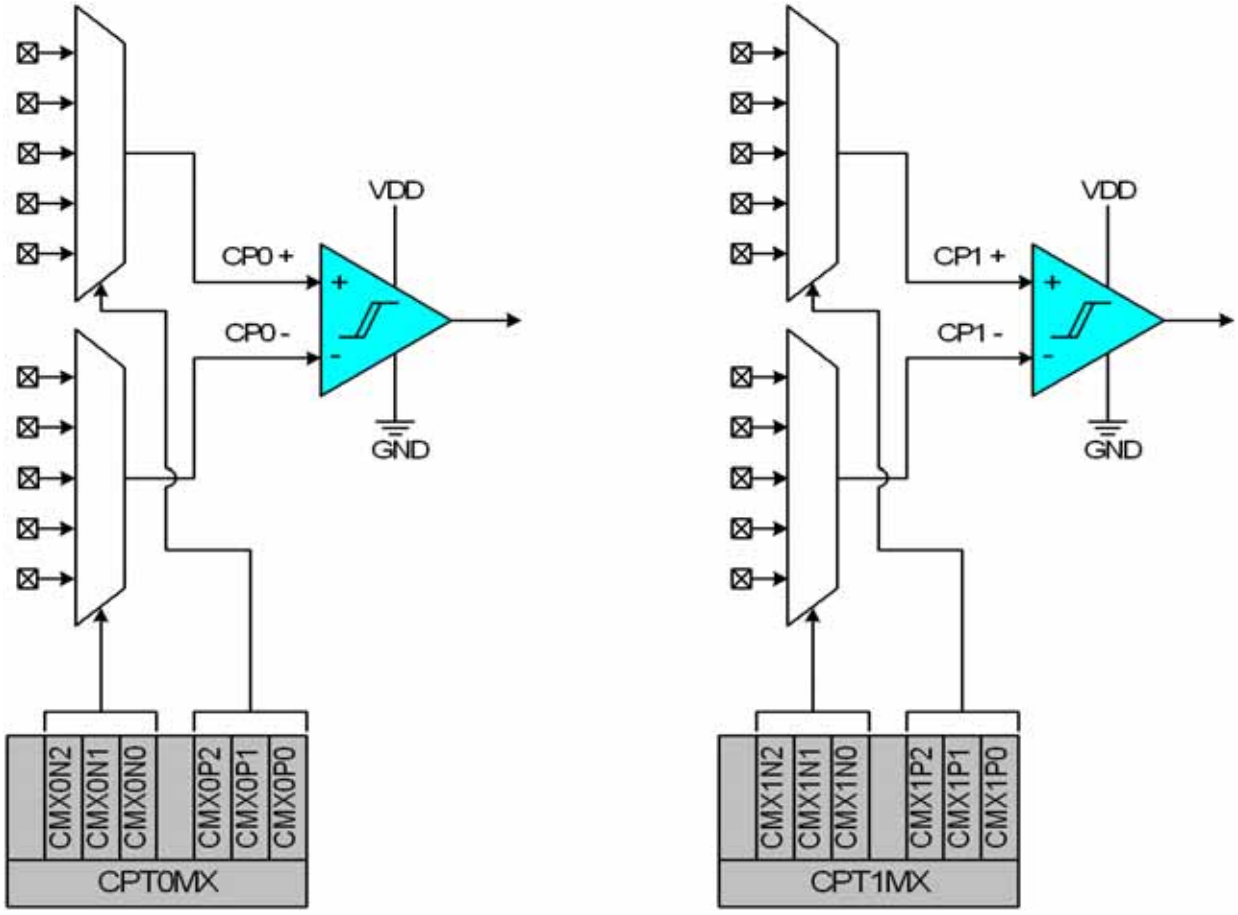

Figure 8.4. Comparator Input Multiplexer Block Diagram

Notes on Registers, Operands and Addressing Modes:
Rn - Register R0–R7 of the currently selected register bank. **@Ri** - Data RAM location addressed indirectly through R0 or R1. **rel** - 8-bit, signed (two's complement) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps. **direct** - 8-bit internal data location's address. This could be a direct-access Data RAM location (0x00–0x7F) or an SFR (0x80–0xFF). **#data** - 8-bit constant **#data16** - 16-bit constant **bit** - Direct-accessed bit in Data RAM or SFR **addr11** - 11-bit destination address used by ACALL and AJMP. The destination must be within the same 2 kB page of program memory as the first byte of the following instruction. **addr16** - 16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 8 kB program memory space. There is one unused opcode (0xA5) that performs the same function as NOP. All mnemonics copyrighted © Intel Corporation 1980.

SFR Definition 14.1. EMI0CN: External Memory Interface Control

Bit	7	6	5	4	3	2	1	0
Name	PGSEL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xAA; SFR Page = All Pages

Bit	Name	Function
7:0	PGSEL[7:0]	**XRAM Page Select Bits.** The XRAM Page Select Bits provide the high byte of the 16-bit external data memory address when using an 8-bit MOVX command, effectively selecting a 256-byte page of RAM. 0x00: 0x0000 to 0x00FF 0x01: 0x0100 to 0x01FF ... 0xFE: 0xFE00 to 0xFEFF 0xFF: 0xFF00 to 0xFFFF

Table 15.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Page	Description	Page
PCA0CPL2	0xEB	All Pages	PCA Capture 2 Low	276
PCA0CPL3	0xED	All Pages	PCA Capture 3 Low	276
PCA0CPL4	0xFD	All Pages	PCA Capture 4 Low	276
PCA0CPM0	0xDA	All Pages	PCA Module 0 Mode Register	274
PCA0CPM1	0xDB	All Pages	PCA Module 1 Mode Register	274
PCA0CPM2	0xDC	All Pages	PCA Module 2 Mode Register	274
PCA0CPM3	0xDD	All Pages	PCA Module 3 Mode Register	274
PCA0CPM4	0xDE	All Pages	PCA Module 4 Mode Register	274
PCA0H	0xFA	All Pages	PCA Counter High	275
PCA0L	0xF9	All Pages	PCA Counter Low	275
PCA0MD	0xD9	All Pages	PCA Mode	273
PCON	0x87	All Pages	Power Control	74
PFE0CN	0xAF	All Pages	Prefetch Engine Control	84
PSCTL	0x8F	All Pages	Program Store R/W Control	133
PSW	0xD0	All Pages	Program Status Word	83
REF0CN	0xD1	All Pages	Voltage Reference Control	59
REG01CN	0xC9	All Pages	Voltage Regulator 0 and 1 Control	71
RSTSRC	0xEF	All Pages	Reset Source Configuration/Status	128
SBCON1	0xAC	All Pages	UART1 Baud Rate Generator Control	209
SBRLH1	0xB5	All Pages	UART1 Baud Rate Generator High	209
SBRLL1	0xB4	All Pages	UART1 Baud Rate Generator Low	210
SBUF0	0x99	All Pages	UART0 Data Buffer	199
SBUF1	0xD3	All Pages	UART1 Data Buffer	208
SCON0	0x98	All Pages	UART0 Control	198
SCON1	0xD2	All Pages	UART1 Control	206
SFRPAGE	0xBF	All Pages	SFR Page Select	105
SMB0ADM	0xCE	0	SMBus0 Address Mask	180
SMB0ADR	0xCF	0	SMBus0 Address	179
SMB0CF	0xC1	0	SMBus0 Configuration	172
SMB0CN	0xC0	0	SMBus0 Control	176
SMB0DAT	0xC2	0	SMBus0 Data	182
SMB1ADM	0xCE	F	SMBus1 Address Mask	181
SMB1ADR	0xCF	F	SMBus1 Address	180
SMB1CF	0xC1	F	SMBus1 Configuration	172

Accessing FLASH **from the C2 debug interface**:

1. Any unlocked page may be read, written, or erased.
2. Locked pages cannot be read, written, or erased.
3. The page containing the Lock Byte may be read, written, or erased if it is unlocked.
4. Reading the contents of the Lock Byte with no pages locked is always permitted.
5. Reading the contents of the Lock Byte with any pages locked is not permitted.
6. Locking additional pages (changing 1s to 0s in the Lock Byte) is not permitted.
7. Unlocking FLASH pages (changing 0s to 1s in the Lock Byte) requires the C2 Device Erase command, which erases all FLASH pages including the page containing the Lock Byte and the Lock Byte itself.
8. The Reserved Area cannot be read, written, or erased.

Accessing FLASH **from user firmware** executing on an **unlocked page**:

1. Any unlocked page except the page containing the Lock Byte may be read, written, or erased.
2. Locked pages cannot be read, written, or erased.
3. The page containing the Lock Byte cannot be erased. It may be read or written only if it is unlocked.
4. Reading the contents of the Lock Byte with no pages locked is always permitted.
5. Reading the contents of the Lock Byte with any pages locked is not permitted.
6. Locking additional pages (changing 1s to 0s in the Lock Byte) is not permitted.
7. Unlocking FLASH pages (changing 0s to 1s in the Lock Byte) is not permitted.
8. The Reserved Area cannot be read, written, or erased. Any attempt to access the reserved area, or any other locked page, will result in a FLASH Error device reset.

Accessing FLASH **from user firmware** executing on a **locked page**:

1. Any unlocked page except the page containing the Lock Byte may be read, written, or erased.
2. Any locked page except the page containing the Lock Byte may be read, written, or erased.
3. The page containing the Lock Byte cannot be erased. It may only be read or written.
4. Reading the contents of the Lock Byte is always permitted.
5. Locking additional pages (changing 1s to 0s in the Lock Byte) is not permitted.
6. Unlocking FLASH pages (changing 0s to 1s in the Lock Byte) is not permitted.
7. The Reserved Area cannot be read, written, or erased. Any attempt to access the reserved area, or any other locked page, will result in a FLASH Error device reset.

SFR Definition 18.3. FLSCL: Flash Scale

Bit	7	6	5	4	3	2	1	0
Name	FOSE	Reserved		FLRT	Reserved			
Type	R/W	R/W		R/W	R/W			
Reset	1	0	0	0	0	0	0	0

SFR Address = 0xB6; SFR Page = All Pages

Bit	Name	Function
7	FOSE	**Flash One-shot Enable.** This bit enables the Flash read one-shot. When the Flash one-shot disabled, the Flash sense amps are enabled for a full clock cycle during Flash reads. At system clock frequencies below 10 MHz, disabling the Flash one-shot will increase system power consumption. 0: Flash one-shot disabled. 1: Flash one-shot enabled.
6:5	Reserved	Must write 00b.
4	FLRT	**FLASH Read Time.** This bit should be programmed to the smallest allowed value, according to the system clock speed. 0: SYSCLK <= 25 MHz. 1: SYSCLK <= 48 MHz.
3:0	Reserved	Must write 0000b.

SFR Definition 20.3. XBR2: Port I/O Crossbar Register 2

Bit	7	6	5	4	3	2	1	0
Name							SMB1E	URT1E
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE3; SFR Page = All Pages

Bit	Name	Function
7:2	Reserved	Must write 000000b
1	SMB1E	**SMBus1 I/O Enable.** 0: SMBus1 I/O unavailable at Port pins. 1: SMBus1 I/O routed to Port pins.
0	URT1E	**UART1 I/O Enable.** 0: UART1 I/O unavailable at Port pins. 1: UART1 TX1, RX1 routed to Port pins.

20.3. General Purpose Port I/O

Port pins that remain unassigned by the Crossbar and are not used by analog peripherals can be used for general purpose I/O. Ports 3-0 are accessed through corresponding special function registers (SFRs) that are both byte addressable and bit addressable. Port 4 (C8051F388/A only) uses an SFR which is byte-addressable. When writing to a Port, the value written to the SFR is latched to maintain the output data value at each pin. When reading, the logic levels of the Port's input pins are returned regardless of the XBRn settings (i.e., even when the pin is assigned to another signal by the Crossbar, the Port register can always read its corresponding Port I/O pin). The exception to this is the execution of the read-modify-write instructions. The read-modify-write instructions when operating on a Port SFR are the following: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ and MOV, CLR or SETB, when the destination is an individual bit in a Port SFR. For these instructions, the value of the register (not the pin) is read, modified, and written back to the SFR.

SFR Definition 20.14. P2MDOUT: Port 2 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P2MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA6; SFR Page = All Pages

Bit	Name	Function
7:0	P2MDOUT[7:0]	**Output Configuration Bits for P2.7–P2.0 (respectively).** These bits are ignored if the corresponding bit in register P2MDIN is logic 0. 0: Corresponding P2.n Output is open-drain. 1: Corresponding P2.n Output is push-pull.

SFR Definition 20.15. P2SKIP: Port 2 Skip

Bit	7	6	5	4	3	2	1	0
Name	P2SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD6; SFR Page = All Pages

Bit	Name	Function
7:0	P2SKIP[3:0]	**Port 2 Crossbar Skip Enable Bits.** These bits select Port 2 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P2.n pin is not skipped by the Crossbar. 1: Corresponding P2.n pin is skipped by the Crossbar.

Table 21.6. SMBus Status Decoding: Hardware ACK Enabled (EHACK = 1) (Continued)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Master Receiver	1000	0	0	1	A master data byte was received; ACK sent.	Set ACK for next data byte; Read SMB0DAT.	0	0	1	1000
						Set NACK to indicate next data byte as the last data byte; Read SMB0DAT.	0	0	0	1000
						Initiate repeated START.	1	0	0	1110
						Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	X	1100
		0	0	0	A master data byte was received; NACK sent (last byte).	Read SMB0DAT; send STOP.	0	1	0	—
						Read SMB0DAT; Send STOP followed by START.	1	1	0	1110
						Initiate repeated START.	1	0	0	1110
						Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	X	1100
Slave Transmitter	0100	0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	X	0001
		0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	X	0100
		0	1	X	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	X	0001
	0101	0	X	X	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	X	—

SFR Definition 25.15. TMR3RLL: Timer 3 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x92; SFR Page = 0

Bit	Name	Function
7:0	TMR3RLL[7:0]	**Timer 3 Reload Register Low Byte.** TMR3RLL holds the low byte of the reload value for Timer 3.

SFR Definition 25.16. TMR3RLH: Timer 3 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3RLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x93; SFR Page = 0

Bit	Name	Function
7:0	TMR3RLH[7:0]	**Timer 3 Reload Register High Byte.** TMR3RLH holds the high byte of the reload value for Timer 3.

SFR Definition 25.17. TMR3L: Timer 3 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x94; SFR Page = 0

Bit	Name	Function
7:0	TMR3L[7:0]	**Timer 3 Low Byte.** In 16-bit mode, the TMR3L register contains the low byte of the 16-bit Timer 3. In 8-bit mode, TMR3L contains the 8-bit low byte timer value.

SFR Definition 25.24. TMR5CN: Timer 5 Control

Bit	7	6	5	4	3	2	1	0
Name	TF5H	TF5L	TF5LEN		T5SPLIT	TR5		T5XCLK
Type	R/W	R/W	R/W	R	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC8; SFR Page = F; Bit-Addressable

Bit	Name	Function
7	TF5H	**Timer 5 High Byte Overflow Flag.** Set by hardware when the Timer 5 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 5 overflows from 0xFFFF to 0x0000. When the Timer 5 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 5 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF5L	**Timer 5 Low Byte Overflow Flag.** Set by hardware when the Timer 5 low byte overflows from 0xFF to 0x00. TF5L will be set when the low byte overflows regardless of the Timer 5 mode. This bit is not automatically cleared by hardware.
5	TF5LEN	**Timer 5 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 5 Low Byte interrupts. If Timer 5 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 5 overflows.
4	Unused	Read = 0b; Write = don't care.
3	T5SPLIT	**Timer 5 Split Mode Enable.** When this bit is set, Timer 5 operates as two 8-bit timers with auto-reload. 0: Timer 5 operates in 16-bit auto-reload mode. 1: Timer 5 operates as two 8-bit auto-reload timers.
2	TR5	**Timer 5 Run Control.** Timer 5 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR5H only; TMR5L is always enabled in split mode.
1	Unused	Read = 0b; Write = don't care.
0	T5XCLK	**Timer 5 External Clock Select.** This bit selects the external clock source for Timer 5. However, the Timer 5 Clock Select bits (T5MH and T5ML in register CKCON1) may still be used to select between the external clock and the system clock for either timer. 0: Timer 5 clock is the system clock divided by 12. 1: Timer 5 clock is the external clock divided by 8 (synchronized with SYSCLK).

26.3. Capture/Compare Modules

Each module can be configured to operate independently in one of six operation modes: edge-triggered capture, software timer, high-speed output, frequency output, 8-bit pulse width modulator, or 16-bit pulse width modulator. Each module has Special Function Registers (SFRs) associated with it in the CIP-51 system controller. These registers are used to exchange data with a module and configure the module's mode of operation. Table 26.2 summarizes the bit settings in the PCA0CPMn register used to select the PCA capture/compare module's operating mode. Setting the ECCFn bit in a PCA0CPMn register enables the module's CCFn interrupt.

Table 26.2. PCA0CPM Bit Settings for PCA Capture/Compare Modules

Operational Mode	PCA0CPMn							
Bit Number	7	6	5	4	3	2	1	0
Capture triggered by positive edge on CEXn	X	X	1	0	0	0	0	A
Capture triggered by negative edge on CEXn	X	X	0	1	0	0	0	A
Capture triggered by any transition on CEXn	X	X	1	1	0	0	0	A
Software Timer	X	B	0	0	1	0	0	A
High Speed Output	X	B	0	0	1	1	0	A
Frequency Output	X	B	0	0	0	1	1	A
8-Bit Pulse Width Modulator	0	B	0	0	C	0	1	A
16-Bit Pulse Width Modulator	1	B	0	0	C	0	1	A

Notes:

1. X = Don't Care (no functional difference for individual module if 1 or 0).
2. A = Enable interrupts for this module (PCA interrupt triggered on CCFn set to 1).
3. B = When set to 0, the digital comparator is off. For high speed and frequency output modes, the associated pin will not toggle. In any of the PWM modes, this generates a 0% duty cycle (output = 0).
4. C = When set, a match event will cause the CCFn flag for the associated channel to be set.