Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	A/D 21x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f38b-gm

26.3.5. 8-bit Pulse Width Modulator Mode 267
26.3.6. 16-Bit Pulse Width Modulator Mode 268
26.4. Watchdog Timer Mode 269
26.4.1. Watchdog Timer Operation 269
26.4.2. Watchdog Timer Usage 270
26.5. Register Descriptions for PCA0 272
27. C2 Interface 277
27.1. C2 Interface Registers 277
27.2. C2 Pin Sharing 280
28. Revision Specific Behavior 281
28.1. Revision Identification 281
28.2. INT2 Pin Not Connected 283
Document Change List 284
Contact Information 285

2. C8051F34x Compatibility

The C8051F388/9/A/B family is designed to be a pin and code compatible replacement for the C8051F34x device family. The C8051F388/9/A/B device should function as a drop-in replacement for the C8051F34x devices in most applications that do not use USB. Table 2.1 lists recommended replacement part numbers for C8051F34x devices. See “2.1. Hardware Incompatibilities” to determine if any changes are necessary when upgrading an existing C8051F34x design to the C8051F388/9/A/B.

Table 2.1. C8051F388/9/A/B Replacement Part Numbers

C8051F34x Part Number	C8051F38x Part Number
C8051F340-GQ	C8051F388-B-GQ
C8051F341-GQ	C8051F38A-B-GQ
C8051F342-GQ	C8051F389-B-GQ
C8051F342-GM	C8051F389-B-GM
C8051F343-GQ	C8051F38B-B-GQ
C8051F343-GM	C8051F38B-B-GM
C8051F344-GQ	C8051F388-B-GQ
C8051F345-GQ	C8051F38A-B-GQ
C8051F346-GQ	C8051F389-B-GQ
C8051F346-GM	C8051F389-B-GM
C8051F347-GQ	C8051F38B-B-GQ
C8051F347-GM	C8051F38B-B-GM
C8051F348-GQ	C8051F38A-B-GQ
C8051F349-GQ	C8051F38B-B-GQ
C8051F349-GM	C8051F38B-B-GM
C8051F34A-GQ	C8051F389-B-GQ
C8051F34A-GM	C8051F389-B-GM
C8051F34B-GQ	C8051F38B-B-GQ
C8051F34B-GM	C8051F38B-B-GM
C8051F34C-GQ	C8051F388-B-GQ
C8051F34D-GQ	C8051F389-B-GQ

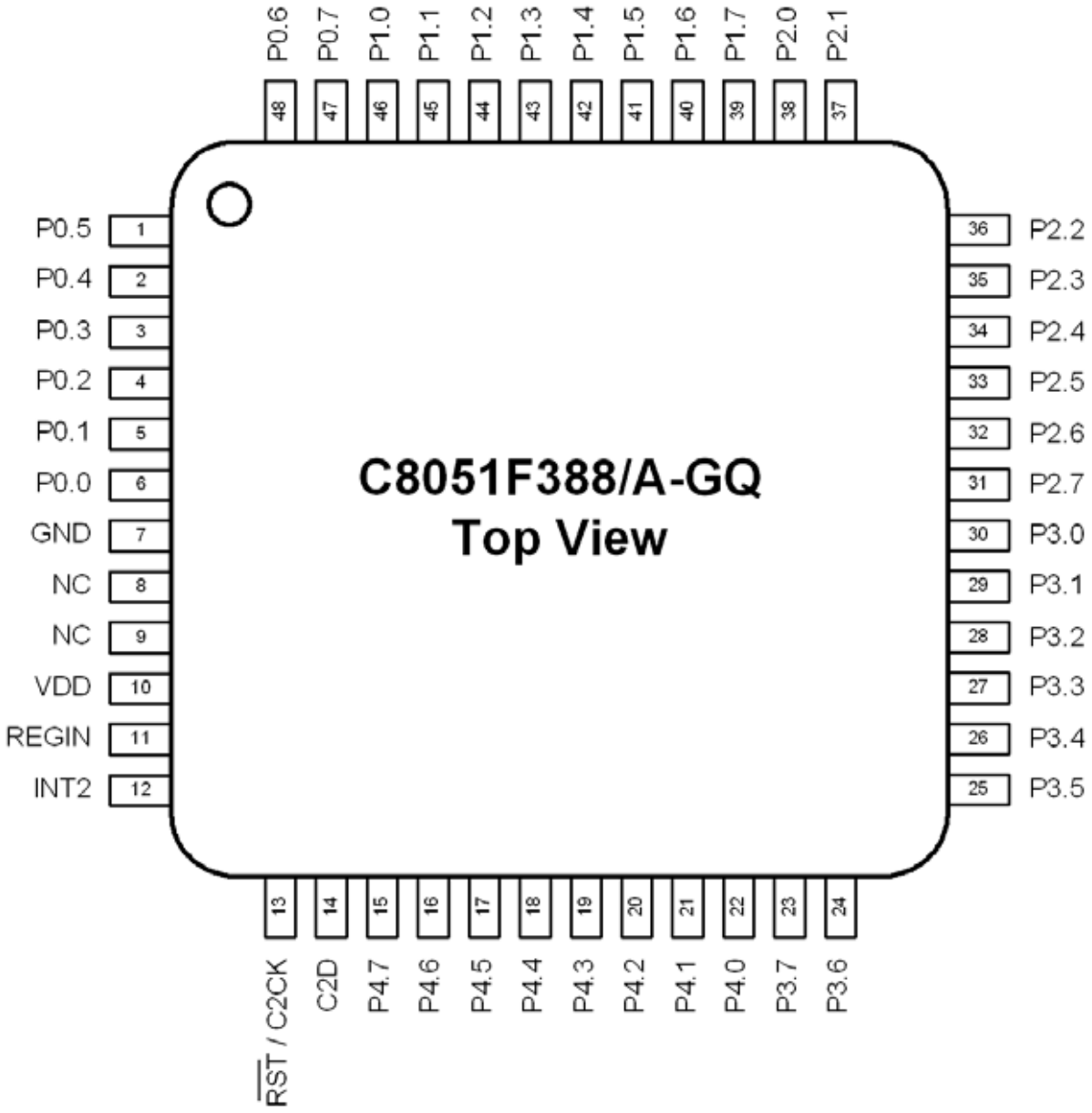


Figure 3.1. TQFP-48 (C8051F388/A) Pinout Diagram (Top View)

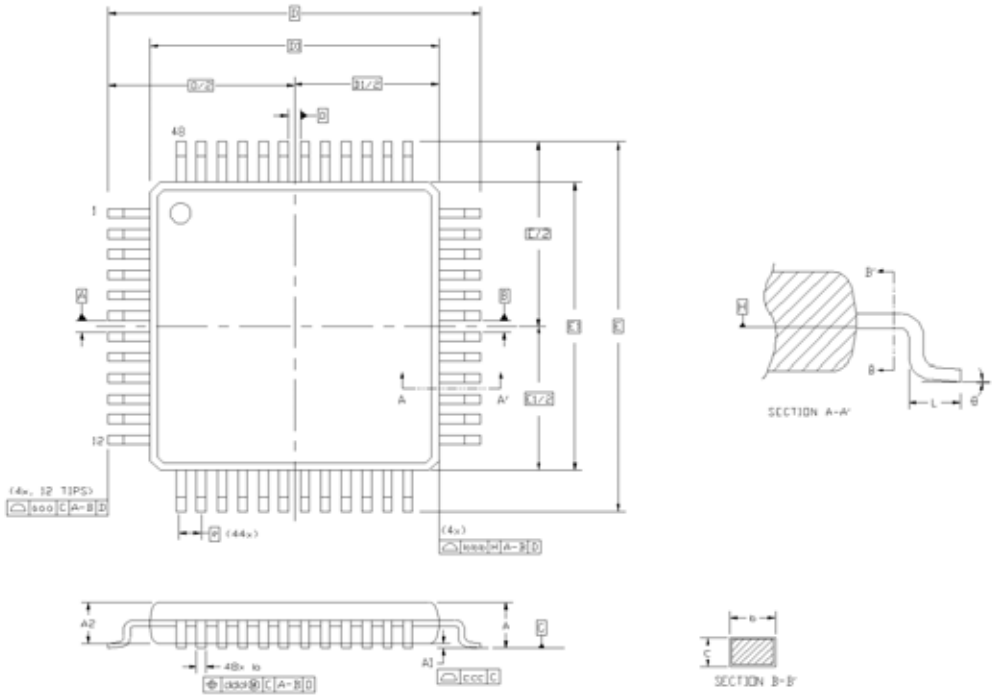


Figure 3.2. TQFP-48 Package Diagram

Table 3.2. TQFP-48 Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—	—	1.20	E		9.00 BSC	
A1	0.05	—	0.15	E1		7.00 BSC	
A2	0.95	1.00	1.05	L	0.45	0.60	0.75
b	0.17	0.22	0.27	aaa		0.20	
c	0.09	—	0.20	bbb		0.20	
D		9.00 BSC		ccc		0.08	
D1		7.00 BSC		ddd		0.08	
e		0.50 BSC		q	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.3.3. Settling Time Requirements

A minimum tracking time is required before each conversion to ensure that an accurate conversion is performed. This tracking time is determined by the AMUX0 resistance, the ADC0 sampling capacitance, any external source resistance, and the accuracy required for the conversion. Note that in low-power tracking mode, three SAR clocks are used for tracking at the start of every conversion. For most applications, these three SAR clocks will meet the minimum tracking time requirements.

Figure 6.5 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation 6.1. See Table 5.10 for ADC0 minimum settling time requirements as well as the mux impedance and sampling capacitor values.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

Equation 6.1. ADC0 Settling Time Requirements

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the AMUX0 resistance and any external source resistance.
n is the ADC resolution in bits (10).

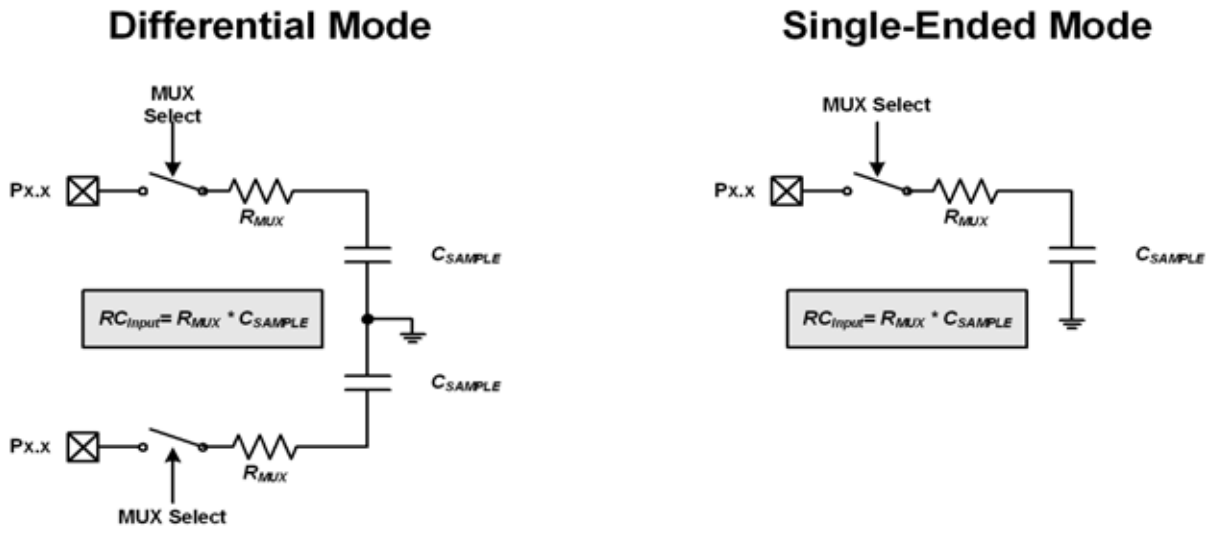


Figure 6.5. ADC0 Equivalent Input Circuits

14.5.3. Split Mode with Bank Select

When EMI0CF.[3:2] are set to 10, the XRAM memory map is split into two areas, on-chip space and off-chip space.

- Effective addresses below the internal XRAM size boundary will access on-chip XRAM space.
- Effective addresses above the internal XRAM size boundary will access off-chip space.
- 8-bit MOVX operations use the contents of EMI0CN to determine whether the memory access is on-chip or off-chip. The upper 8-bits of the Address Bus A[15:8] are determined by EMI0CN, and the lower 8-bits of the Address Bus A[7:0] are determined by R0 or R1. All 16-bits of the Address Bus A[15:0] are driven in “Bank Select” mode.
- 16-bit MOVX operations use the contents of DPTR to determine whether the memory access is on-chip or off-chip, and the full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

14.5.4. External Only

When EMI0CF[3:2] are set to 11, all MOVX operations are directed to off-chip space. On-chip XRAM is not visible to the CPU. This mode is useful for accessing off-chip memory located between 0x0000 and the internal XRAM size boundary.

- 8-bit MOVX operations ignore the contents of EMI0CN. The upper Address bits A[15:8] are not driven (identical behavior to an off-chip access in “Split Mode without Bank Select” described above). This allows the user to manipulate the upper address bits at will by setting the Port state directly. The lower 8-bits of the effective address A[7:0] are determined by the contents of R0 or R1.
- 16-bit MOVX operations use the contents of DPTR to determine the effective address A[15:0]. The full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

14.6.1. Non-multiplexed Mode

14.6.1.1. 16-bit MOVX: EMI0CF[4:2] = 101, 110, or 111

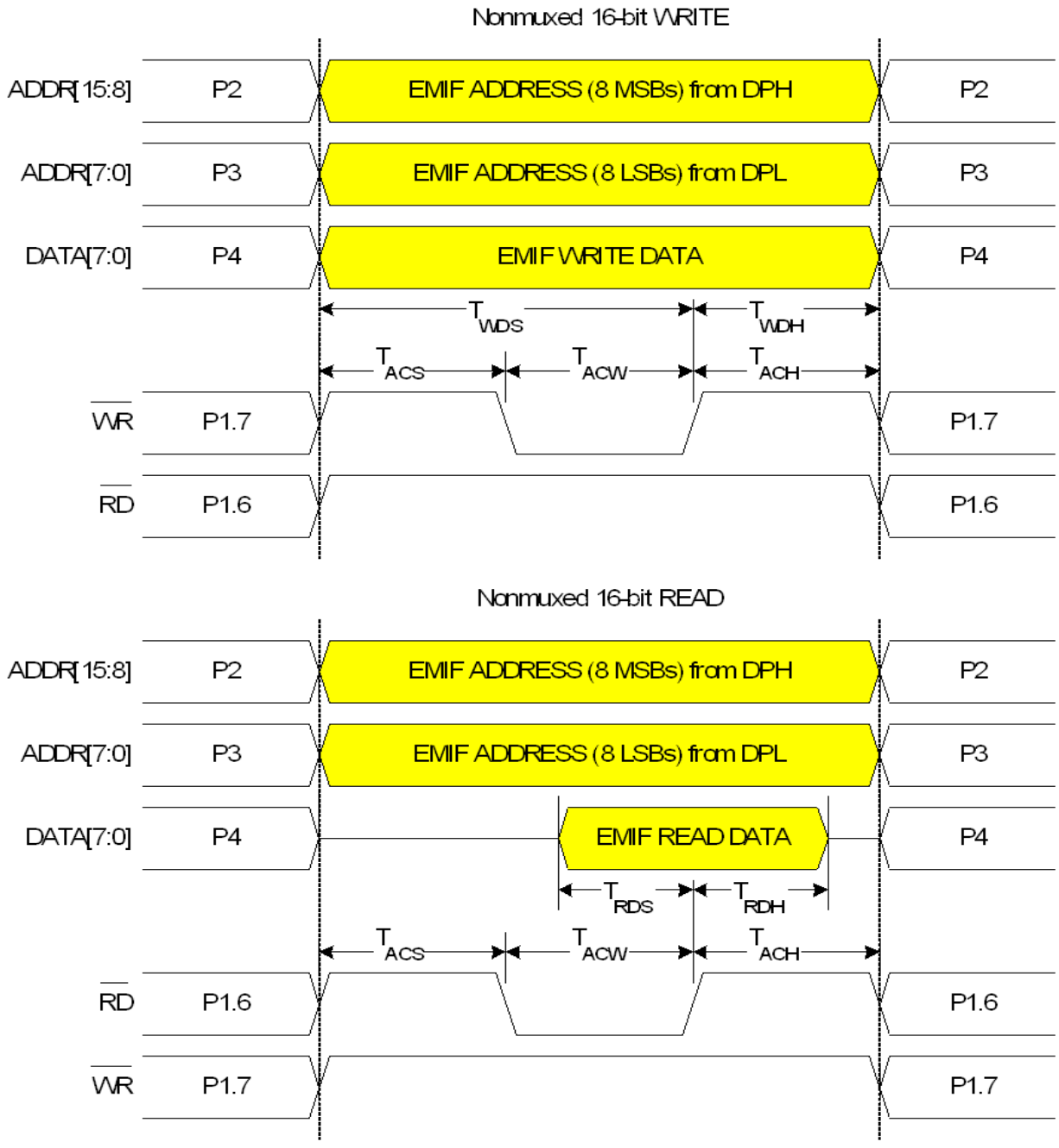


Figure 14.4. Non-Multiplexed 16-bit MOVX Timing

Table 15.2. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Page	Description	Page
ACC	0xE0	All Pages	Accumulator	82
ADC0CF	0xBC	All Pages	ADC0 Configuration	49
ADC0CN	0xE8	All Pages	ADC0 Control	51
ADC0GTH	0xC4	All Pages	ADC0 Greater-Than Compare High	52
ADC0GTL	0xC3	All Pages	ADC0 Greater-Than Compare Low	52
ADC0H	0xBE	All Pages	ADC0 High	50
ADC0L	0xBD	All Pages	ADC0 Low	50
ADC0LTH	0xC6	All Pages	ADC0 Less-Than Compare Word High	53
ADC0LTL	0xC5	All Pages	ADC0 Less-Than Compare Word Low	53
AMX0N	0xBA	All Pages	AMUX0 Negative Channel Select	57
AMX0P	0xBB	All Pages	AMUX0 Positive Channel Select	56
B	0xF0	All Pages	B Register	82
CKCON	0x8E	All Pages	Clock Control	225
CKCON1	0xE4	F	Clock Control 1	226
CLKMUL	0xB9	0	Clock Multiplier	141
CLKSEL	0xA9	All Pages	Clock Select	138
CPT0CN	0x9B	All Pages	Comparator0 Control	63
CPT0MD	0x9D	All Pages	Comparator0 Mode Selection	64
CPT0MX	0x9F	All Pages	Comparator0 MUX Selection	68
CPT1CN	0x9A	All Pages	Comparator1 Control	65
CPT1MD	0x9C	All Pages	Comparator1 Mode Selection	66
CPT1MX	0x9E	All Pages	Comparator1 MUX Selection	69
DPH	0x83	All Pages	Data Pointer High	81
DPL	0x82	All Pages	Data Pointer Low	81
EIE1	0xE6	All Pages	Extended Interrupt Enable 1	117
EIE2	0xE7	All Pages	Extended Interrupt Enable 2	119
EIP1	0xF6	All Pages	Extended Interrupt Priority 1	118
EIP2	0xF7	All Pages	Extended Interrupt Priority 2	120
EMI0CF	0x85	All Pages	External Memory Interface Configuration	91
EMI0CN	0xAA	All Pages	External Memory Interface Control	90
EMI0TC	0x84	All Pages	External Memory Interface Timing	97
FLKEY	0xB7	All Pages	Flash Lock and Key	134
FLSCL	0xB6	All Pages	Flash Scale	135

17.2. Power-Fail Reset / V_{DD} Monitor

When a powerdown transition or power irregularity causes V_{DD} to drop below V_{RST}, the power supply monitor will drive the $\overline{RST}$ pin low and hold the CIP-51 in a reset state (see Figure 17.2). When V_{DD} returns to a level above V_{RST}, the CIP-51 will be released from the reset state. Note that even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if V_{DD} dropped below the level required for data retention. If the PORSF flag reads 1, the data may no longer be valid. The V_{DD} monitor is enabled after power-on resets. Its defined state (enabled/disabled) is not altered by any other reset source. For example, if the V_{DD} monitor is disabled by code and a software reset is performed, the V_{DD} monitor will still be disabled after the reset.

I**mportant Note:** If the V_{DD} monitor is being turned on from a disabled state, it should be enabled before it is selected as a reset source. Selecting the V_{DD} monitor as a reset source before it is enabled and stabilized may cause a system reset. In some applications, this reset may be undesirable. If this is not desirable in the application, a delay should be introduced between enabling the monitor and selecting it as a reset source. The procedure for enabling the V_{DD} monitor and configuring it as a reset source from a disabled state is shown below:

1. Enable the V_{DD} monitor (VDMEN bit in VDM0CN = 1).
2. If necessary, wait for the V_{DD} monitor to stabilize (see Table 5.4 for the V_{DD} Monitor turn-on time).
3. Select the V_{DD} monitor as a reset source (PORSF bit in RSTSRC = 1).

See Figure 17.2 for V_{DD} monitor timing; note that the power-on-reset delay is not incurred after a V_{DD} monitor reset. See Table 5.4 for complete electrical characteristics of the V_{DD} monitor.

18. Flash Memory

On-chip, re-programmable Flash memory is included for program code and non-volatile data storage. The Flash memory can be programmed in-system through the C2 interface or by software using the MOVX instruction. Once cleared to logic 0, a Flash bit must be erased to set it back to logic 1. Flash bytes would typically be erased (set to 0xFF) before being reprogrammed. The write and erase operations are automatically timed by hardware for proper execution; data polling to determine the end of the write/erase operation is not required. Code execution is stalled during a Flash write/erase operation.

18.1. Programming The Flash Memory

The simplest means of programming the Flash memory is through the C2 interface using programming tools provided by Silicon Labs or a third party vendor. This is the only means for programming a non-initialized device. For details on the C2 commands to program Flash memory, see Section “27. C2 Interface” on page 277.

To ensure the integrity of Flash contents, it is strongly recommended that the V_{DD} monitor be left enabled in any system which writes or erases Flash memory from code. It is also crucial to ensure that the FLRT bit in register FLSCL be set to '1' if a clock speed higher than 25 MHz is being used for the device.

18.1.1. Flash Lock and Key Functions

Flash writes and erases by user software are protected with a lock and key function. The Flash Lock and Key Register (FLKEY) must be written with the correct key codes, in sequence, before Flash operations may be performed. The key codes are: 0xA5, 0xF1. The timing does not matter, but the codes must be written in order. If the key codes are written out of order, or the wrong codes are written, Flash writes and erases will be disabled until the next system reset. Flash writes and erases will also be disabled if a Flash write or erase is attempted before the key codes have been written properly. The Flash lock resets after each write or erase; the key codes must be written again before a following Flash operation can be performed. The FLKEY register is detailed in SFR Definition 18.2.

18.1.2. Flash Erase Procedure

The Flash memory can be programmed by software using the MOVX write instruction with the address and data byte to be programmed provided as normal operands. Before writing to Flash memory using MOVX, Flash write operations must be enabled by: (1) Writing the Flash key codes in sequence to the Flash Lock register (FLKEY); and (2) Setting the PSWE Program Store Write Enable bit (PSCTL.0) to logic 1 (this directs the MOVX writes to target Flash memory). The PSWE bit remains set until cleared by software.

A write to Flash memory can clear bits to logic 0 but cannot set them; only an erase operation can set bits to logic 1 in Flash. **A byte location to be programmed must be erased before a new value is written.** The Flash memory is organized in 512-byte pages. The erase operation applies to an entire page (setting all bytes in the page to 0xFF). To erase an entire 512-byte page, perform the following steps:

1. Disable interrupts (recommended).
2. Write the first key code to FLKEY: 0xA5.
3. Write the second key code to FLKEY: 0xF1.
4. Set the PSEE bit (register PSCTL).
5. Set the PSWE bit (register PSCTL).
6. Using the MOVX instruction, write a data byte to any location within the 512-byte page to be erased.
7. Clear the PSWE bit (register PSCTL).
8. Clear the PSEE bit (register PSCTI).

19.3. Clock Multiplier

The C8051F388/9/A/B device includes a 48 MHz high-frequency oscillator instead of a 12 MHz oscillator and a 4x Clock Multiplier. For compatibility with C8051F34x and C8051F32x devices however, the CLKMUL register (SFR Definition 19.4) behaves as if the Clock Multiplier is present and working.

SFR Definition 19.4. CLKMUL: Clock Multiplier Control

Bit	7	6	5	4	3	2	1	0
Name	MULEN	MULINIT	MULRDY				MULSEL[1:0]	
Type	R	R	R	R	R	R	R	
Reset	1	1	1	0	0	0	0	0

SFR Address = 0xB9; SFR Page = 0

Bit	Name	Description
7	MULEN	**Clock Multiplier Enable Bit.** This bit always reads 1.
6	MULINIT	**Clock Multiplier Initialize Bit.** This bit always reads 1.
5	MULRDY	**Clock Multiplier Ready Bit.** This bit always reads 1.
4:2	Unused	Read = 000b; Write = don't care
1:0	MULSEL[1:0]	**Clock Multiplier Input Select Bits.** These bits always read 00.

SFR Definition 20.20. P4: Port 4

Bit	7	6	5	4	3	2	1	0
Name	P4[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC7; SFR Page = All Pages

Bit	Name	Description	Write	Read
7:0	P4[7:0]	**Port 4 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P4.n Port pin is logic LOW. 1: P4.n Port pin is logic HIGH.

SFR Definition 20.21. P4MDIN: Port 4 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P4MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF5; SFR Page = All Pages

Bit	Name	Function
7:0	P4MDIN[7:0]	**Analog Configuration Bits for P4.7–P4.0 (respectively).** Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled. 0: Corresponding P4.n pin is configured for analog mode. 1: Corresponding P4.n pin is not configured for analog mode.

low. With the associated timer enabled and configured to overflow after 25 ms (and SMBnTOE set), the timer interrupt service routine can be used to reset (disable and re-enable) the SMBus in the event of an SCL low timeout.

21.3.5. SCL High (SMBus Free) Timeout

The SMBus specification stipulates that if the SCL and SDA lines remain high for more that 50 µs, the bus is designated as free. When the SMBnFTE bit in SMBnCF is set, the bus will be considered free if SCL and SDA remain high for more than 10 SMBus clock source periods (as defined by the timer configured for the SMBus clock source). If the SMBus is waiting to generate a Master START, the START will be generated following this timeout. A clock source is required for free timeout detection, even in a slave-only implementation.

21.4. Using the SMBus

The SMBus can operate in both Master and Slave modes. The interface provides timing and shifting control for serial transfers; higher level protocol is determined by user software. The SMBus interface provides the following application-independent features:

- Byte-wise serial data transfers
- Clock signal generation on SCL (Master Mode only) and SDA data synchronization
- Timeout/bus error recognition, as defined by the SMB0CF configuration register
- START/STOP timing, detection, and generation
- Bus arbitration
- Interrupt generation
- Status information
- Optional hardware recognition of slave address and automatic acknowledgement of address/data

SMBus interrupts are generated for each data byte or slave address that is transferred. When hardware acknowledgment is disabled, the point at which the interrupt is generated depends on whether the hardware is acting as a data transmitter or receiver. When a transmitter (i.e., sending address/data, receiving an ACK), this interrupt is generated after the ACK cycle so that software may read the received ACK value; when receiving data (i.e., receiving address/data, sending an ACK), this interrupt is generated before the ACK cycle so that software may define the outgoing ACK value. If hardware acknowledgment is enabled, these interrupts are always generated after the ACK cycle. See Section 21.5 for more details on transmission sequences.

Interrupts are also generated to indicate the beginning of a transfer when a master (START generated), or the end of a transfer when a slave (STOP detected). Software should read the SMBnCN (SMBus Control register) to find the cause of the SMBus interrupt. The SMBnCN register is described in Section 21.4.3; Table 21.5 provides a quick SMBnCN decoding reference.

21.4.1. SMBus Configuration Register

The SMBus Configuration register (SMBnCF) is used to enable the SMBus Master and/or Slave modes, select the SMBus clock source, and select the SMBus timing and timeout options. When the ENSMB bit is set, the SMBus is enabled for all master and slave events. Slave events may be disabled by setting the INH bit. With slave events inhibited, the SMBus interface will still monitor the SCL and SDA pins; however, the interface will NACK all received addresses and will not generate any slave interrupts. When the INH bit is set, all slave events will be inhibited following the next START (interrupts will continue for the duration of the current transfer).

SFR Definition 21.11. SMB1DAT: SMBus Data

Bit	7	6	5	4	3	2	1	0
Name	SMB1DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC2; SFR Page = F

Bit	Name	Function
7:0	SMB1DAT[7:0]	**SMBus1 Data.** The SMB1DAT register contains a byte of data to be transmitted on the SMBus1 serial interface or a byte that has just been received on the SMBus1 serial interface. The CPU can read from or write to this register whenever the SI1 serial interrupt flag (SMB1CN.0) is set to logic 1. The serial data in the register remains stable as long as the SI1 flag is set. When the SI1 flag is not set, the system may be in the process of shifting data in/out and the CPU should not attempt to access this register.

22.3. Multiprocessor Communications

9-Bit UART mode supports multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0.

Setting the MCE0 bit (SCON0.5) of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the ninth bit is logic 1 (RB80 = 1) signifying an address byte has been received. In the UART interrupt handler, software will compare the received address with the slave's own assigned 8-bit address. If the addresses match, the slave will clear its MCE0 bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their MCE0 bits set and do not generate interrupts on the reception of the following data bytes, thereby ignoring the data. Once the entire message is received, the addressed slave resets its MCE0 bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).

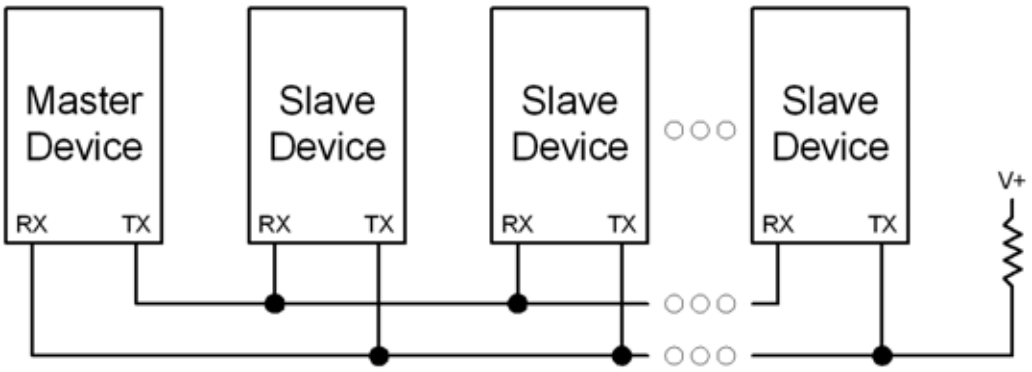


Figure 22.6. UART Multi-Processor Mode Interconnect Diagram

SFR Definition 23.4. SBCON1: UART1 Baud Rate Generator Control

Bit	7	6	5	4	3	2	1	0
Name		SB1RUN					SB1PS[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xAC; SFR Page = All Pages

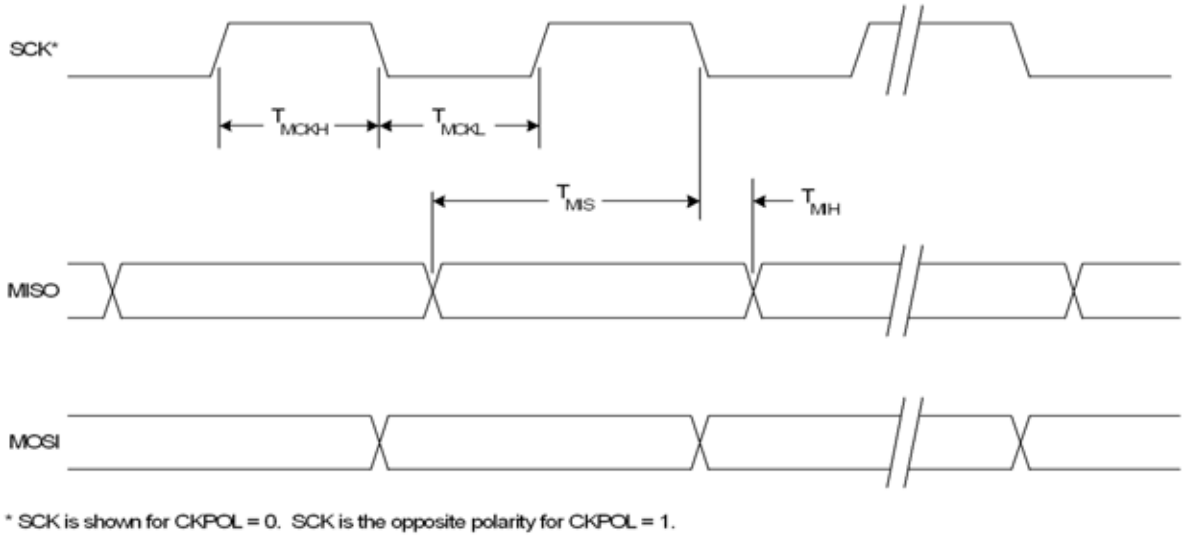
Bit	Name	Function
7	Reserved	Read = 0b. Must Write 0b.
6	SB1RUN	**Baud Rate Generator Enable.** 0: Baud Rate Generator is disabled. UART1 will not function. 1: Baud Rate Generator is enabled.
5:2	Reserved	Read = 0000b. Must Write 0000b.
1:0	SB1PS[1:0]	**Baud Rate Prescaler Select.** 00: Prescaler = 12 01: Prescaler = 4 10: Prescaler = 48 11: Prescaler = 1

SFR Definition 23.5. SBRLH1: UART1 Baud Rate Generator High Byte

Bit	7	6	5	4	3	2	1	0
Name	SBRLH1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

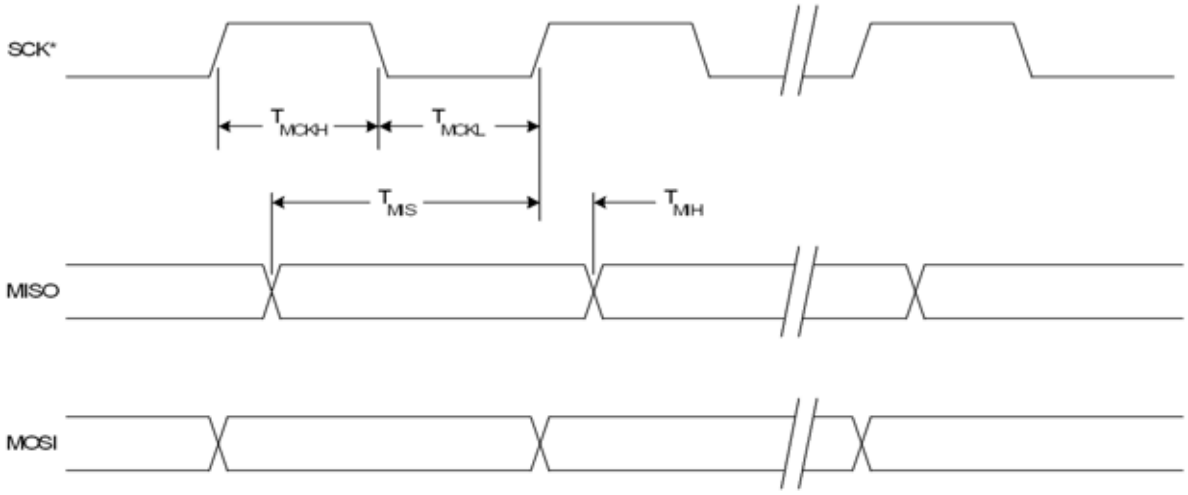
SFR Address = 0xB5; SFR Page = All Pages

Bit	Name	Function
7:0	SBRLH1[7:0]	**UART1 Baud Rate Reload High Bits.** High Byte of reload value for UART1 Baud Rate Generator.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 24.8. SPI Master Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 24.9. SPI Master Timing (CKPHA = 1)

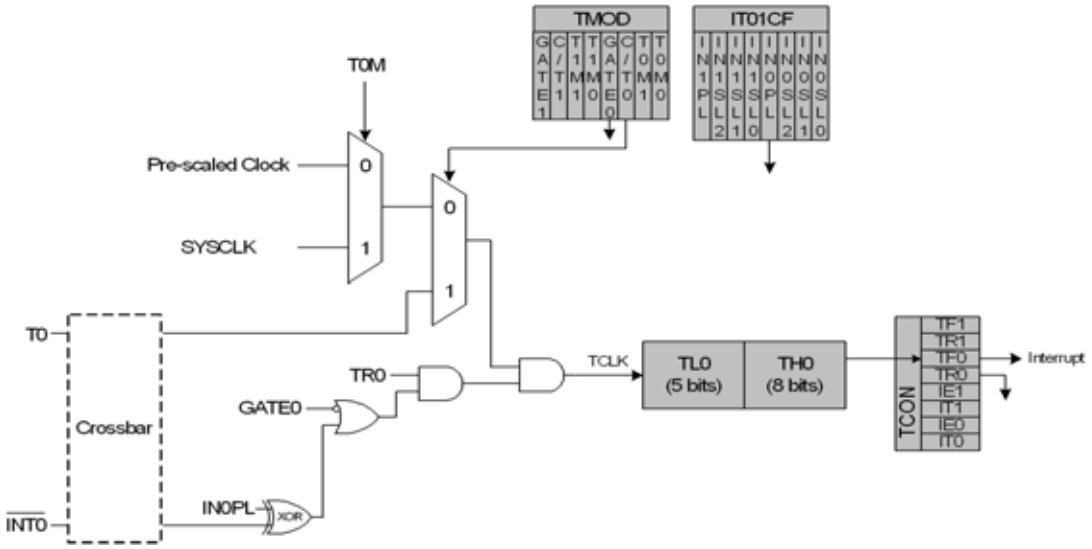


Figure 25.1. T0 Mode 0 Block Diagram

25.1.2. Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

25.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timer 0 and Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from all ones to 0x00, the timer overflow flag TF0 in the TCON register is set and the counter in TL0 is reloaded from TH0. If Timer 0 interrupts are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0.

Both counter/timers are enabled and configured in Mode 2 in the same manner as Mode 0. Setting the TR0 bit (TCON.4) enables the timer when either GATE0 in the TMOD register is logic 0 or when the input signal $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 16.7 for details on the external input signals $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$).

SFR Definition 25.28. TMR5H Timer 5 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR5H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCD; SFR Page = F

Bit	Name	Function
7:0	TMR5H[7:0]	**Timer 5 High Byte.** In 16-bit mode, the TMR5H register contains the high byte of the 16-bit Timer 5. In 8-bit mode, TMR5H contains the 8-bit high byte timer value.

26. Programmable Counter Array

The Programmable Counter Array (PCA0) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. The PCA consists of a dedicated 16-bit counter/timer and five 16-bit capture/compare modules. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the Crossbar to Port I/O when enabled. The counter/timer is driven by a programmable timebase that can select between six sources: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, Timer 0 overflows, or an external clock signal on the ECI input pin. Each capture/compare module may be configured to operate independently in one of six modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8-Bit PWM, or 16-Bit PWM (each mode is described in Section “26.3. Capture/Compare Modules” on page 262). The external oscillator clock option is ideal for real-time clock (RTC) functionality, allowing the PCA to be clocked by a precision external oscillator while the internal oscillator drives the system clock. The PCA is configured and controlled through the system controller's Special Function Registers. The PCA block diagram is shown in Figure 26.1

Important Note: The PCA Module 4 may be used as a watchdog timer (WDT), and is enabled in this mode following a system reset. **Access to certain PCA registers is restricted while WDT mode is enabled**. See Section 26.4 for details.

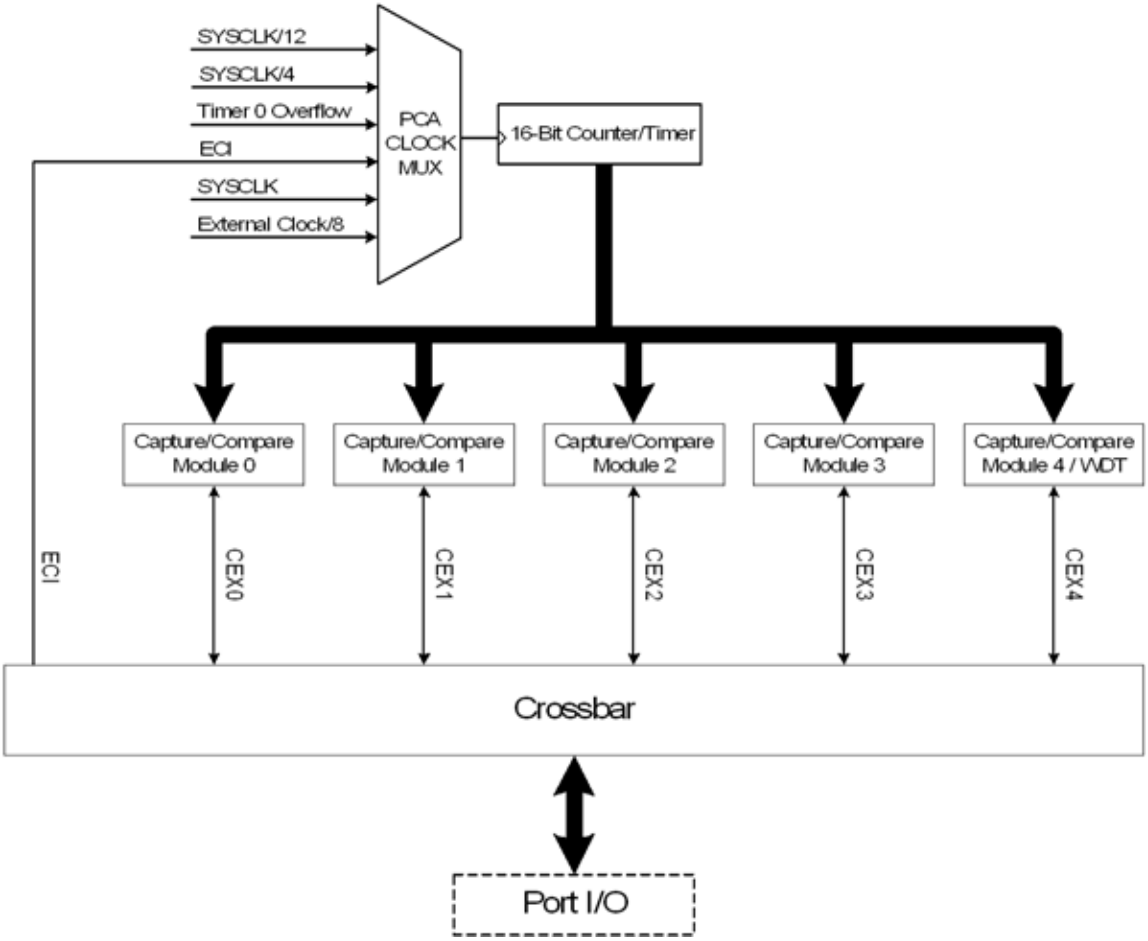


Figure 26.1. PCA Block Diagram