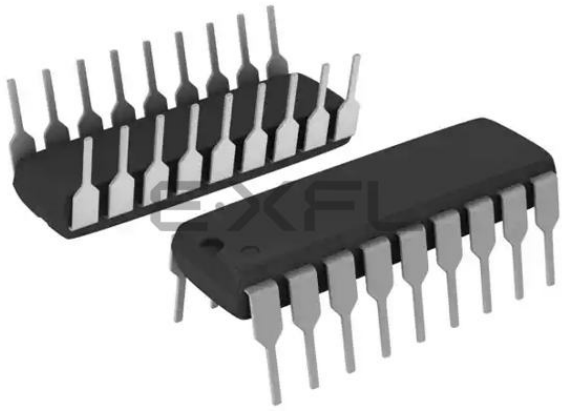

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	60 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0308psc

PIN DESCRIPTION

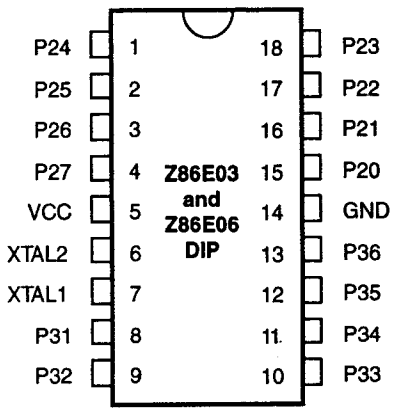


Figure 2. 18-Pin DIP Pin Configuration

Table 1. 18-Pin DIP and SOIC Pin Identification

No	Symbol	Function	Direction
1-4	P24-27	Port 2, pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-33	Port 3, pins 1, 2, 3	Fixed Input
11-13	P34-36	Port 3, pins 4, 5, 6	Fixed Output
14	GND	Ground	
15-18	P20-23	Port 2, pins 0, 1, 2, 3	In/Output

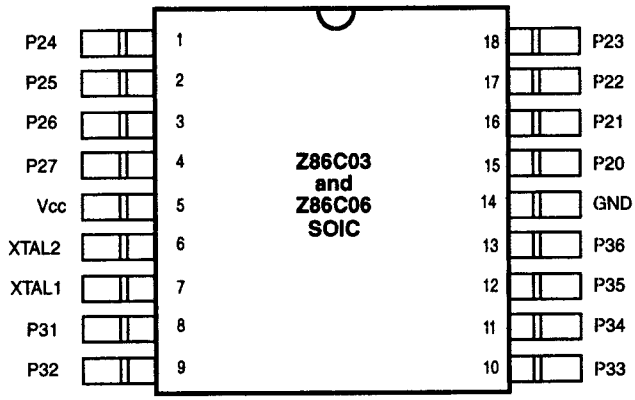


Figure 3. 18-Pin SOIC Pin Configuration

PIN FUNCTIONS

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered and contain Auto Latches. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 4a., 4b., and 4c.). Low EMI output buffers can be globally programmed by the software. In addition, when the SPI is enabled, P20 functions as data-in (DI), and P27 functions as data-out (DO) for the SPI (SPI on the Z86E06 only).

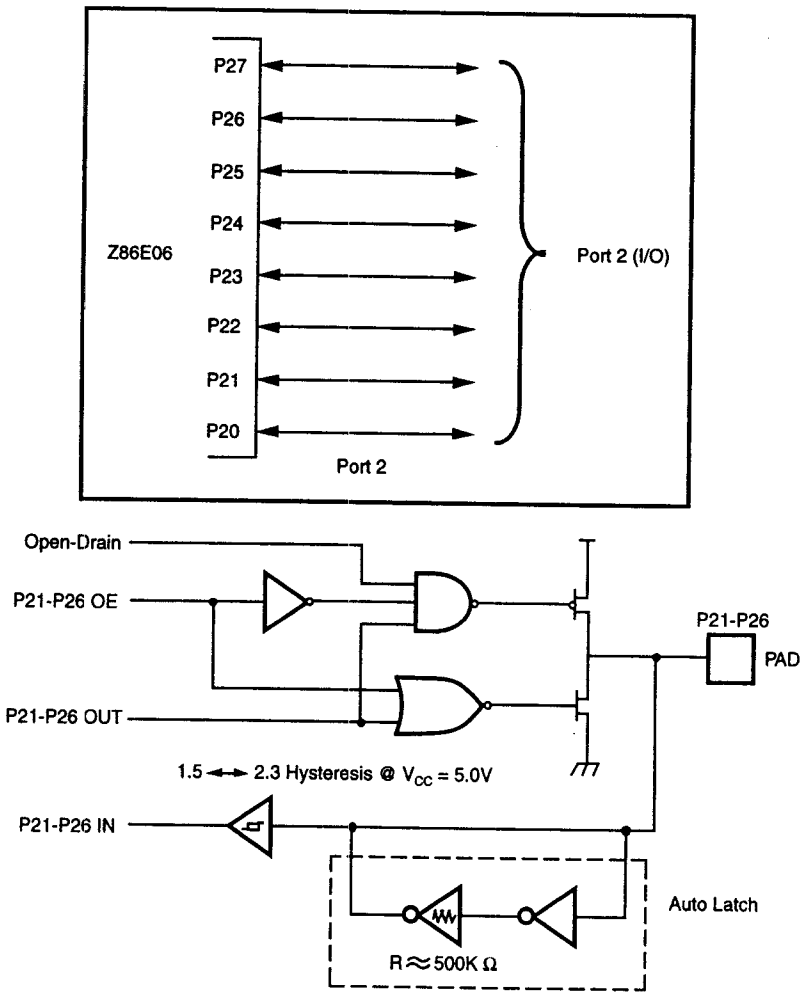


Figure 4a. Port 2 Configuration (Z86E06)

PS021001-0603

FUNCTIONAL DESCRIPTION (Continued)

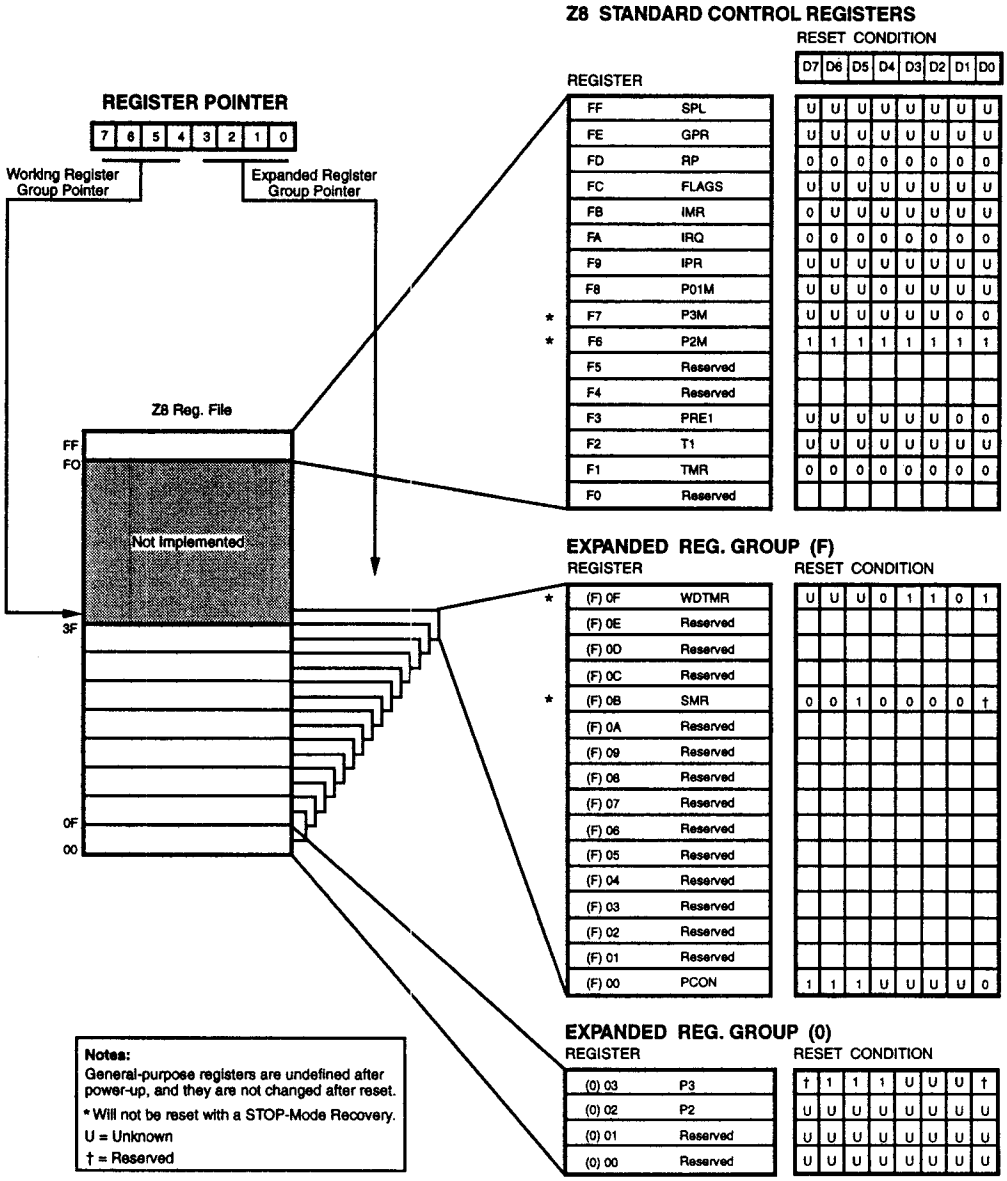


Figure 7a. Expanded Register File Architecture (Z86E03)

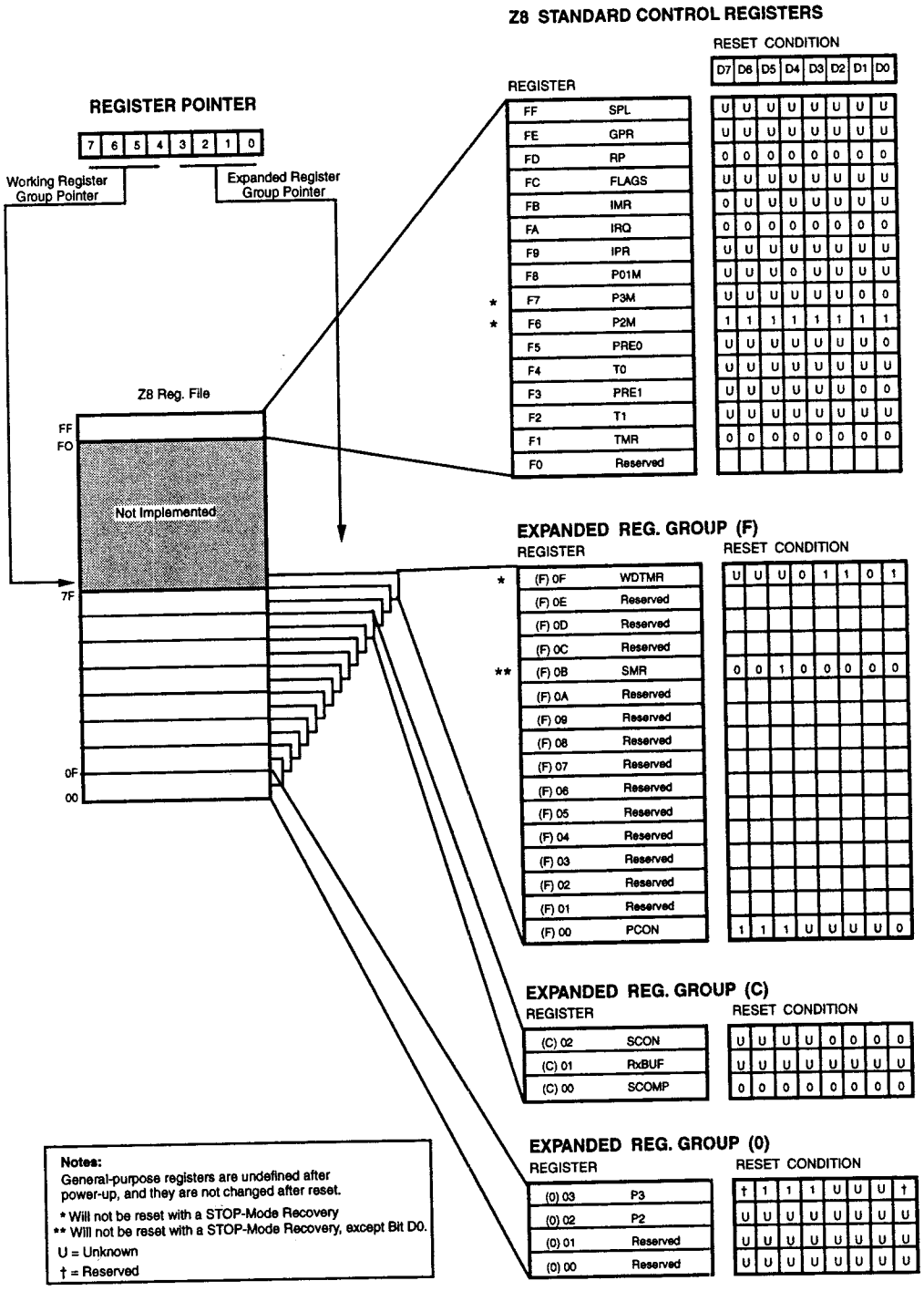
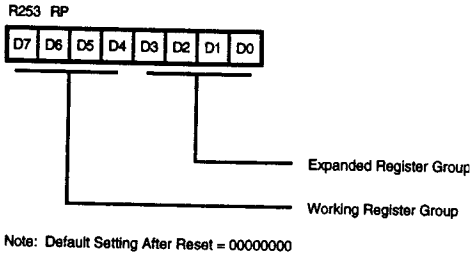


Figure 7b. Expanded Register File Architecture (Z86E06)

FUNCTIONAL DESCRIPTION (Continued)



Note: Default Setting After Reset = 00000000

Figure 8. Register Pointer Register

Register File. The Register File consists of two I/O port registers, 60/124 general-purpose registers, and 13/15 control and status registers. The Z86E03 General-Purpose Register file ranges from address 00 to 3F while the Z86E06 General-Purpose Register file ranges from address 00 to 7F (see Figure 9). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 9). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

Stack. An 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60/124 general-purpose registers.

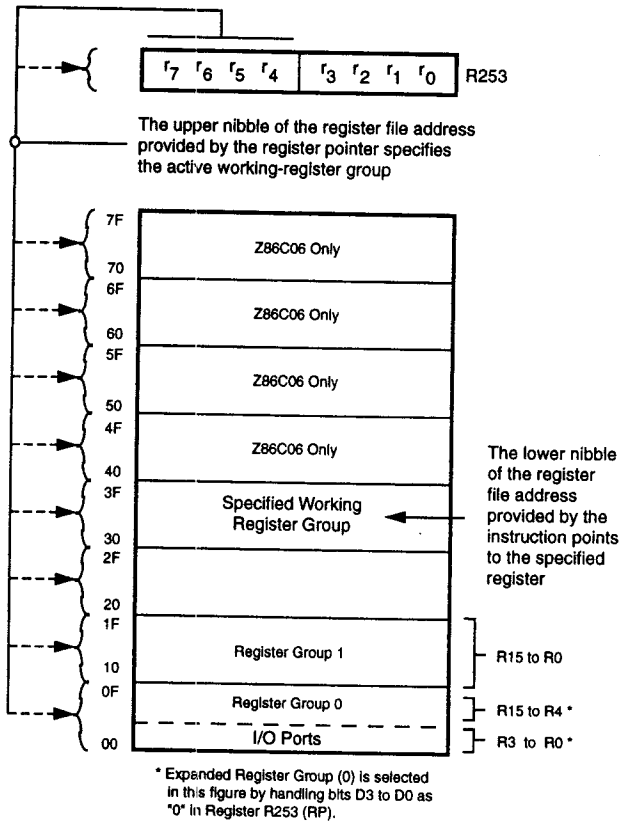


Figure 9. Register Pointer

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	IRQ 0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ 1	IRQ 1	2, 3	External (P33), Falling Edge Triggered
IRQ 2	IRQ 2, T_{IN}	4,5	External (P31), Rising/Falling Edge Triggered
IRQ 3	IRQ 3	6, 7	Software Generated, SPI Receive
IRQ 4	T0/IRQ 4	8, 9	Internal for E06 and Software Generated for E03
IRQ 5	TI	10, 11	Internal

Note:
When enabled, the SPI receive interrupt is mapped to IRQ3 in the Z86E06.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E03/E06 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service. In the Z86E06, when the SPI is disabled, IRQ3 has no hardware source but can be invoked by software (write to IRQ3 Register). When the SPI is enabled, an interrupt will be mapped to IRQ3 after a byte of data has been received by the SPI Shift Register.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

The programming bits for the INTERRUPT EDGE SELECT are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

Table 3. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

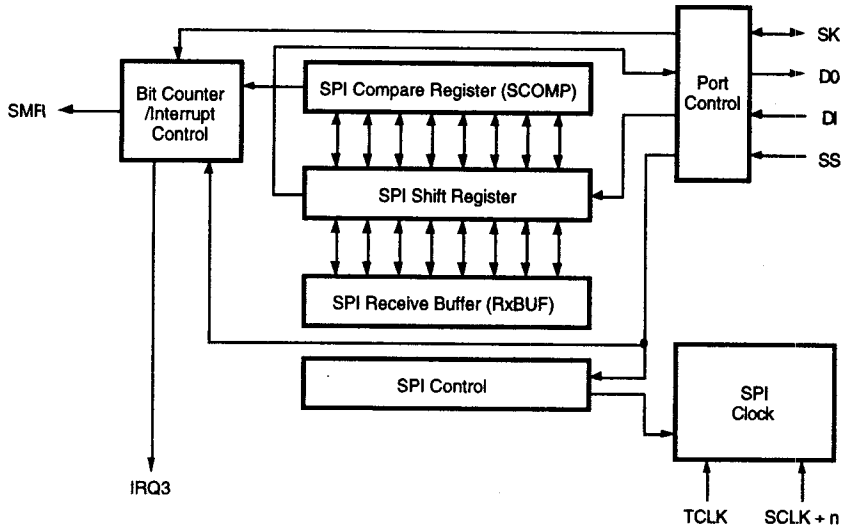


Figure 16. SPI Logic (Z86E06 Only)

PORT Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 17).

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34, and P35 and a 0 releases the Port to its standard I/O configuration.

Bits D4-D1. These bits are reserved and must be 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting D5=1. The default value is 1.

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting D6=1. The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive, it does not affect the relationship of SCLK and XTAL.

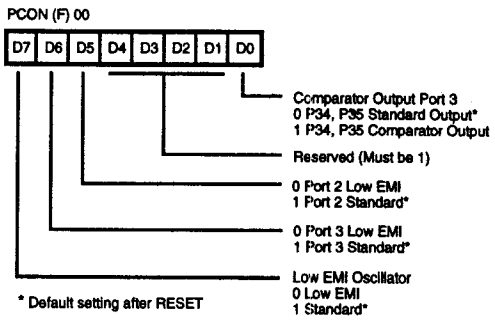


Figure 17. Port Configuration Register (PCON) (Write Only)

STOP-Mode Recovery Source (D2,D3,D4). These three bits of the SMR specify the wake-up source of the STOP-Mode Recovery (Figure 19 and Table 5).

Table 5. STOP-Mode Recovery Source

SMR D4	SMR D3	SMR D2	Operation Description of Action
0	0	0	POR recovery only
0	0	1	POR recovery only (E03 = Reserved)
0	1	0	P31 transition (E03 = Reserved)
0	1	1	P32 transition (E03 = Reserved)
1	0	0	P33 transition (E03 = Reserved)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0:3
1	1	1	Logical NOR of Port 2 bits 0:7

P31-P33 cannot wake up from STOP Mode if the input lines are configured as analog inputs. In the Z86E06, when the SPI is enabled and the Compare feature is active, a SMR is generated upon a comparison in the SPI Shift Register and SCOMP Register, regardless of the above SMR Register settings. If SPI Compare is used to wake up the part from STOP Mode, it is still possible to have one of the other STOP-Mode Recovery sources active. **Note:** These other STOP- Mode Recovery sources must be active level Low (bit D6 in SMR set to 0 if P31, P32, P33, and P27 selected, or bit D6 in SMR set to 1 if logical NOR of Port 2 is selected).

STOP-Mode Recovery Delay Select (D5). This bit disables the 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the "fast" wake up is selected, the STOP-Mode Recovery source needs to be kept active for at least 5 TpC.

STOP-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 19).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. It is active High, and is 0 (cold) on POR/WDT RESET. This bit is Read Only. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

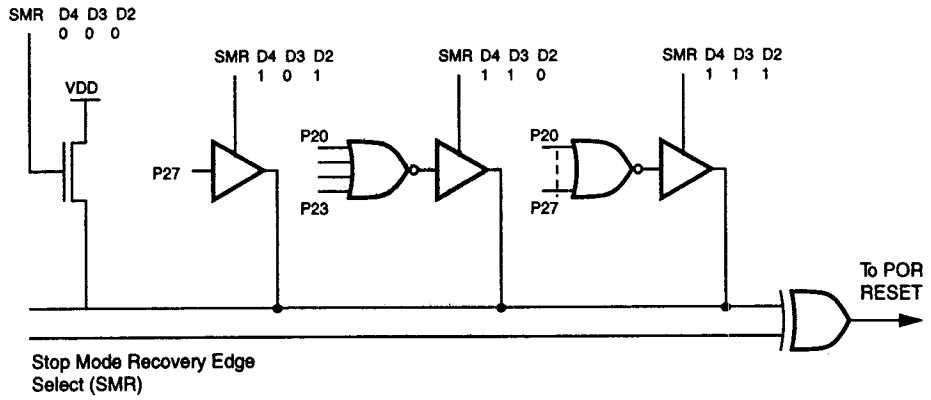


Figure 19a. STOP Mode Recovery Source (Z86E03)

Internal Address Counter. The address of Z86E03/E06 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the high level of pin P00 (Clear) will reset the address to zero. Figure 16 shows the setup time of the serial address input.

Programming Waveform. Figures 24, 25 and 26 show the programming waveforms of each mode. Table 7 shows the timing of programming waveforms.

Programming Algorithm. Figure 27 shows the flow chart of the Z86E03/E06 programming algorithm.

Table 8. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OL3}	P36	5.0V		1.0		1.0		V	I_{OL} = 24 mA	
I_{CC1}	Standby Current	3.3V		3.0		3.0	1.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4, 5,12]
		5.0V		5		5	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4, 5,12]
		3.3V		4.5		4.5	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5,13]
		5.0V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5,13]
		3.3V		1.4		1.4	0.7	mA	Clock Divide-by-16 @ 8 MHz	[4, 5,12]
		5.0V		3.5		3.5	2.0	mA	Clock Divide-by-16 @ 8 MHz	[4, 5,12]
		3.3V		2.0		2.0	1.0	mA	Clock Divide-by-16 @ 12 MHz	[4, 5,13]
		5.0V		4.5		4.5	2.5	mA	Clock Divide-by-16 @ 12 MHz	[4, 5,13]
		5.0V		1.0		1.0		mA	HALT Mode @ 12 kHz	[4,5,11,13]
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6, 9]
		5.0V		10		20	3.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6, 9]
		3.3V		600		600	400	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6, 9,12]
		5.0V		1000		1000	800	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6, 9,12]
I_{ALL}	Auto Latch Low Current	3.3V		7.0		14.0	4.0	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		20.0		30.0	10	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.3V		−4.0		−8.0	−2.0	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		−9.0		−16.0	−5.0	µA	$0V < V_{IN} < V_{CC}$	
T_{POR}	Power-On Reset	3.3V	7	24	6	25	13	ms		
		5.0V	3	13	2	14	7	ms		
V_{LV}	V_{CC} Low Voltage Protection Voltage		2.2	2.8	1.7	3.0	2.6	V	6 MHz max Int. CLK Freq.	[3]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven on XTAL	0.3	5.0	mA	8 MHz
Crystal or Ceramic Resonator	3.0	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND

[3] V_{CC} = 3.0V to 5.5V. The V_{LV} increases as the temperature decreases. Typical values measured at 3.3V and 5.0V.

[4] All outputs unloaded, I/O pins floating, inputs at rail.

[5] $C_{L1} = C_{L2}$ = 100 pF

[6] Same as note [4] except inputs at V_{CC}.

[7] For analog comparator inputs when analog comparators are enabled.

[8] Excludes clock pins.

[9] Clock must be forced Low when XTAL1 is clock-driven and XTAL2 is floating.

[10] STD mode (not low EMI mode).

[11] Low EMI Oscillator enabled.

[12] Z86E03 only.

[13] Z86E06 only.

AC ELECTRICAL CHARACTERISTICS
Z86E03/E06

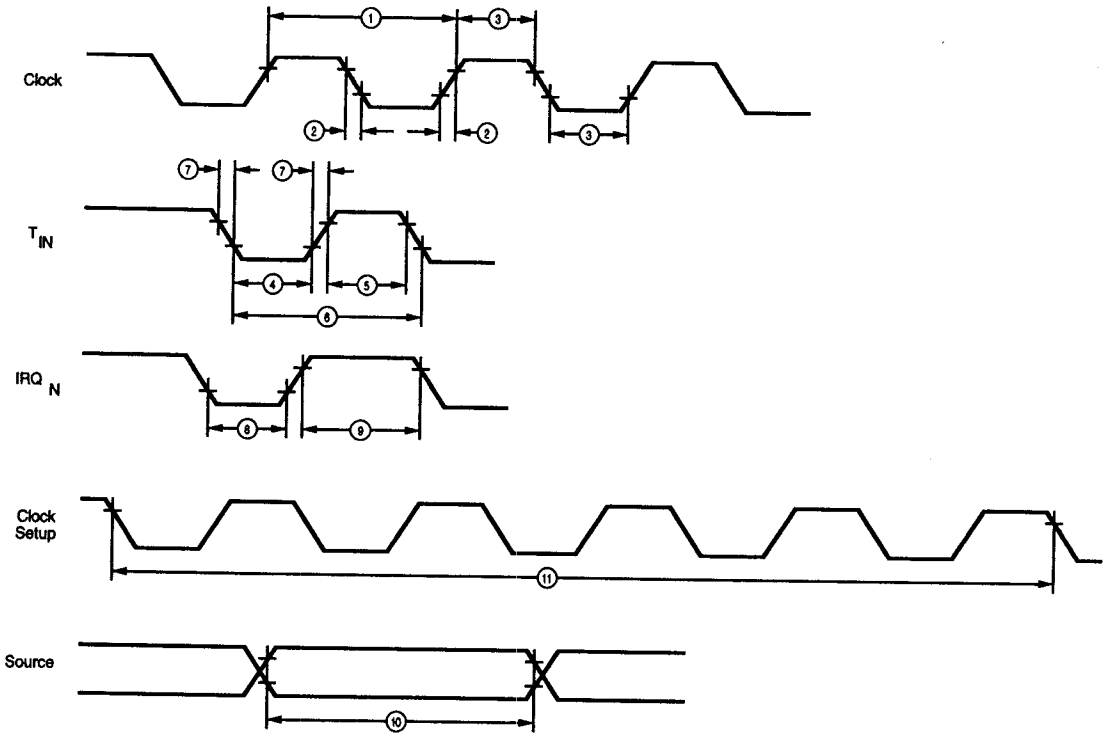


Figure 29. Additional Timing

AC ELECTRICAL CHARACTERISTICS
(SCLK/TCLK = EXTERNAL/2)

				T_A = 0°C To +70°C				T_A = −40°C To +105°C					
			V_{CC}	8 MHz [11]		12 MHz [11]		8 MHz [11]		12 MHz [11]			
No	Symbol	Parameter	Note[3]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	125	DC	83	DC	ns	[1,7,8]
			5.5V	125	DC	83	DC	125	DC	83	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise	3.0V		25		15		25		15	ns	[1,7,8]
		and Fall Times	5.5V		25		15		25		15	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	62		41		62		41		ns	[1,7,8]
			5.5V	62		41		62		41		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1,7,8]
			5.5V	70		70		70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			[1,7,8]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,7,8]

AC ELECTRICAL CHARACTERISTICS (Continued)
(SCLK/TCLK = EXTERNAL/2)

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C TO +70°C 8 MHz[11] Min	Max	12 MHz[11] Min	Max	T_A = –40°C TO +105°C 8 MHz[11] Min	Max	12 MHz[11] Min	Max	Units	Notes
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			[1,7,8]
			5.5V	8TpC		8TpC		8TpC		8TpC			[1,7,8]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100		100		100	ns	[1,7,8]
			5.5V		100		100		100		100	ns	[1,7,8]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		100		ns	[1,2,7,8]
			5.5V	70		70		70		70		ns	[1,2,7,8]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1,2,7,8]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,2,7,8]
10	Twsm	STOP Mode Recovery Width Spec	3.0V	12		12		12		12			[1,8,10]
			5.5V	12		12		12		12			[1,8,10]
11	Tost	Oscillator Startup Time	3.0V	5TpC		5TpC		5TpC		5TpC		ns	[1,3,4,9]
			5.5V	5TpC		5TpC		5TpC		5TpC		ns	[1,3,4,9]
12	Twdt	Watch-Dog Timer Refresh Time	3.0V	15		15		12		12		ms	D0 = 0 [5,6]
			5.5V	5		5		3		3		ms	D1 = 0 [5,6]
			3.0V	30		30		25		25		ms	D0 = 1 [5,6]
			5.5V	16		16		12		12		ms	D1 = 0 [5,6]
			3.0V	60		60		50		50		ms	D0 = 0 [5,6]
			5.5V	25		25		30		30		ms	D1 = 1 [5,6]
			3.0V	250		250		200		200		ms	D0 = 1 [5,6]
			5.5V	120		120		100		100		ms	D1 = 1 [5,6]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] V_{CC} = 3.0V to 5.5V.
[4] SMR-D5 = 0, POR delay is off.
[5] WDTMR Register
[6] Internal RC Oscillator only.
[7] SMR D1 = 0, SCLK = External/2
[8] Maximum frequency for internal system clock is 4 MHz when using SCLK = EXTERNAL clock mode.
[9] For RC and LC oscillator and for clock-driven oscillator.
[10] SMR-D5 = 1, STOP-Mode Recovery delay is on.
[11] Z86E03 = 8 MHz; Z86E06 = 12 MHz.

EXPANDED REGISTER FILE CONTROL REGISTERS (Continued)

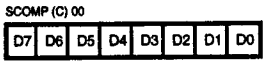


Figure 34. SPI Compare Register (Z86E06 Only)

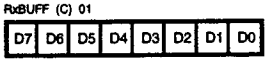


Figure 35. SPI Receive Buffer (Z86E06 Only)

Z8 CONTROL REGISTER DIAGRAMS

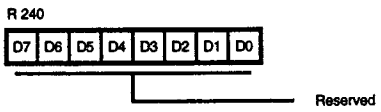


Figure 36. Reserved

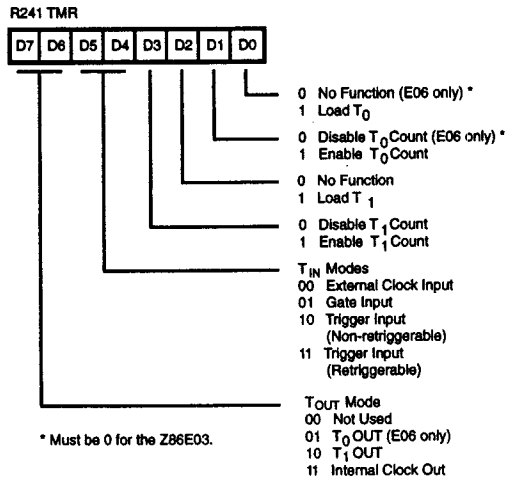


Figure 37. Timer Mode Register ($F1_H$: Read/Write)

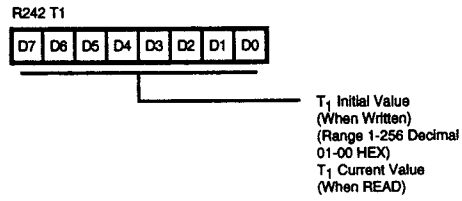


Figure 38. Counter Timer 1 Register ($F2_H$: Read/Write)

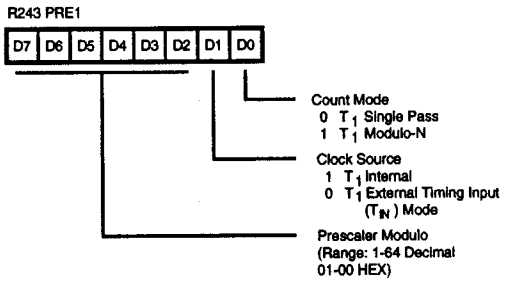


Figure 39. Prescaler 1 Register ($F3_H$: Write Only)

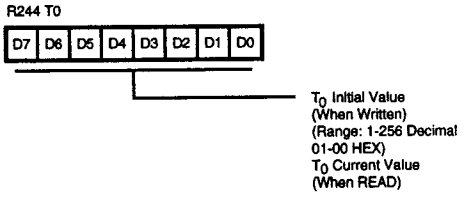


Figure 40. Counter/Timer 0 Register ($F4_H$: Read/Write; Z86E06 Only)

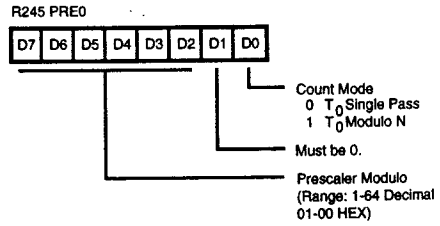


Figure 41. Prescaler 0 Register ($F5_H$: Write Only; Z86E06 Only)

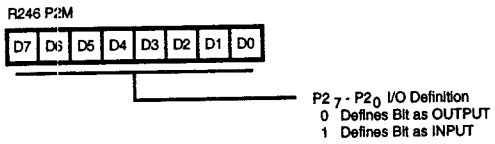


Figure 42. Port 2 Mode Register ($F6_H$: Write Only)

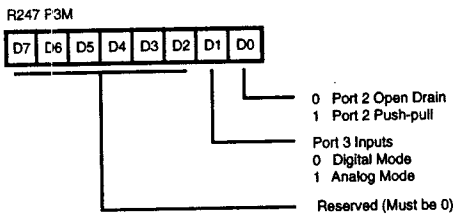


Figure 43. Port 3 Mode Register ($F7_H$: Write Only)

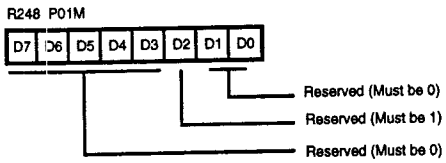


Figure 44. Port 0 and 1 Mode Register ($F8_H$: Write Only)

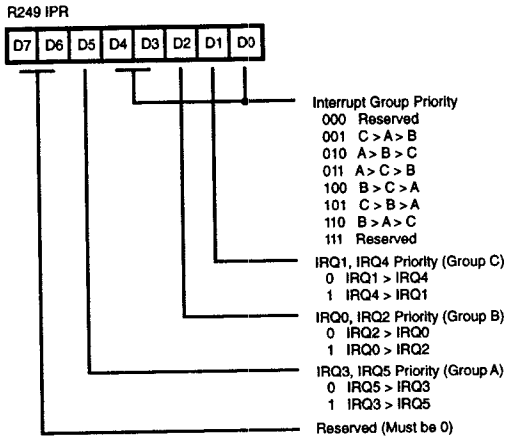


Figure 45. Interrupt Priority Register ($F9_H$: Write Only)

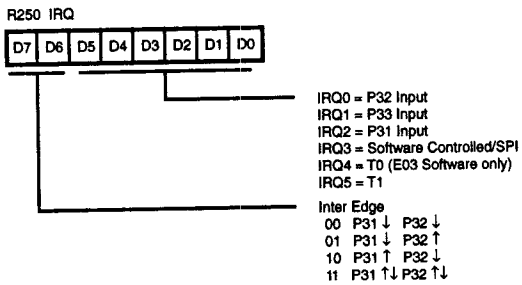


Figure 46. Interrupt Request Register (FA_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

2

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

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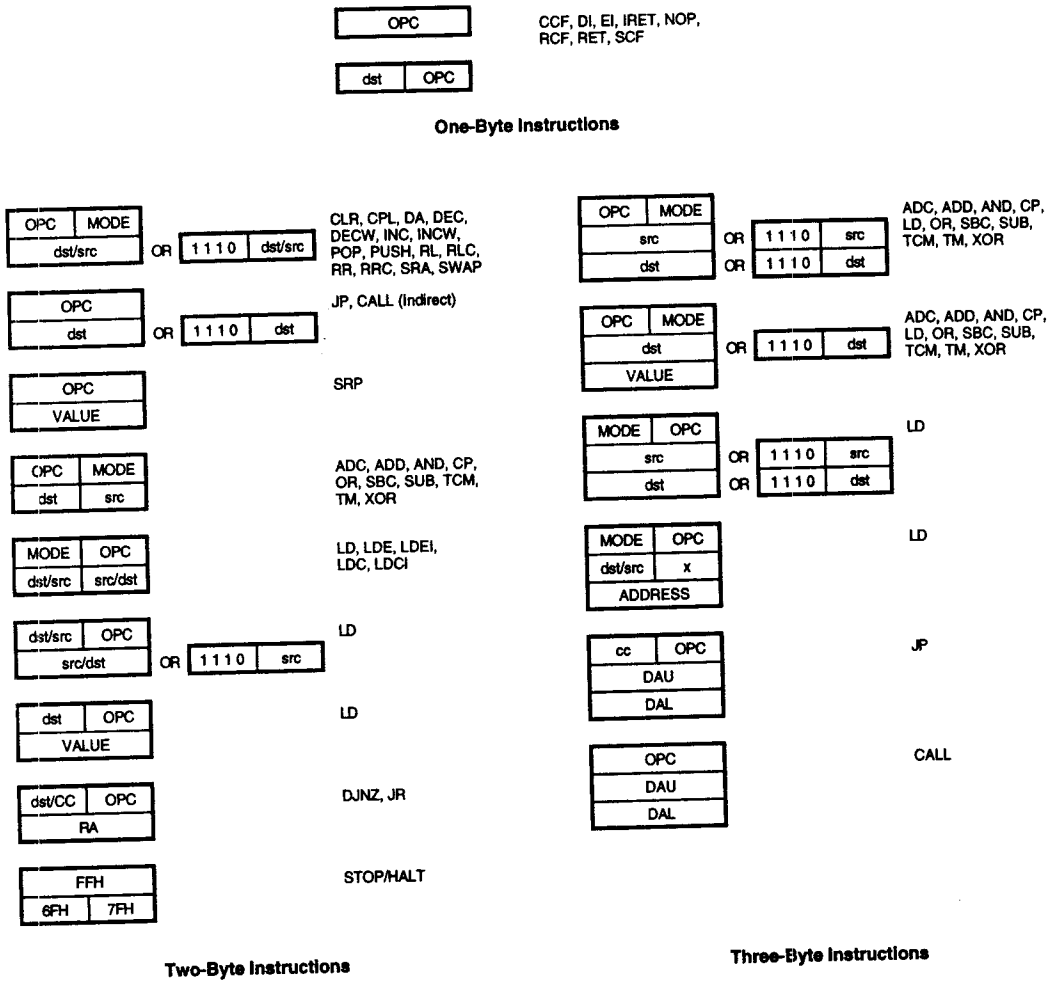
INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

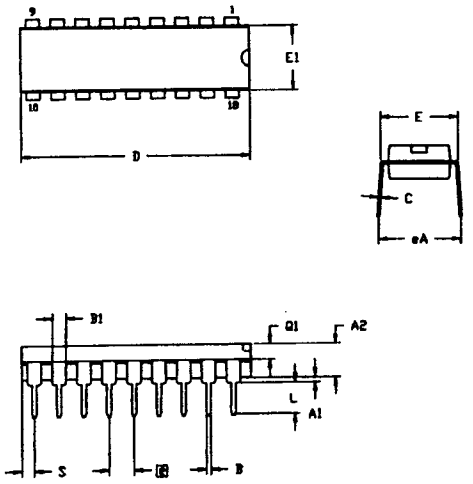
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, 128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r r R R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

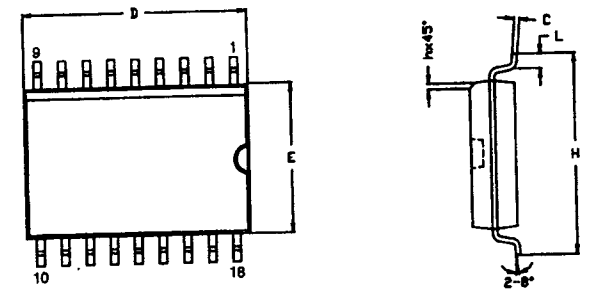
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86E03 (8 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86E0308PSC	Z86E0308SSC	Z86E0308PEC	Z86E0308SEC

Z86E06 (12 MHz)

Standard Temperature		Extended Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86E0612PSC	Z86E0612SSC	Z86E0612PEC	Z86E0612SEC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
S = Plastic SOIC

Preferred Temperature
S = 0°C to +70°C

Longer Lead Time
E = –40°C to +105°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86E03 08 P S C is a Z86E03, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow