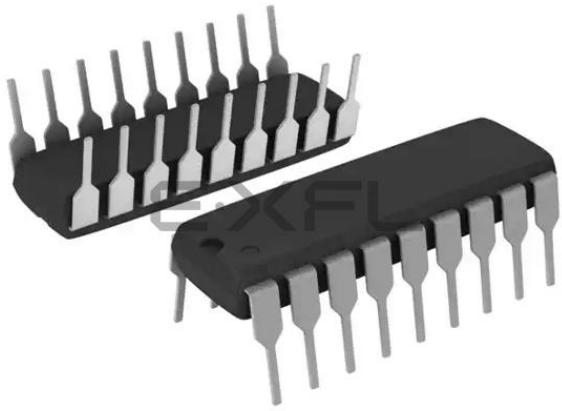


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	60 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0308psg

GENERAL DESCRIPTION (Continued)

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File (Figure 1). The Register File is composed of 60/124 bytes of General-Purpose Registers, two I/O Port registers, and thirteen/fifteen Control and Status registers. The Expanded Register File consists of three control registers in the Z86E03, and four control registers, a SPI Receive Buffer, and a SPI compare register in the Z86E06.

With powerful peripheral features such as on-board comparators, counter/timer(s), Watch-Dog Timer (WDT), and serial peripheral interface (E06 only), the Z86E03/E06 meets the needs of a variety of sophisticated controlle applications.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g. B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

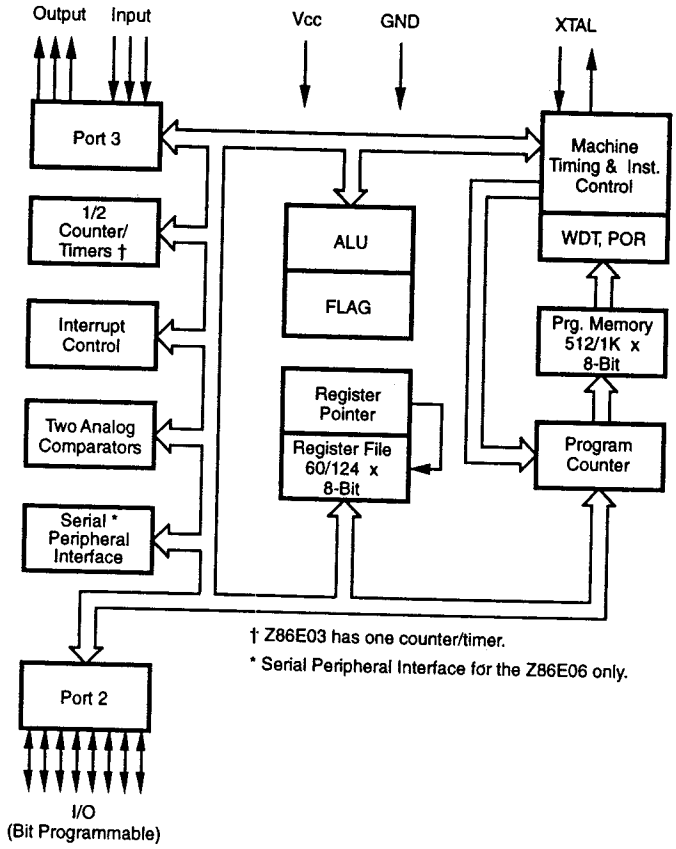


Figure 1. Z86E03/E06 Functional Block Diagram

PIN FUNCTIONS (Continued)

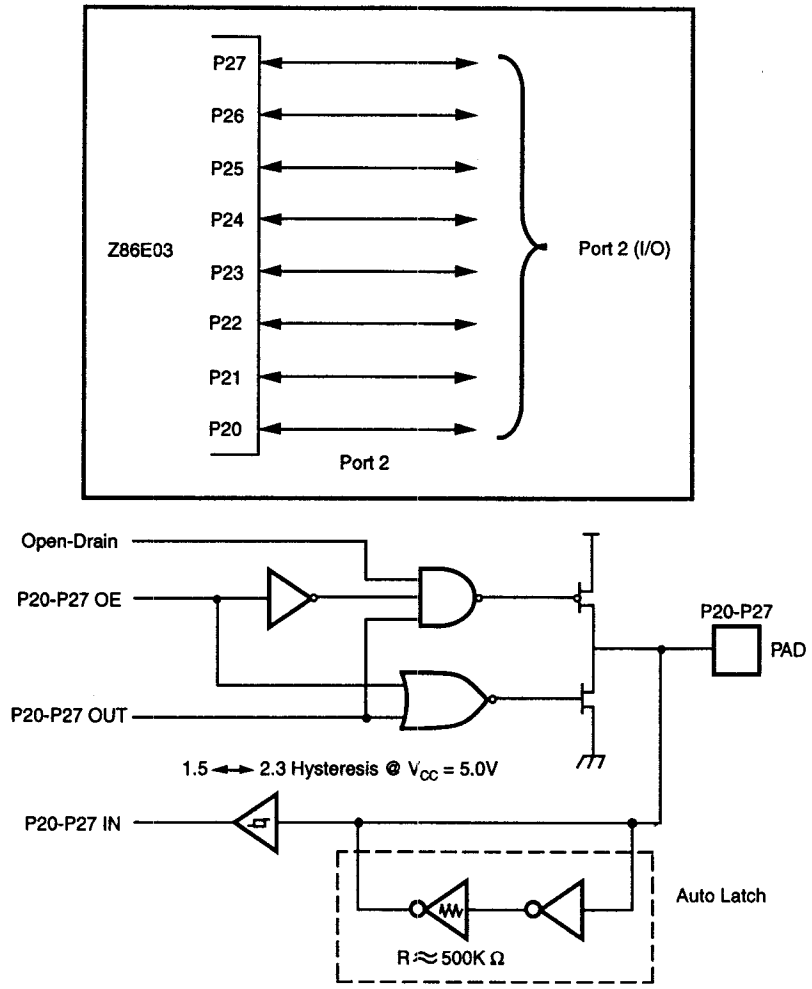


Figure 4c. Port 2 Configuration (Z86E03)

FUNCTIONAL DESCRIPTION (Continued)

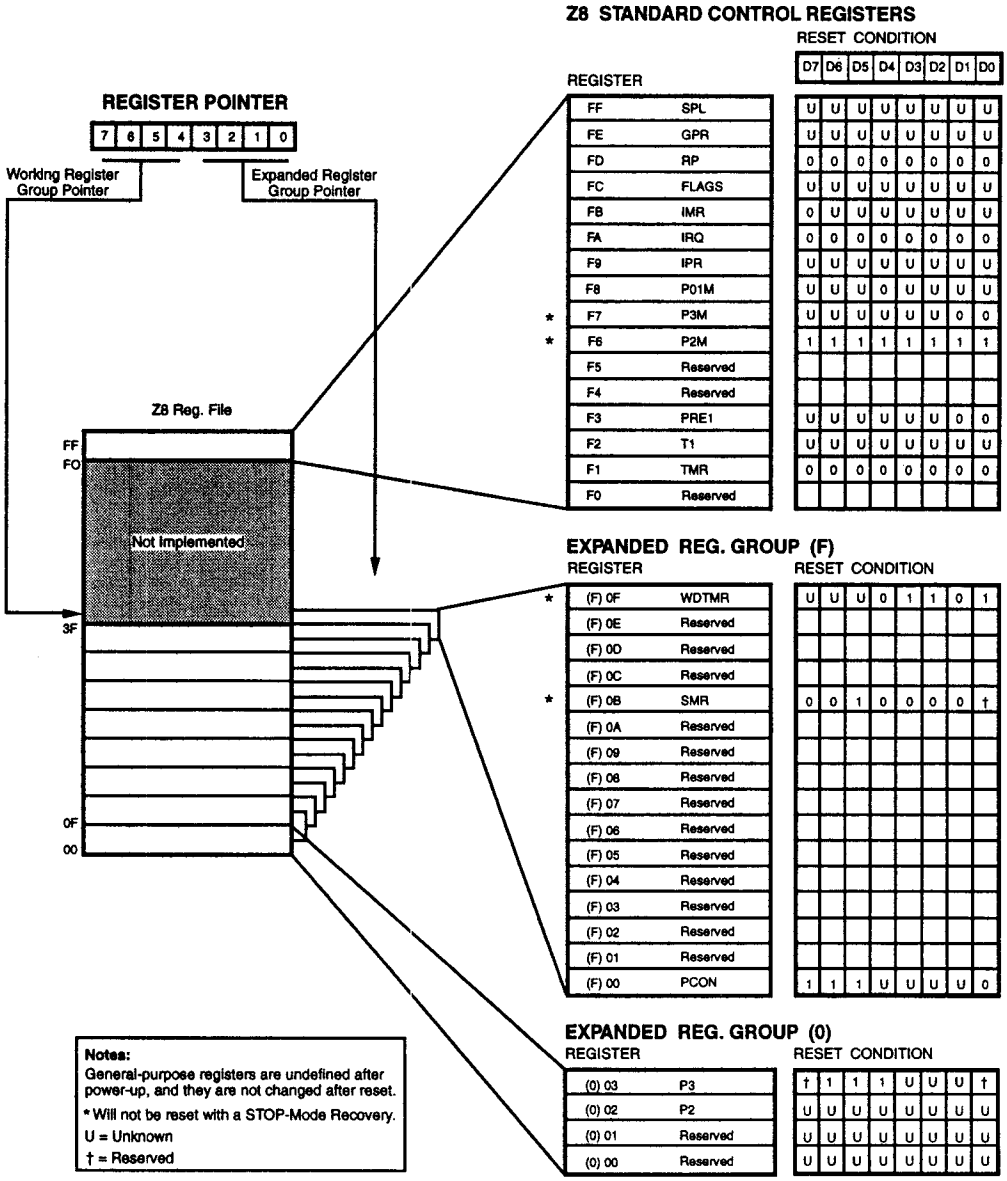


Figure 7a. Expanded Register File Architecture (Z86E03)

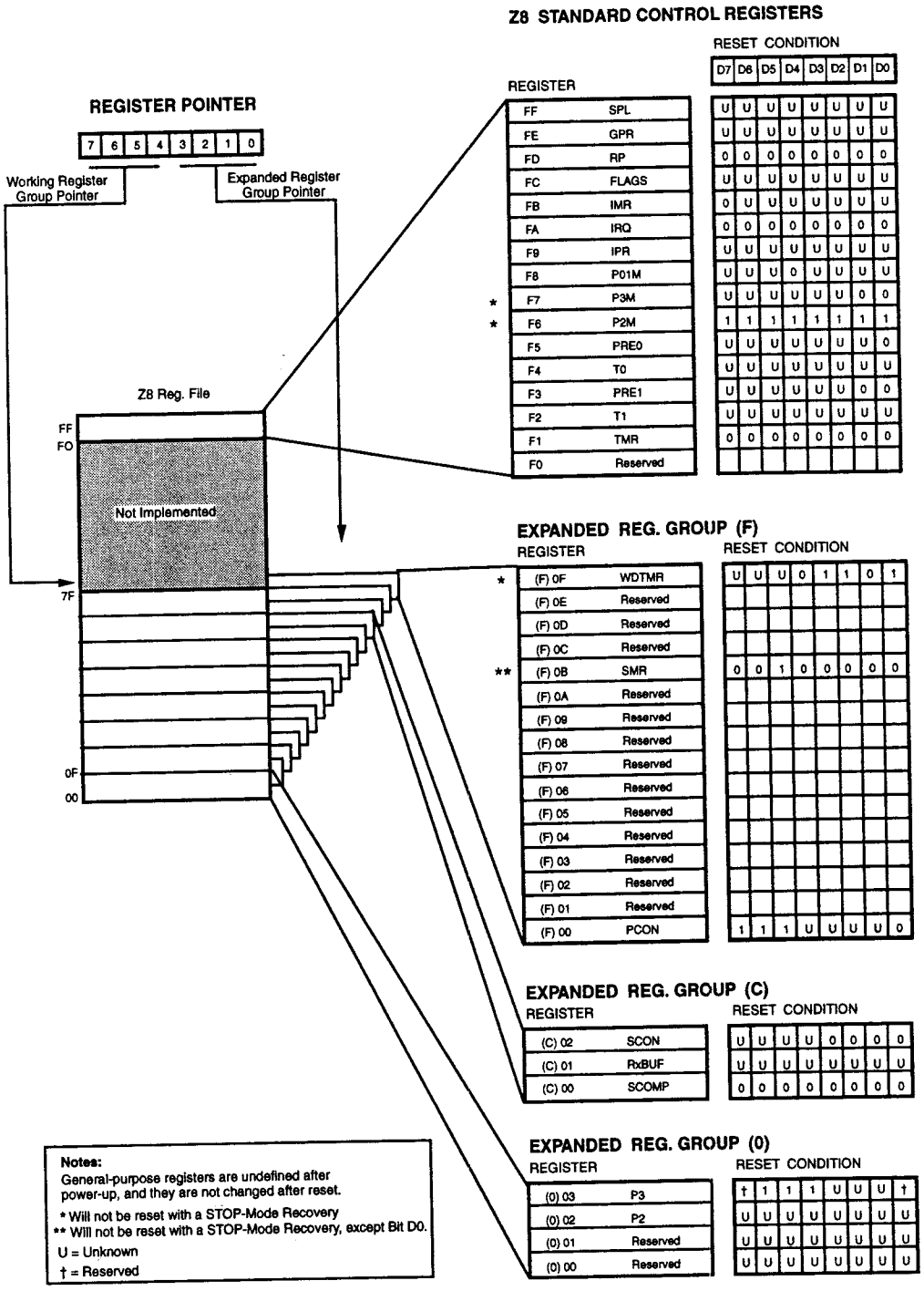
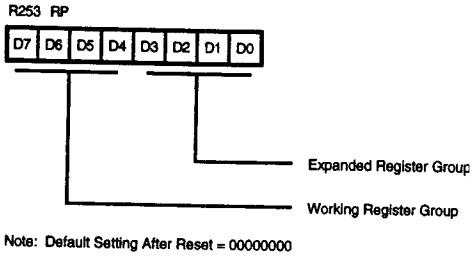


Figure 7b. Expanded Register File Architecture (Z86E06)

FUNCTIONAL DESCRIPTION (Continued)



Note: Default Setting After Reset = 00000000

Figure 8. Register Pointer Register

Register File. The Register File consists of two I/O port registers, 60/124 general-purpose registers, and 13/15 control and status registers. The Z86E03 General-Purpose Register file ranges from address 00 to 3F while the Z86E06 General-Purpose Register file ranges from address 00 to 7F (see Figure 9). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 9). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

Stack. An 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60/124 general-purpose registers.

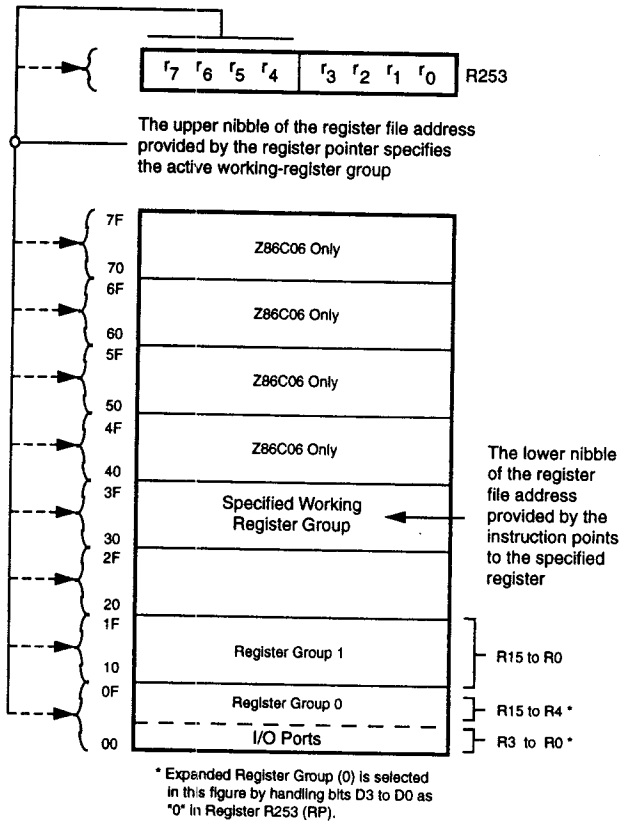


Figure 9. Register Pointer

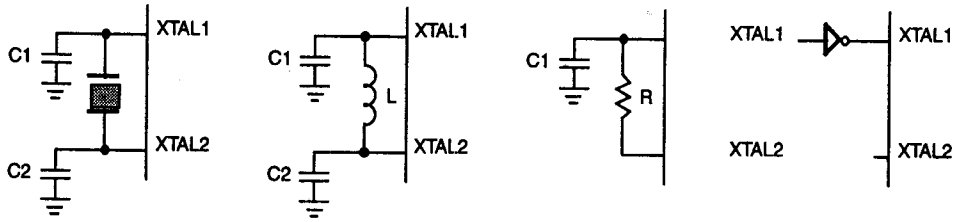
FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86E03/E06 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 8 MHz/12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values (capacitance between 10 pF to 300 pF) from each pin directly to the device ground (pin 14). The layout is important to reduce ground noise injection.

The RC oscillator option is EPROM-programmable, to be selected by the customer at the time the Z8 is EPROM programmed. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 12).

In addition, a special feature has been incorporated into the Z86E03/E06; in low EMI noise mode (bit 7 of PCON register=0) with the RC option selected, the oscillator is targeted to consume considerately less I_{cc} current at frequencies of 10 kHz or less.



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC
C1, C2 = 22 pF
L = 130 µH *
F = 3 MHz

RC
@ 5V Vcc (TYP)
C1 = 33pF*
R = 1kΩ*
F = 9.5 MHz

External Clock

* Preliminary Value Including Pin Parasitics

Figure 12. Oscillator Configuration

Power-On Reset. A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{cc} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the three conditions:

- Power-Fail to Power-OK Status
- STOP-Mode Recovery (If D5 of SMR=1)
- WDT Time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after STOP mode recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. Will turn off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device may be recovered by interrupts either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP mode is terminated by a RESET only, either by WDT time-out, POR, SPI compare; or SMR recovery. This causes the processor to restart the application program at address 000C (HEX). Note, the crystal remains active in STOP mode if bits 3 and 4 of the WDTMR are enabled. In this mode, only the Watch-Dog Timer runs in STOP mode.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, i.e.:

```
FF    NOP   ; clear the pipeline
6F    STOP  ; enter STOP mode
or
FF    NOP   ; clear the pipeline
7F    HALT  ; enter HALT mode
```

Serial Peripheral Interface (SPI)—Z86E06 Only. The Z86E06 incorporates a serial peripheral interface for communication with other microcontrollers and peripherals. **The SPI does not exist on the Z86E03.** The SPI includes features such as STOP-Mode Recovery, Master/Slave selection, and Compare mode. Table 4 contains the pin configuration for the SPI feature when it is enabled. The SPI consists of four registers: SPI Control Register (SCON), SPI Compare Register (SCOMP), SPI Receive/Buffer Register (RxBUF), and SPI Shift Register. SCON is located in bank (C) of the Expanded Register Group at address 02.

Table 4. SPI Pin Configuration

Name	Function	Pin Location
DI	Data-In	P20
DO	Data-Out	P27
SS	Slave Select	P35
SK	SPI Clock	P34

The SPI Control Register (SCON) (Figure 13) is a read/write register that controls; Master/Slave selection, interrupts, clock source and phase selection, and error flag. Bit 0 enables/disables the SPI with the default being SPI disabled. A 1 in this location will enable the SPI, and a 0 will disable the SPI. Bits 1 and 2 of the SCON register in Master mode select the clock rate. The user may choose whether internal clock is divide-by-2, -4, -8, or -16. In slave mode, Bit 1 of this register flags the user if an overrun of the RxBUF Register has occurred. The RxCharOverrun flag is only reset by writing a 0 to this bit. In slave mode, bit 2 of the Control Register disables the data-out I/O function. If a 1 is written to this bit, the data-out pin is released to its original port configuration. If a 0 is written to this bit, the SPI shifts out one bit for each bit received. Bit 3 of the SCON Register enables the compare feature of the SPI, with the default being disabled. When the compare feature is enabled, a comparison of the value in the SCOMP Register is made with the value in the RxBUF Register. Bit 4 signals that a receive character is available in the RxBUF Register.

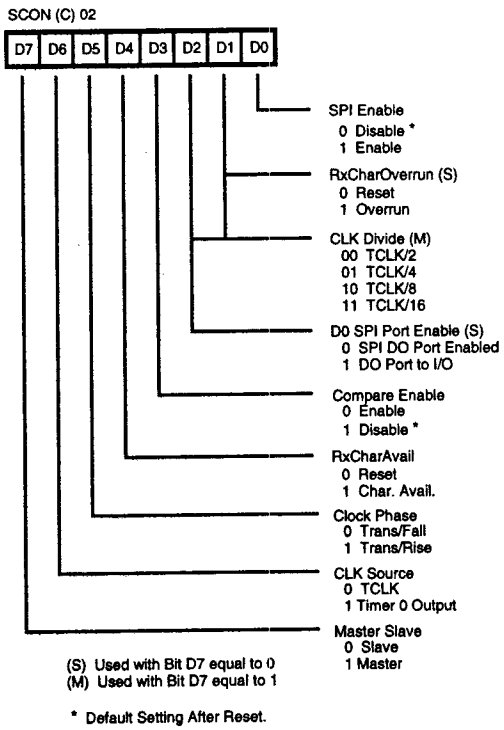


Figure 13. SPI Control Register (SCON) (Z86E06 Only)

If the associated IRQ3 is enabled, an interrupt is generated. Bit 5 controls the clock phase of the SPI. A 1 in Bit 5 allows for receiving data on the clock's falling edge and transmitting data on the clock's rising edge. A 0 allows receiving data on the clock's rising edge and transmitting on the clock's falling edge. The SPI clock source is defined in bit 6. A 1 uses Timer0 output for the SPI clock, and a 0 uses TCLK for clocking the SPI. Finally, bit 7 determines whether the SPI is used as a Master or a Slave. A 1 puts the SPI into Master mode and a 0 puts the SPI into Slave mode.

FUNCTIONAL DESCRIPTION (Continued)

Receive Character Available and Overrun (Z86E06 Only). When a complete data stream is received, an interrupt is generated and the RxCharAvail bit in the SCON Register is set. Bit 4 in the SCON Register is for enabling or disabling the RxCharAvail interrupt. The RxCharAvail bit is available for interrupt polling purposes and is reset when the RxBUF Register is read. RxCharAvail is generated in both master and slave modes. While in slave mode, if the RxBUF is not read before the next data stream is received and loaded into the RxBUF Register, Receive Character Overrun (RxCharOverrun) occurs. Since there is no need for clock control in slave mode, bit D1 in the SPI Contro Register is used to log any RxCharOverrun (Figure 15 and Figure 16).

No	Parameter	Min	Units
1	DI to SK Setup	10	ns
2	SK to D0 Valid	15	ns
3	SS to SK Setup	.5 Tsk	ns
4	SS to D0 Valid	15	ns
5	SK to DI Hold Time	10	ns

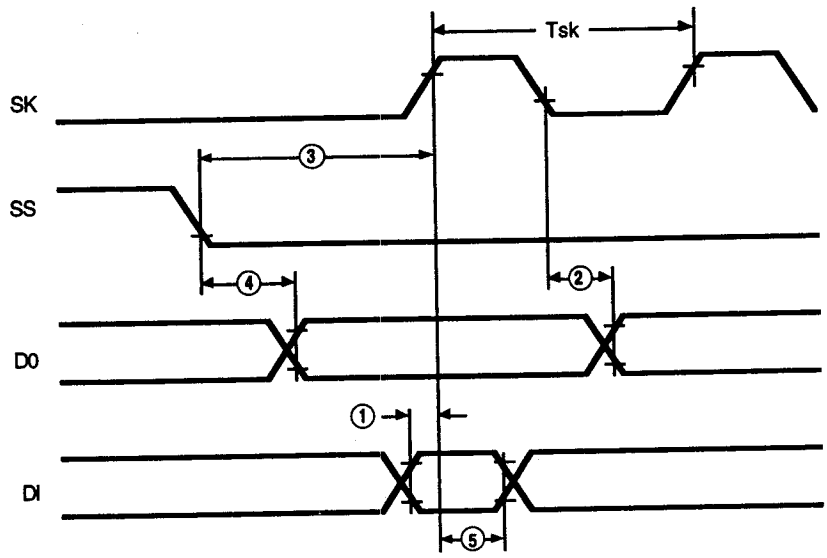


Figure 15. SPI Timing (Z86E06 Only)

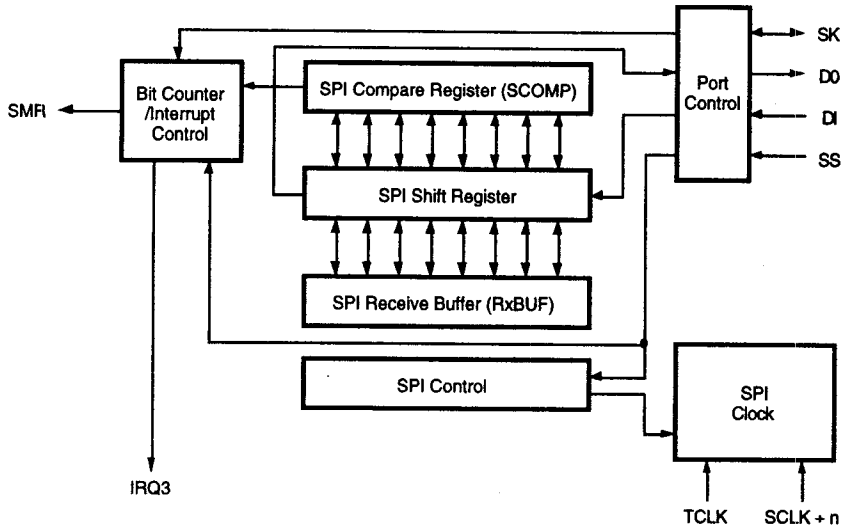


Figure 16. SPI Logic (Z86E06 Only)

PORT Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 17).

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34, and P35 and a 0 releases the Port to its standard I/O configuration.

Bits D4-D1. These bits are reserved and must be 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting D5=1. The default value is 1.

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting D6=1. The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive, it does not affect the relationship of SCLK and XTAL.

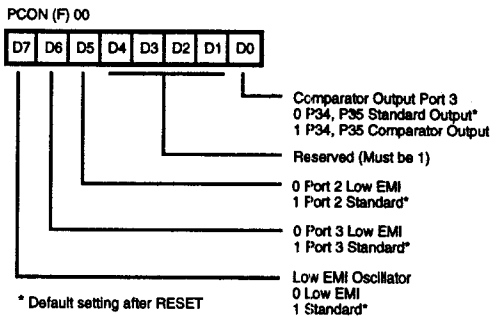


Figure 17. Port Configuration Register (PCON) (Write Only)

STOP-Mode Recovery Source (D2,D3,D4). These three bits of the SMR specify the wake-up source of the STOP-Mode Recovery (Figure 19 and Table 5).

Table 5. STOP-Mode Recovery Source

SMR D4	SMR D3	SMR D2	Operation Description of Action
0	0	0	POR recovery only
0	0	1	POR recovery only (E03 = Reserved)
0	1	0	P31 transition (E03 = Reserved)
0	1	1	P32 transition (E03 = Reserved)
1	0	0	P33 transition (E03 = Reserved)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0:3
1	1	1	Logical NOR of Port 2 bits 0:7

P31-P33 cannot wake up from STOP Mode if the input lines are configured as analog inputs. In the Z86E06, when the SPI is enabled and the Compare feature is active, a SMR is generated upon a comparison in the SPI Shift Register and SCOMP Register, regardless of the above SMR Register settings. If SPI Compare is used to wake up the part from STOP Mode, it is still possible to have one of the other STOP-Mode Recovery sources active. **Note:** These other STOP- Mode Recovery sources must be active level Low (bit D6 in SMR set to 0 if P31, P32, P33, and P27 selected, or bit D6 in SMR set to 1 if logical NOR of Port 2 is selected).

STOP-Mode Recovery Delay Select (D5). This bit disables the 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the "fast" wake up is selected, the STOP-Mode Recovery source needs to be kept active for at least 5 TpC.

STOP-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 19).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. It is active High, and is 0 (cold) on POR/WDT RESET. This bit is Read Only. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

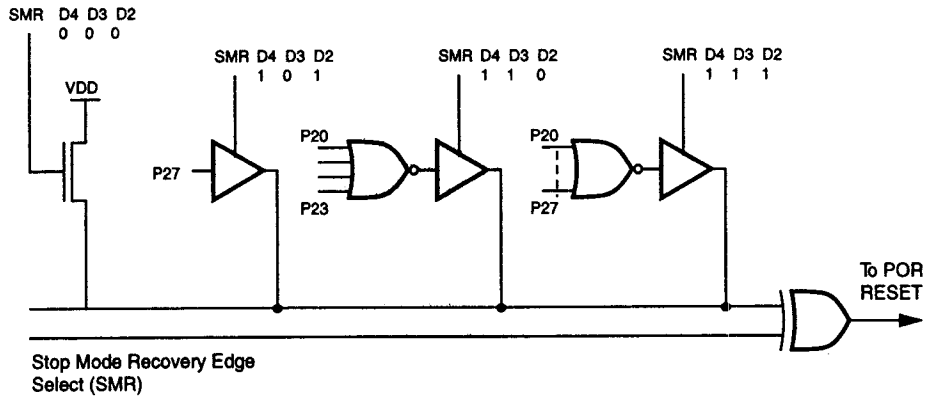
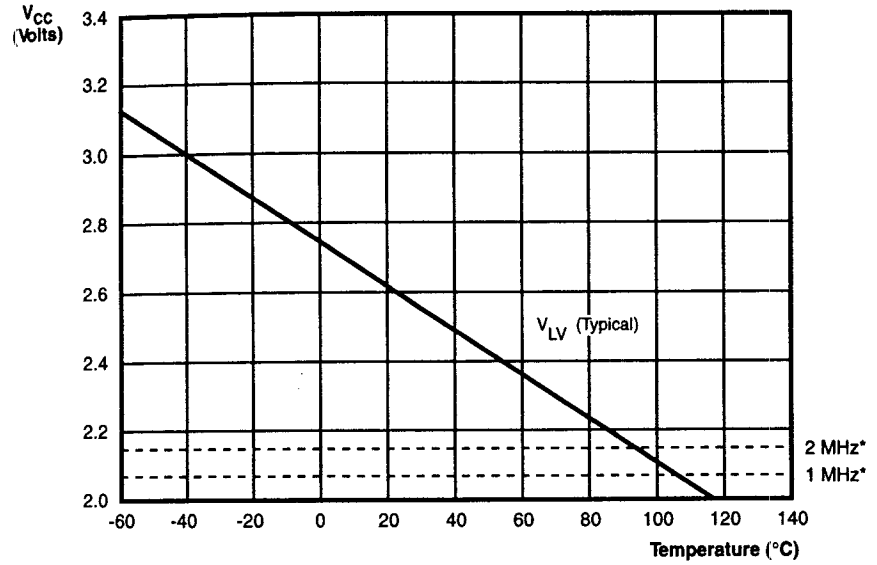


Figure 19a. STOP Mode Recovery Source (Z86E03)



Note: * The typical minimum operating Vcc voltage at that frequency.

Figure 22. Typical Z86E03/E06 V_{LV} Voltage vs Temperature

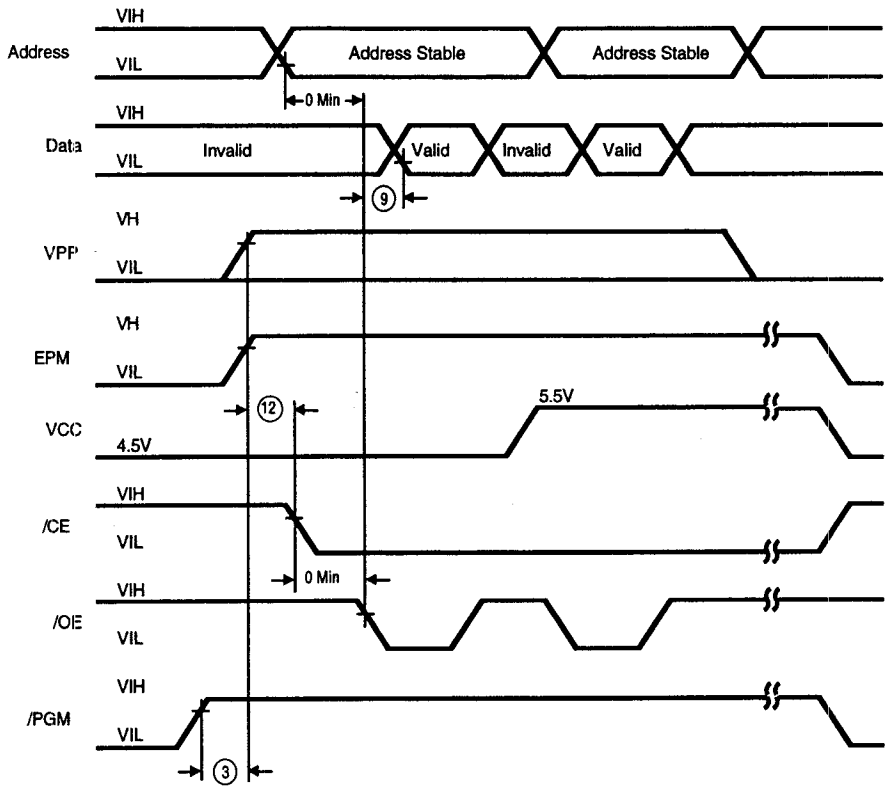


Figure 24. Z86E03/E07 Programming Waveform (EPROM Read)

DC ELECTRICAL CHARACTERISTICS
Z86E03/E06

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.3V	0.9 V_{CC}	V_{CC}+0.3	0.9 V_{CC}	V_{CC}+0.3	2.4	V	Driven by External Clock Generator	
		5.0V	0.9 V_{CC}	V_{CC}+0.3	0.9 V_{CC}	V_{CC}+0.3	3.9	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.3V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.6	V	Driven by External Clock Generator	
		5.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	2.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	3.3V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.0	V		
		5.0V	V_{SS}–0.3	0.2 V_{CC}	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.3V	V_{CC}–0.4		V_{CC}–0.4		3.1	V	I_{OH} = -2.0 mA	[10]
		5.0V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	I_{OH} = -2.0 mA	[10]
V_{OL1}	Output Low Voltage	3.3V		0.8		0.8	0.2	V	I_{OL} = +4.0 mA	[10]
		5.0V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	[10]
V_{OL2}	Output Low Voltage	3.3V		1.0		1.0	0.4	V	I_{OL} = + 6 mA, 3 Pin Max	[10]
		5.0V		1.0		1.0	0.5	V	I_{OL} = +12 mA, 3 Pin Max	[10]
V_{OFFSET}	Comparator Input Offset Voltage	3.3V		±10		±10	±5	mV		
		5.0V		±10		±10	±5	mV		
V_{ICR}	Input Common Mode Voltage Range	3.3V	0V	V_{CC}–1.0v	0V	V_{CC}–1.5v				[7]
		5.0V	0V	V_{CC}–1.0v	0V	V_{CC}–1.5v				[7]
I_{IL}	Input Leakage	3.3V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.3V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.0V	–1.0	1.0	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	3.3V		6		6	3.0	mA	@ 8 MHz	[4,5,12]
		5.0V		11.0		11.0	6.0	mA	@ 8 MHz	[4,5,12]
		3.3V		8.0		8.0	4.5	mA	@ 12 MHz	[4,5,10,13]
		5.0V		15		15	9.0	mA	@ 12 MHz	[4,5,10,13]
I_{OB}	Input Bias Current	3.3V		300		300		nA		[7]
		5.0V		300		300		nA		[7]
I_{IO}	Input Offset Current	3.3V		+150		+150		nA		[7]
		5.0V		+150		+150		nA		[7]

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{OL3}	P36	5.0V		1.0		1.0		V	I_{OL} = 24 mA	
I_{CC1}	Standby Current	3.3V		3.0		3.0	1.3	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4, 5,12]
		5.0V		5		5	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4, 5,12]
		3.3V		4.5		4.5	2.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5,13]
		5.0V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5,13]
		3.3V		1.4		1.4	0.7	mA	Clock Divide-by-16 @ 8 MHz	[4, 5,12]
		5.0V		3.5		3.5	2.0	mA	Clock Divide-by-16 @ 8 MHz	[4, 5,12]
		3.3V		2.0		2.0	1.0	mA	Clock Divide-by-16 @ 12 MHz	[4, 5,13]
		5.0V		4.5		4.5	2.5	mA	Clock Divide-by-16 @ 12 MHz	[4, 5,13]
		5.0V		1.0		1.0		mA	HALT Mode @ 12 kHz	[4,5,11,13]
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6, 9]
		5.0V		10		20	3.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6, 9]
		3.3V		600		600	400	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6, 9,12]
		5.0V		1000		1000	800	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6, 9,12]
I_{ALL}	Auto Latch Low Current	3.3V		7.0		14.0	4.0	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		20.0		30.0	10	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.3V		−4.0		−8.0	−2.0	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		−9.0		−16.0	−5.0	µA	$0V < V_{IN} < V_{CC}$	
T_{POR}	Power-On Reset	3.3V	7	24	6	25	13	ms		
		5.0V	3	13	2	14	7	ms		
V_{LV}	V_{CC} Low Voltage Protection Voltage		2.2	2.8	1.7	3.0	2.6	V	6 MHz max Int. CLK Freq.	[3]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven on XTAL	0.3	5.0	mA	8 MHz
Crystal or Ceramic Resonator	3.0	5.0	mA	8 MHz

[2] V_{SS} = 0V = GND

[3] V_{CC} = 3.0V to 5.5V. The V_{LV} increases as the temperature decreases. Typical values measured at 3.3V and 5.0V.

[4] All outputs unloaded, I/O pins floating, inputs at rail.

[5] $C_{L1} = C_{L2}$ = 100 pF

[6] Same as note [4] except inputs at V_{CC}.

[7] For analog comparator inputs when analog comparators are enabled.

[8] Excludes clock pins.

[9] Clock must be forced Low when XTAL1 is clock-driven and XTAL2 is floating.

[10] STD mode (not low EMI mode).

[11] Low EMI Oscillator enabled.

[12] Z86E03 only.

[13] Z86E06 only.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = EXTERNAL)

No	Symbol	Parameter	V_{CC} Note [6]	T_A = 0°C to +70°C 4 MHz Min	Max	T_A = −40°C to +105°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	[1,7,8]
			5.5V	250	DC	250	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	[1,7,8]
			5.5V		25		25	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	125		125		ns	[1,7,8]
			5.5V	125		125		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			[1,7,8]
			5.5V	3TpC		3TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1,7,8]
			5.5V	4TpC		4TpC			[1,7,8]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	[1,7,8]
			5.5V		100		100	ns	[1,7,8]
8	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,7,8]
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			[1,2,7,8]
			5.5V	3TpC		3TpC			[1,2,7,8]
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	[1,4,]
			5.5V	12		12		ns	[1,4]
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		[1,3,8,9]
			5.5V		5TpC		5TpC		[1,3,8,9]

Notes:

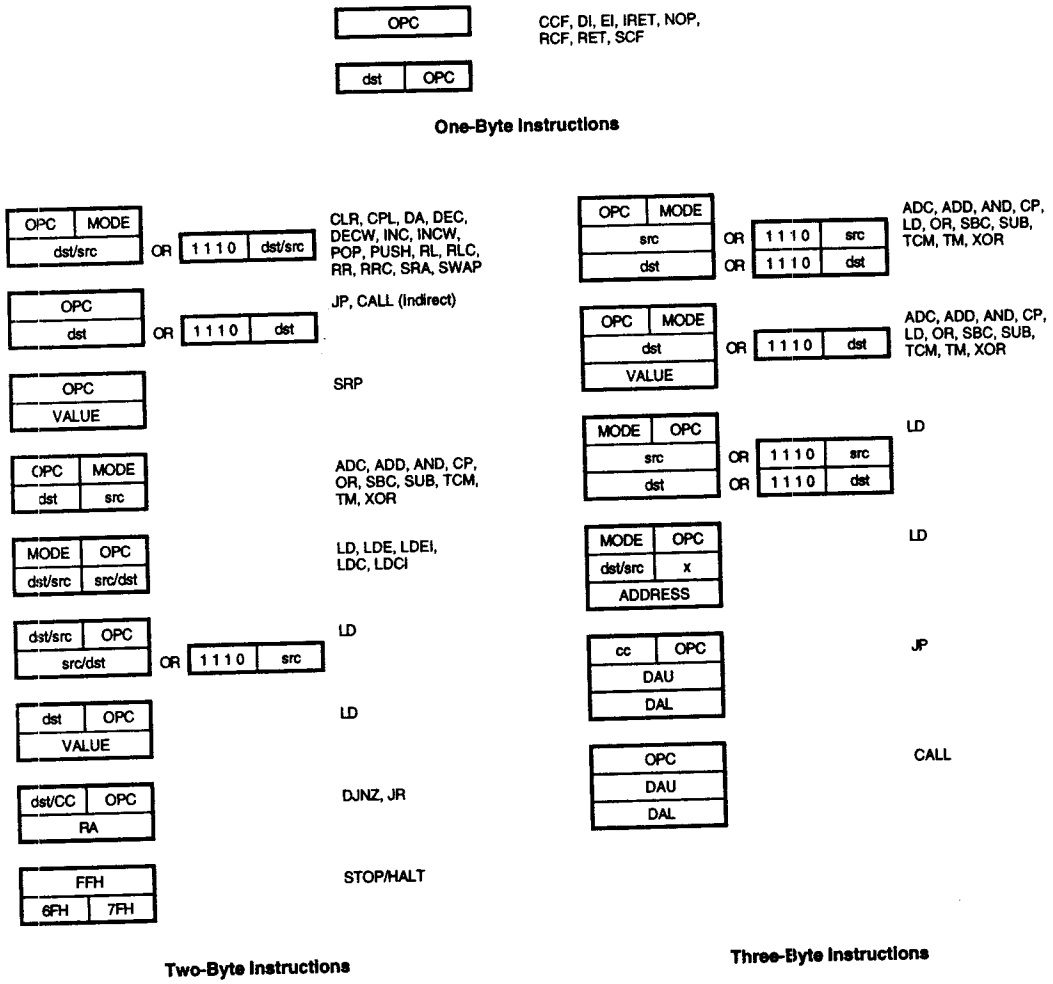
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P33-P31).
[3] SMR-D5 = 0.
[4] SMR-D5 = 1, POR STOP mode delay is on.
[5] Reg. WDTMR.
[6] V_{CC} = 3.0V to 5.5V.
[7] SMR D1 = 1.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

PS0201001-0603

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, 128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r r R R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -
POP dst dst←@SP; SP←SP + 1	R IR	50 51	- - - - - -
PUSH src SP←SP - 1; @SP←src	R IR	70 71	- - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP + 2		AF	- - - - - -
RL dst	R IR	90 91	* * * * - -
RLC dst	R IR	10 11	* * * * - -
RR dst	R IR	E0 E1	* * * * - -
RRC dst	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst–src–C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst	R IR	D0 D1	* * * 0 - -
SRP dst RP←src	Im	31	- - - - - -
STOP		6F	1 - - - - -

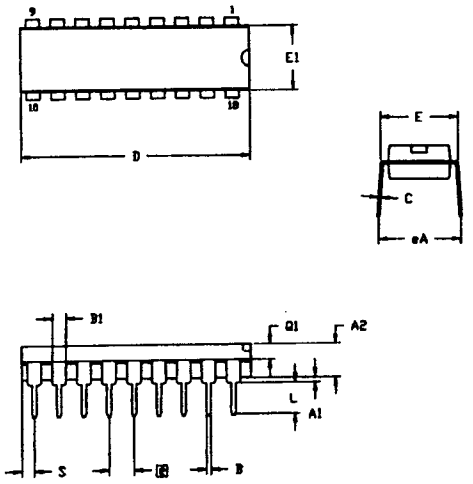
Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
SUB dst, src dst←dst - src	†	2[ ]	* * * * 1 *
SWAP dst	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
WDT		5F	- X X X - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

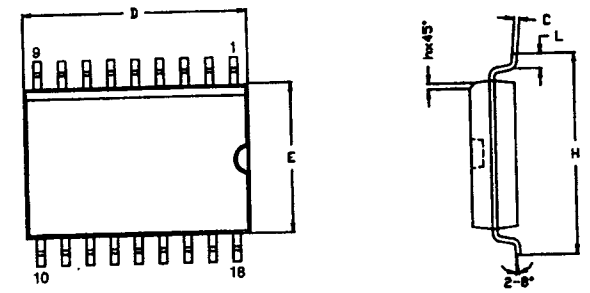
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

18-Pin SOIC Package Diagram