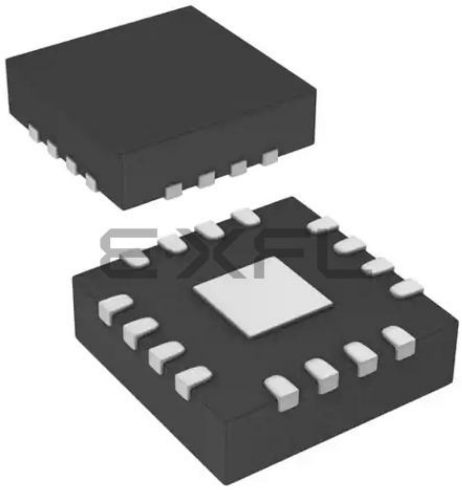

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	67 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 3x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VFQFN Exposed Pad
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f526-e-mg

4.2 Data Memory (SRAM and FSRs)

Data memory is composed of registers or bytes of SRAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers (SFR) and General Purpose Registers (GPR).

The Special Function Registers are registers used by the CPU and peripheral functions for controlling desired operations of the PIC16F526. See Figure 4-1 for details.

The PIC16F526 register file is composed of 16 Special Function Registers and 67 General Purpose Registers.

4.2.1 GENERAL PURPOSE REGISTER FILE

The General Purpose Register file is accessed, either directly or indirectly, through the File Select Register (FSR). See **Section 4.8 “Indirect Data Addressing: INDF and FSR Registers”**.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

FIGURE 4-2: REGISTER FILE MAP

FSR<6:5> → / File Address	00	01 (20h)	10 (40h)	11 (60h)
00h	INDF(1)	INDF(1)	INDF(1)	INDF(1)
01h	TMR0	EECON	TMR0	EECON
02h	PCL	PCL	PCL	PCL
03h	STATUS	STATUS	STATUS	STATUS
04h	FSR	FSR	FSR	FSR
05h	OSCCAL	EEDATA	OSCCAL	EEDATA
06h	PORTB	EEADR	PORTB	EEADR
07h	PORTC	PORTC	PORTC	PORTC
08h	CM1CON0	CM1CON0	CM1CON0	CM1CON0
09h	ADCON0	ADCON0	ADCON0	ADCON0
0Ah	ADRES	ADRES	ADRES	ADRES
0Bh	CM2CON0	CM2CON0	CM2CON0	CM2CON0
0Ch	VRCON	VRCON	VRCON	VRCON
0Dh–0Fh	General Purpose Registers	Addresses map back to addresses in Bank 0. (2Fh)	(4Fh)	(6Fh)
10h–1Fh	General Purpose Registers	30h–3Fh General Purpose Registers	50h–5Fh General Purpose Registers	70h–7Fh General Purpose Registers
	Bank 0	Bank 1	Bank 2	Bank 3

Note 1: Not a physical register. See **Section 4.8 “Indirect Data Addressing: INDF and FSR Registers”**.

4.8 Indirect Data Addressing: INDF and FSR Registers

The INDF Register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR Register (FSR is a *pointer*). This is indirect addressing.

Reading INDF itself indirectly (FSR = `0`) will produce 00h. Writing to the INDF Register indirectly results in a no-operation (although Status bits may be affected).

The FSR is an 8-bit wide register. It is used in conjunction with the INDF Register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

FSR<6:5> are the bank select bits and are used to select the bank to be addressed (`00` = Bank 0, `01` = Bank 1, `10` = Bank 2, `11` = Bank 3).

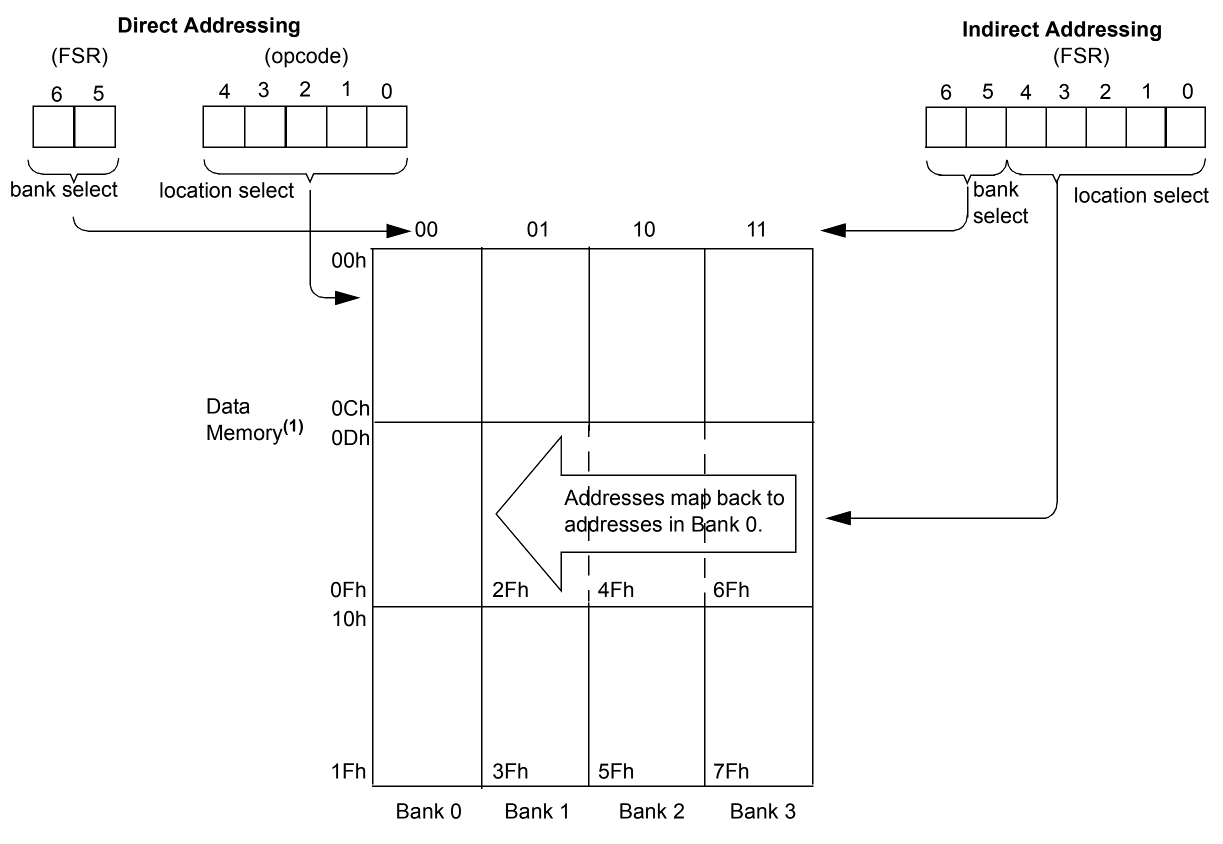
FSR<7> is unimplemented and read as '`1`'.

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
         MOVLW   0x10     ;initialize pointer
         MOVWF   FSR      ;to RAM
NEXT     CLRF    INDF     ;clear INDF
                          ;register
         INCF    FSR,F    ;inc pointer
         BTFSC   FSR,4    ;all done?
         GOTO    NEXT     ;NO, clear next
CONTINUE
              :           ;YES, continue
              :
```

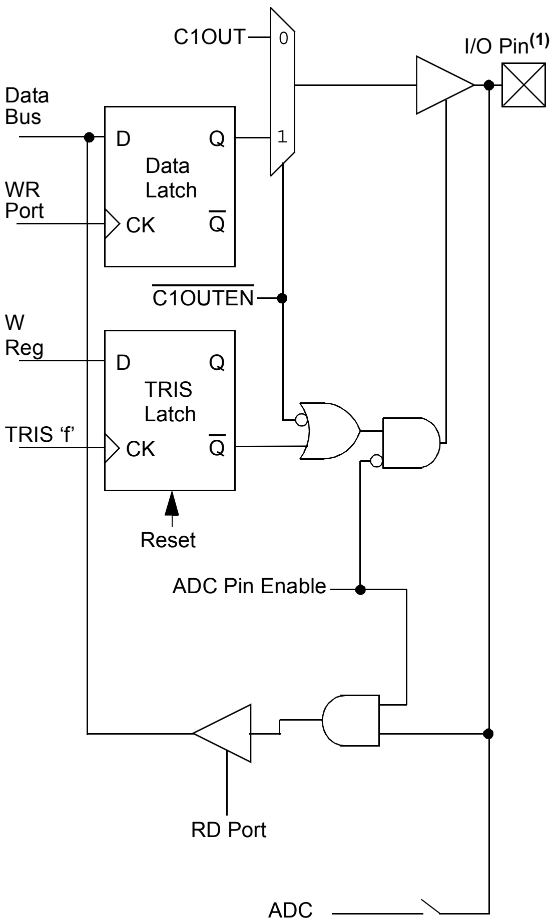
FIGURE 4-4: DIRECT/INDIRECT ADDRESSING



Note 1: For register map detail see Figure 4-1.

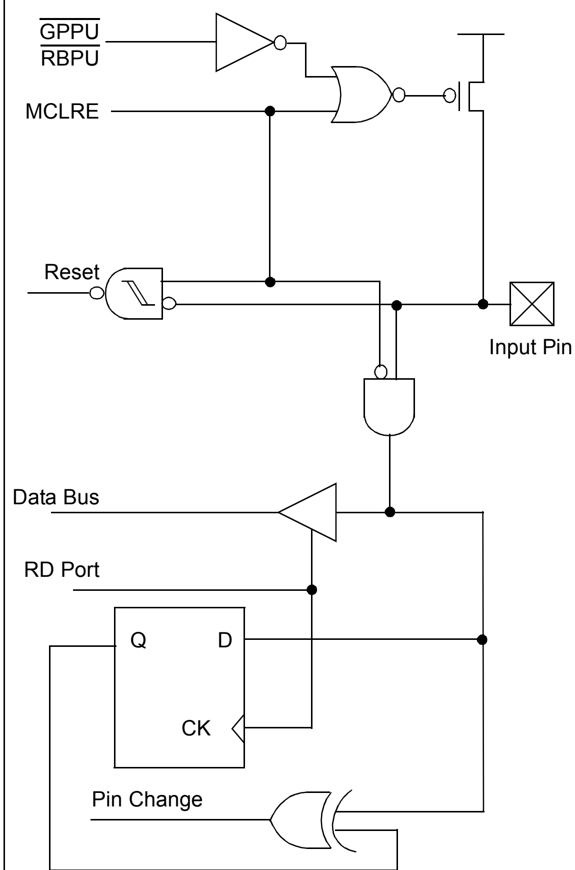
NOTES:

FIGURE 6-2: BLOCK DIAGRAM OF RB2



Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 6-3: BLOCK DIAGRAM OF RB3 (with Weak Pull-up and Wake-up on Change)



Note 1: RB3/MCLR pin has a protection diode to VSS only.

6.5 I/O Programming Considerations

6.5.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The `BCF` and `BSF` instructions, for example, read the entire port into the CPU, execute the bit operation and rewrite the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a `BSF` operation on bit 5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit 5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit 0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 6-1 shows the effect of two sequential Read-Modify-Write instructions (e.g., `BCF`, `BSF`, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired OR", "wired AND"). The resulting high output currents may damage the chip.

EXAMPLE 6-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT(e.g. DSTEMP)

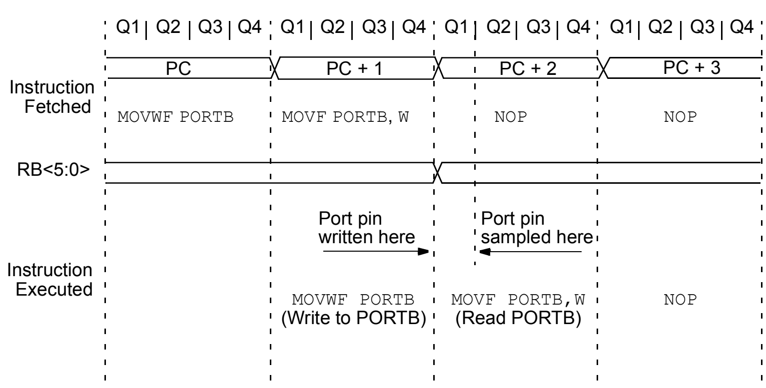
```
;Initial PORTB Settings
;PORTB<5:3> Inputs
;PORTB<2:0> Outputs
;
;                PORTB latch  PORTB pins
;                ----------   ----------
 BCF    PORTB, 5 ;--01 -ppp   --11 pppp
 BCF    PORTB, 4 ;--10 -ppp   --11 pppp
 MOVLW  007h;
 TRIS   PORTB    ;--10 -ppp   --11 pppp
;
```

Note 1: The user may have expected the pin values to be '`--00 pppp`'. The 2nd `BCF` caused RB5 to be latched as the pin value (High).

6.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 6-11). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a `NOP` or another instruction not accessing this I/O port.

FIGURE 6-11: SUCCESSIVE I/O OPERATION



This example shows a write to PORTB followed by a read from PORTB.

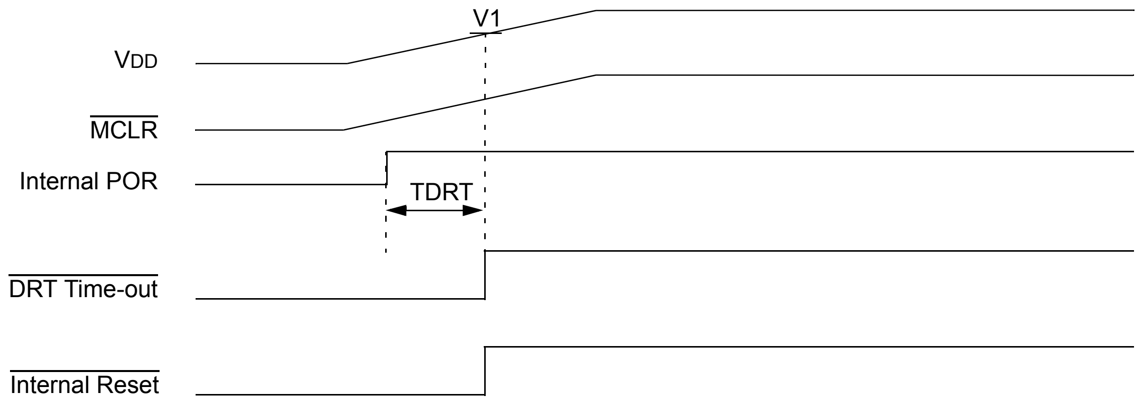
Data setup time = (0.25 T_{CY} – T_{PD})

where: T_{CY} = instruction cycle.

T_{PD} = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.

FIGURE 8-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



Note: When V_{DD} rises slowly, the T_{DRT} time-out expires long before V_{DD} has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ V_{DD} min.

8.5 Device Reset Timer (DRT)

On the PIC16F526 device, the DRT runs any time the device is powered up. DRT runs from Reset and varies based on oscillator selection and Reset type (see Table 8-5).

The DRT operates on an internal RC oscillator. The processor is kept in Reset as long as the DRT is active. The DRT delay allows VDD to rise above VDD min. and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a Reset condition after $\overline{\text{MCLR}}$ has reached a logic high (VIH $\overline{\text{MCLR}}$) level. Programming RB3/$\overline{\text{MCLR}}$/VPP as $\overline{\text{MCLR}}$ and using an external RC network connected to the $\overline{\text{MCLR}}$ input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the RB3/$\overline{\text{MCLR}}$/VPP pin as a general purpose input.

The Device Reset Time delays will vary from chip-to-chip due to VDD, temperature and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out from Sleep. This is particularly important for applications using the WDT to wake from Sleep mode automatically.

Reset sources are POR, $\overline{\text{MCLR}}$, WDT time-out and wake-up on pin or comparator change. See **Section 8.9.2 "Wake-up from Sleep", Notes 1, 2** and **3**.

8.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the external RC oscillator of the RB5/OSC1/CLKIN pin and the internal 4/8 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a `SLEEP` instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset, generates a device Reset.

The $\overline{\text{TO}}$ bit of the STATUS register will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a '0' (see **Section 8.1 "Configuration Bits"**). Refer to the PIC16F526 Programming Specifications to determine how to access the Configuration Word.

TABLE 8-5: TYPICAL DRT PERIODS

Oscillator Configuration	POR Reset	Subsequent Resets
HS, XT, LP	18 ms	18 ms
EC	1.125 ms	10 μs
INTOSC, EXTRC	1.125 ms	10 μs

8.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst-case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

8.6.2 WDT PROGRAMMING CONSIDERATIONS

The `CLRWDT` instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The `SLEEP` instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

9.0 ANALOG-TO-DIGITAL (A/D) CONVERTER

The A/D Converter allows conversion of an analog signal into an 8-bit digital signal.

9.1 Clock Divisors

The ADC has 4 clock source settings ADCS<1:0>. There are 3 divisor values 16, 8 and 4. The fourth setting is INTOSC with a divisor of 4. These settings will allow a proper conversion when using an external oscillator at speeds from 20 MHz to 350 kHz. Using an external oscillator at a frequency below 350 kHz requires the ADC oscillator setting to be INTOSC/4 (ADCS<1:0> = `11`) for valid ADC results.

The ADC requires 13 T_{AD} periods to complete a conversion. The divisor values do not affect the number of T_{AD} periods required to perform a conversion. The divisor values determine the length of the T_{AD} period.

When the ADCS<1:0> bits are changed while an ADC conversion is in process, the new ADC clock source will not be selected until the next conversion is started. This clock source selection will be lost when the device enters Sleep.

> **Note:** The ADC clock is derived from the instruction clock. The ADCS divisors are then applied to create the ADC clock

9.1.1 VOLTAGE REFERENCE

There is no external voltage reference for the ADC. The ADC reference voltage will always be V_{DD}.

9.1.2 ANALOG MODE SELECTION

The ANS<1:0> bits are used to configure pins for analog input. Upon any Reset, ANS<1:0> defaults to 11. This configures pins AN0, AN1 and AN2 as analog inputs. The comparator output, C1OUT, will override AN2 as an input if the comparator output is enabled. Pins configured as analog inputs are not available for digital output. Users should not change the ANS bits while a conversion is in process. ANS bits are active regardless of the condition of ADON.

9.1.3 ADC CHANNEL SELECTION

The CHS bits are used to select the analog channel to be sampled by the ADC. The CHS<1:0> bits can be changed at any time without adversely effecting a conversion. To acquire an analog signal the CHS<1:0> selection must match one of the pin(s) selected by the ANS<1:0> bits. When the ADC is on (ADON = `1`) and a channel is selected that is also being used by the comparator, then both the comparator and the ADC will see the analog voltage on the pin.

> **Note:** It is the users responsibility to ensure that use of the ADC and comparator simultaneously on the same pin, does not adversely affect the signal being monitored or adversely effect device operation.

When the CHS<1:0> bits are changed during an ADC conversion, the new channel will not be selected until the current conversion is completed. This allows the current conversion to complete with valid results. All channel selection information will be lost when the device enters Sleep.

TABLE 9-1: CHANNEL SELECT (ADCS) BITS AFTER AN EVENT

Event	ADCS<1:0>
$\overline{\text{MCLR}}$	11
Conversion completed	CS<1:0>
Conversion terminated	CS<1:0>
Power-on	11
Wake from Sleep	11

9.1.4 THE GO/$\overline{\text{DONE}}$ BIT

The GO/$\overline{\text{DONE}}$ bit is used to determine the status of a conversion, to start a conversion and to manually halt a conversion in process. Setting the GO/$\overline{\text{DONE}}$ bit starts a conversion. When the conversion is complete, the ADC module clears the GO/$\overline{\text{DONE}}$ bit. A conversion can be terminated by manually clearing the GO/$\overline{\text{DONE}}$ bit while a conversion is in process. Manual termination of a conversion may result in a partially converted result in ADRES.

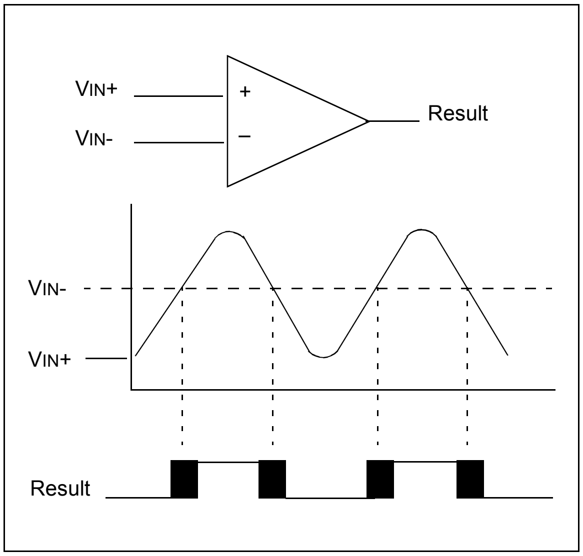
The GO/$\overline{\text{DONE}}$ bit is cleared when the device enters Sleep, stopping the current conversion. The ADC does not have a dedicated oscillator, it runs off of the instruction clock. Therefore, no conversion can occur in sleep.

The GO/$\overline{\text{DONE}}$ bit cannot be set when ADON is clear.

10.1 Comparator Operation

A single comparator is shown in Figure 10-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. The shaded area of the output of the comparator in Figure 10-2 represent the uncertainty due to input offsets and response time. See Table 14-2 for Common Mode Voltage.

FIGURE 10-2: SINGLE COMPARATOR



10.2 Comparator Reference

An internal reference signal may be used depending on the comparator operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 10-2). Please see **Section 11.0 “Comparator Voltage Reference Module”** for internal reference specifications.

10.3 Comparator Response Time

Response time is the minimum time after selecting a new reference voltage or input source before the comparator output is to have a valid level. If the comparator inputs are changed, a delay must be used to allow the comparator to settle to its new state. Please see Table 14-3 for comparator response time specifications.

10.4 Comparator Output

The comparator output is read through the CM1CON0 or CM2CON0 register. This bit is read-only. The comparator output may also be used externally, see Figure 10-1.

Note:	Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

10.5 Comparator Wake-up Flag

The Comparator Wake-up Flag is set whenever all of the following conditions are met:

- $\overline{\text{C1WU}}$ = `0` (CM1CON0<0>) or $\overline{\text{C2WU}}$ = `0` (CM2CON0<0>)
- CM1CON0 or CM2CON0 has been read to latch the last known state of the C1OUT and C2OUT bit (`MOVF CM1CON0, W`)
- Device is in Sleep
- The output of a comparator has changed state

The wake-up flag may be cleared in software or by another device Reset.

10.6 Comparator Operation During Sleep

When the comparator is enabled it is active. To minimize power consumption while in Sleep mode, turn off the comparator before entering Sleep.

10.7 Effects of Reset

A Power-on Reset (POR) forces the CM2CON0 register to its Reset state. This forces the Comparator input pins to analog Reset mode. Device current is minimized when analog inputs are present at Reset time.

10.8 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 10-3. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

11.0 COMPARATOR VOLTAGE REFERENCE MODULE

The Comparator Voltage Reference module also allows the selection of an internally generated voltage reference for one of the C2 comparator inputs. The VRCON register (Register 11-1) controls the Voltage Reference module shown in Figure 11-1.

11.1 Configuring The Voltage Reference

The voltage reference can output 32 voltage levels; 16 in a high range and 16 in a low range.

Equation 11-1 determines the output voltages:

EQUATION 11-1:

$$VRR = 1 \text{ (low range)}: CV_{REF} = (VR<3:0>/24) \times V_{DD}$$

$$VRR = 0 \text{ (high range)}:$$

$$CV_{REF} = (V_{DD}/4) + (VR<3:0> \times V_{DD}/32)$$

11.2 Voltage Reference Accuracy/Error

The full range of VSS to VDD cannot be realized due to construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 11-1) keep CVREF from approaching VSS or VDD. The exception is when the module is disabled by clearing the VREN bit of the VRCON register. When disabled, the reference voltage is VSS when VR<3:0> is '0000' and the VRR bit of the VRCON register is set. This allows the comparator to detect a zero-crossing and not consume the CVREF module current.

The voltage reference is VDD derived and, therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the comparator voltage reference can be found in **Section 14.0 "Electrical Characteristics"**.

REGISTER 11-1: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	VROE	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **VREN:** CVREF Enable bit
1 = CVREF is powered on
0 = CVREF is powered down, no current is drawn

bit 6 **VROE:** CVREF Output Enable bit(1)
1 = CVREF output is enabled
0 = CVREF output is disabled

bit 5 **VRR:** CVREF Range Selection bit
1 = Low range
0 = High range

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **VR<3:0>** CVREF Value Selection bit
When VRR = 1: CVREF= (VR<3:0>/24)*VDD
When VRR = 0: CVREF= VDD/4+(VR<3:0>/32)*VDD

Note 1: When this bit is set, the TRIS for the CVREF pin is overridden and the analog voltage is placed on the CVREF pin.

FIGURE 11-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

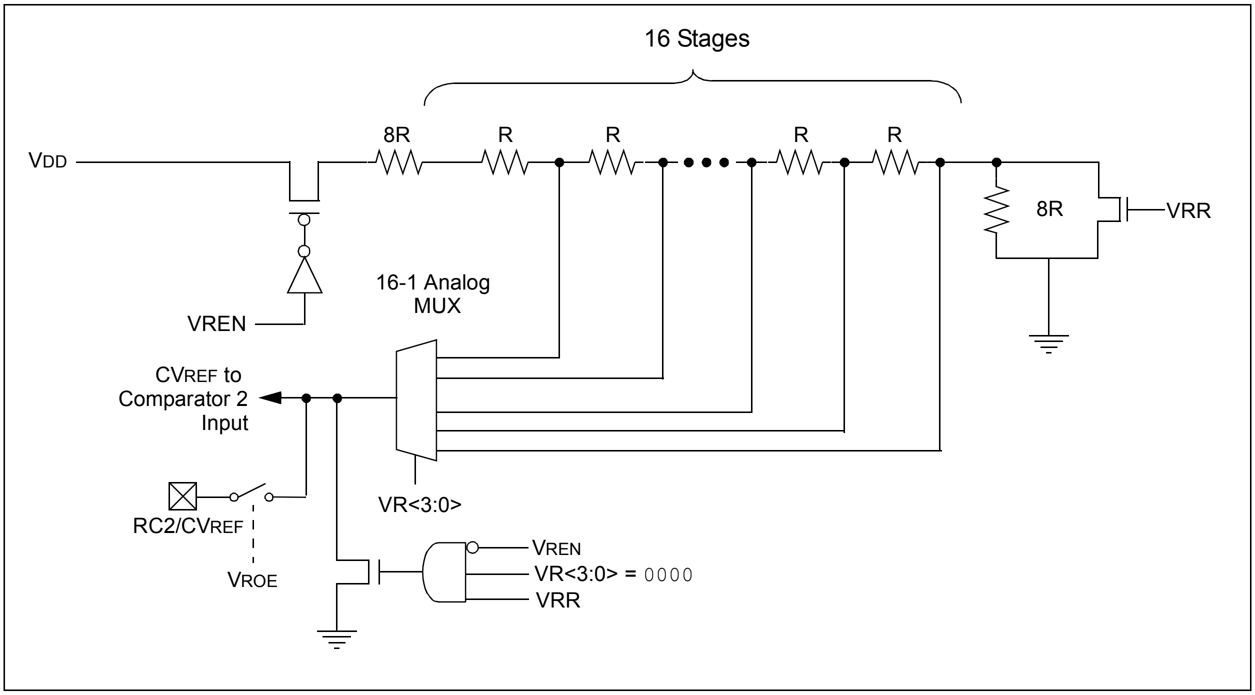


TABLE 11-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	001- 1111	uuu- uuuu
CM1CON0	C1OUT	$\overline{\text{C1OUTEN}}$	C1POL	$\overline{\text{C1T0CS}}$	C1ON	C1NREF	C1PREF	$\overline{\text{C1WU}}$	q111 1111	quuu uuuu
CM2CON0	C2OUT	$\overline{\text{C2OUTEN}}$	C2POL	C2PREF2	C2ON	C2NREF	C2PREF1	$\overline{\text{C2WU}}$	q111 1111	quuu uuuu

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0', q = value depends on condition.

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \leq f \leq 31$ $0 \leq b < 7$
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.

CALL	Subroutine Call
Syntax:	[*label*] CALL k
Operands:	$0 \leq k \leq 255$
Operation:	(PC) + 1→ Top-of-Stack; k → PC<7:0>; (STATUS<6:5>) → PC<10:9>; 0 → PC<8>
Status Affected:	None
Description:	Subroutine call. First, return address (PC + 1) is PUSHed onto the stack. The eight-bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two-cycle instruction.

CLRF	Clear f
Syntax:	[*label*] CLRF f
Operands:	$0 \leq f \leq 31$
Operation:	00h → (f); 1 → Z
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

CLRW	Clear W
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W); 1 → Z
Status Affected:	Z
Description:	The W register is cleared. Zero bit (Z) is set.

CLRWDT	Clear Watchdog Timer
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT; 0 → WDT prescaler (if assigned); 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

COMF	Complement f
Syntax:	[*label*] COMF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(\bar{f})$ → (dest)
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

DECF	Decrement f
Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) – 1 → (dest)
Status Affected:	Z
Description:	Decrement register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) – 1 → d; skip if result = 0
Status Affected:	None
Description:	The contents of register ‘f’ are decremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. If the result is ‘0’, the next instruction, which is already fetched, is discarded and a `NOP` is executed instead making it a two-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 511$
Operation:	k → PC<8:0>; STATUS<6:5> → PC<10:9>
Status Affected:	None
Description:	`GOTO` is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. `GOTO` is a two-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) + 1 → (dest)
Status Affected:	Z
Description:	The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) + 1 → (dest), skip if result = 0
Status Affected:	None
Description:	The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. If the result is ‘0’, then the next instruction, which is already fetched, is discarded and a `NOP` is executed instead making it a two-cycle instruction.

IORLW	Inclusive OR literal with W
Syntax:	[*label*] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. (k) → (W)
Status Affected:	Z
Description:	The contents of the W register are OR’ed with the eight-bit literal ‘k’. The result is placed in the W register.

TRIS	Load TRIS Register
Syntax:	[*label*] TRIS f
Operands:	f = 6
Operation:	(W) $\rightarrow$ TRIS register f
Status Affected:	None
Description:	TRIS register ‘f’ (f = 6 or 7) is loaded with the contents of the W register

XORLW	Exclusive OR literal with W
Syntax:	[*label*] XORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .XOR. k $\rightarrow$ (W)
Status Affected:	Z
Description:	The contents of the W register are XOR’ed with the eight-bit literal ‘k’. The result is placed in the W register.

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (dest)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

13.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

13.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

13.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

13.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

14.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Ambient temperature under bias .... -40°C to +125°C
Storage temperature .... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... 0 to +6.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} .... 0 to +13.5V
Voltage on all other pins with respect to V_{SS} .... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) .... 700 mW
Max. current out of V_{SS} pin .... 200 mA
Max. current into V_{DD} pin .... 150 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) .... ±20 mA
Max. output current sunk by any I/O pin .... 25 mA
Max. output current sourced by any I/O pin .... 25 mA
Max. output current sourced by I/O port .... 75 mA
Max. output current sunk by I/O port .... 75 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 14-1: PIC16F526 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C

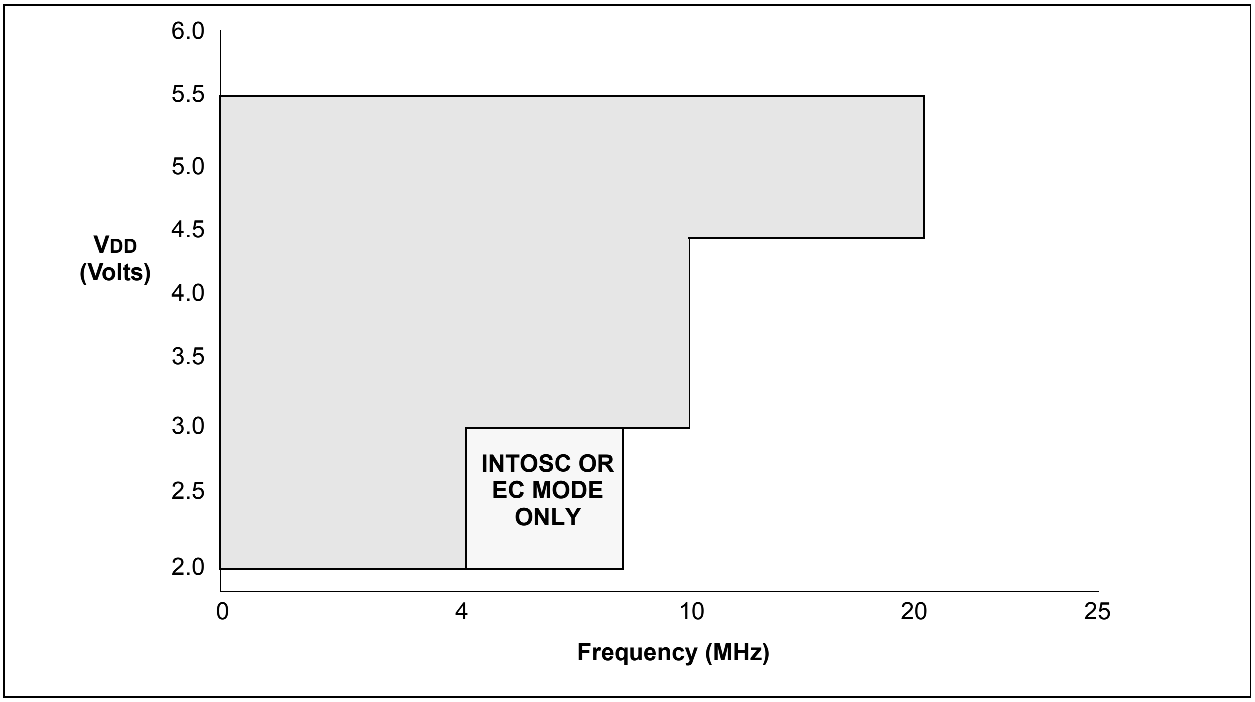
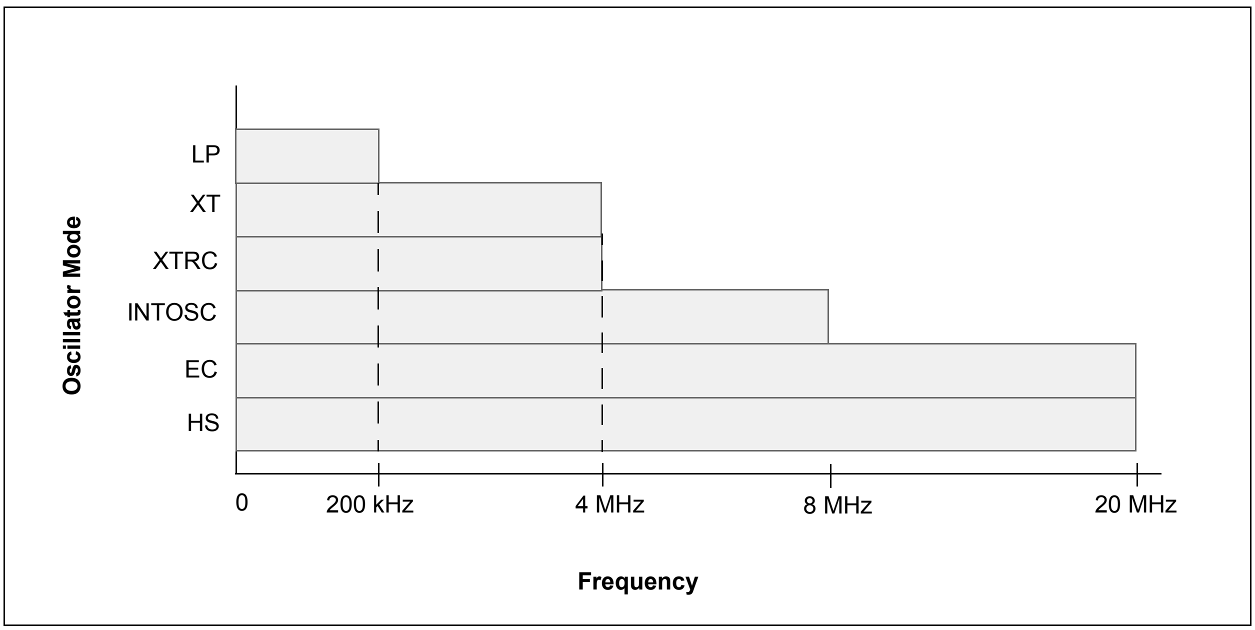
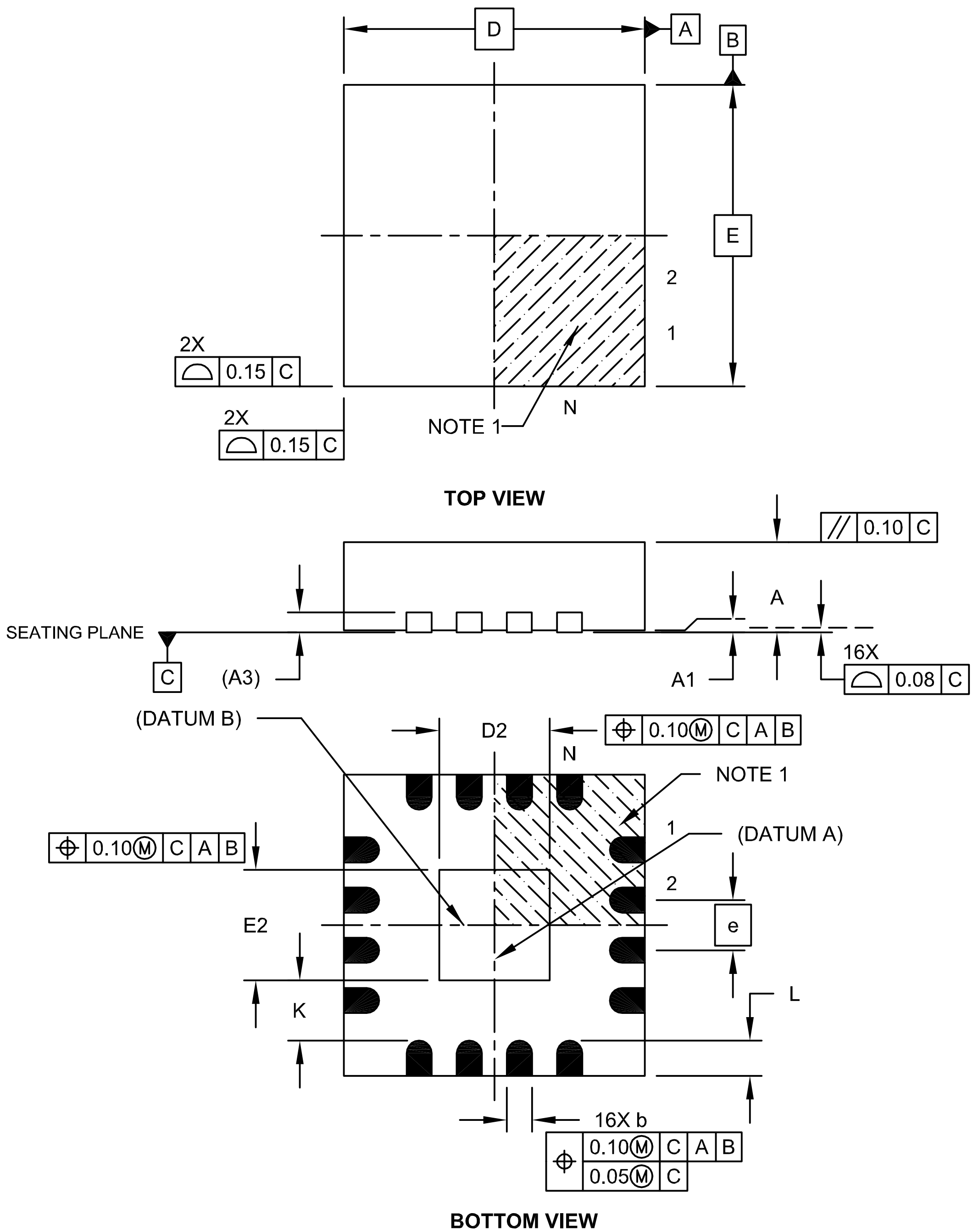


FIGURE 14-2: MAXIMUM OSCILLATOR FREQUENCY TABLE



16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-142A Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision A (August 2007)

Original release of this document.

Revision B (December 2008)

Added DC and AC Characteristics graphs; Updated Electrical Characteristics section; added I/O diagrams; updated the Flash Data Memory Control Section; made various changes to the Special Features of the CPU Section and made general edits. Miscellaneous updates.

Revision C (July 2009)

Removed "Preliminary" status; Revised Table 6-3: I/O Pins; Revised Table 8-3: Reset Conditions; Revised Table 14-4: A/D Converter Char.

Revision D (March 2010)

Added Package Drawings and Package Marking Information for the 16-Lead Package Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body (QFN); Updated the Product Identification System section.

Revision E (June 2010)

Revised Section 6 (I/O) Figures 6-1, 6-4 and 6-6.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC16F526 PIC16F526T(1)
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package:	P = Plastic (PDIP)(2) SL = 14L Small Outline, 3.90 mm (SOIC)(2) ST = Thin Shrink Small Outline (TSSOP)(2) MG = 16-Lead 3x3 (QFN)(2)
Pattern:	Special Requirements

Examples:

a) PIC16F526-E/P 301 = Extended Temp., PDIP package, QTP pattern #301
b) PIC16F526-I/SL = Industrial Temp., SOIC package
c) PIC16F526T-E/P = Extended Temp., PDIP package, Tape and Reel
d) PIC16F526T-I/MG = Industrial Temp., QFN Package, Tape and Reel

Note 1: T = in tape and reel SOIC, TSSOP and QFN packages only
2: Pb-free.