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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	67 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 3x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f526-e-sl

FIGURE 1-1: 14-PIN PDIP, SOIC, TSSOP DIAGRAM

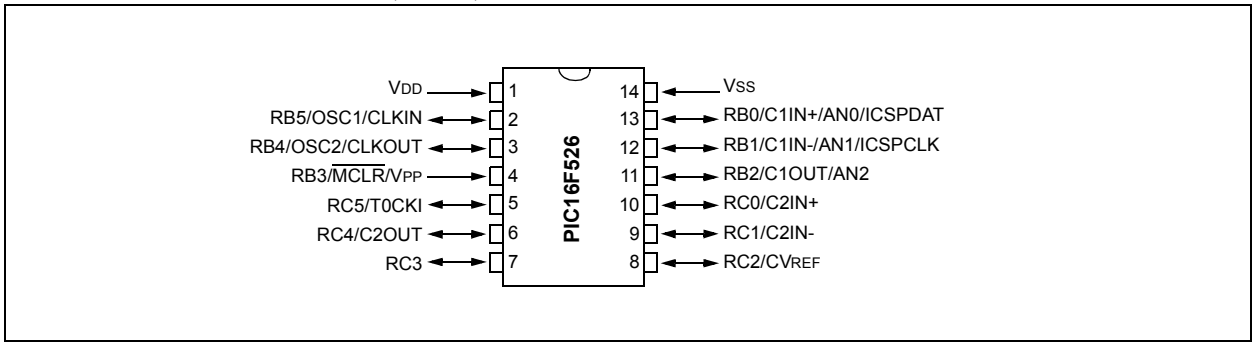


FIGURE 1-2: 16-PIN QFN DIAGRAM

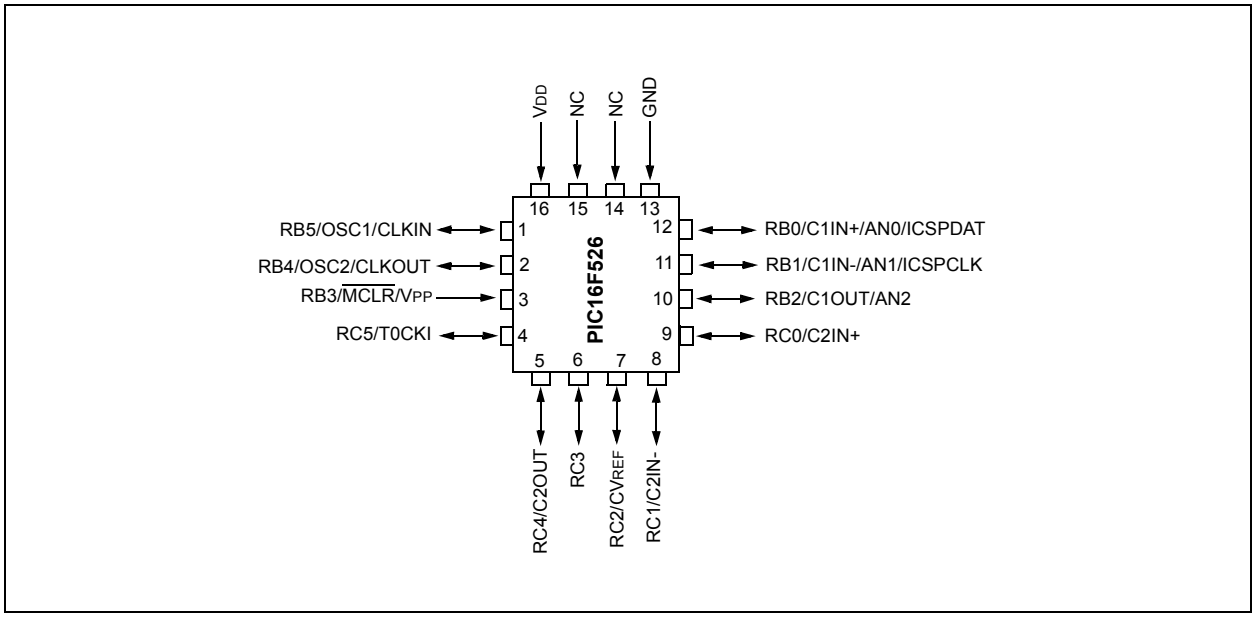


TABLE 3-2: PIC16F526 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RB0//C1IN+/AN0/ ICSPDAT	RB0	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	C1IN+	AN	—	Comparator 1 input.
	AN0	AN	—	ADC channel input.
	ICSPDAT	ST	CMOS	ICSP™ mode Schmitt Trigger.
RB1/C1IN-/AN1/ ICSPCLK	RB1	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	C1IN-	AN	—	Comparator 1 input.
	AN1	AN	—	ADC channel input.
	ICSPCLK	ST	CMOS	ICSP mode Schmitt Trigger.
RB2/C1OUT/AN2	RB2	TTL	CMOS	Bidirectional I/O pin.
	C1OUT	—	CMOS	Comparator 1 output.
	AN2	AN	—	ADC channel input.
RB3/$\overline{\text{MCLR}}$/V_{PP}	RB3	TTL	—	Input pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear (Reset). When configured as $\overline{\text{MCLR}}$, this pin is an active-low Reset to the device. Voltage on $\overline{\text{MCLR}}$/V_{PP} must not exceed V_{DD} during normal device operation or the device will enter Programming mode. Weak pull-up always on if configured as $\overline{\text{MCLR}}$.
	V_{PP}	HV	—	Programming voltage input.
RB4/OSC2/CLKOUT	RB4	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	OSC2	—	XTAL	Oscillator crystal output. Connections to crystal or resonator in Crystal Oscillator mode (XT, HS and LP modes only, PORTB in other modes).
	CLKOUT	—	CMOS	EXTRC/INTRC CLKOUT pin (F_{OSC}/4).
RB5/OSC1/CLKIN	RB5	TTL	CMOS	Bidirectional I/O pin.
	OSC1	XTAL	—	Oscillator crystal input.
	CLKIN	ST	—	External clock source input.
RC0/C2IN+	RC0	TTL	CMOS	Bidirectional I/O port.
	C2IN+	AN	—	Comparator 2 input.
RC1/C2IN-	RC1	TTL	CMOS	Bidirectional I/O port.
	C2IN-	AN	—	Comparator 2 input.
RC2/CV_{REF}	RC2	TTL	CMOS	Bidirectional I/O port.
	CV_{REF}	—	AN	Programmable Voltage Reference output.
RC3	RC3	TTL	CMOS	Bidirectional I/O port.
RC4/C2OUT	RC4	TTL	CMOS	Bidirectional I/O port.
	C2OUT	—	CMOS	Comparator 2 output.
RC5/T0CKI	RC5	TTL	CMOS	Bidirectional I/O port.
	T0CKI	ST	—	Timer0 Schmitt Trigger input pin.
V_{DD}	V_{DD}	—	P	Positive supply for logic and I/O pins.
V_{SS}	V_{SS}	—	P	Ground reference for logic and I/O pins.

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, HV = High Voltage

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

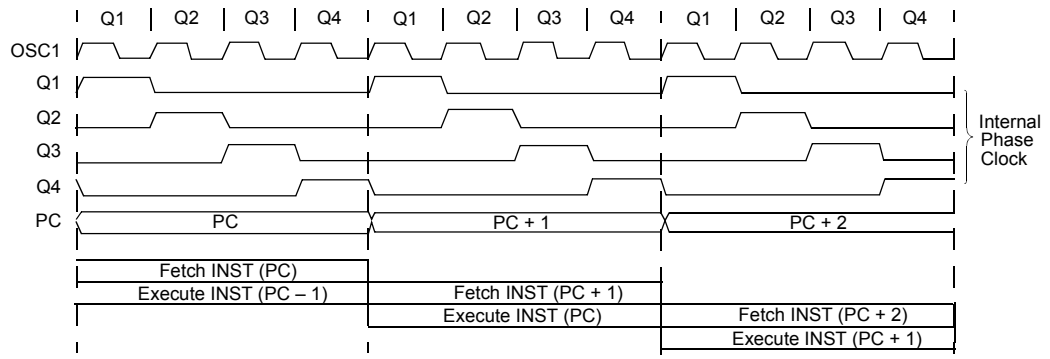
3.2 Instruction Flow/Pipelining

An instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the PC to change (e.g., `GOTO`), then two cycles are required to complete the instruction (Example 3-1).

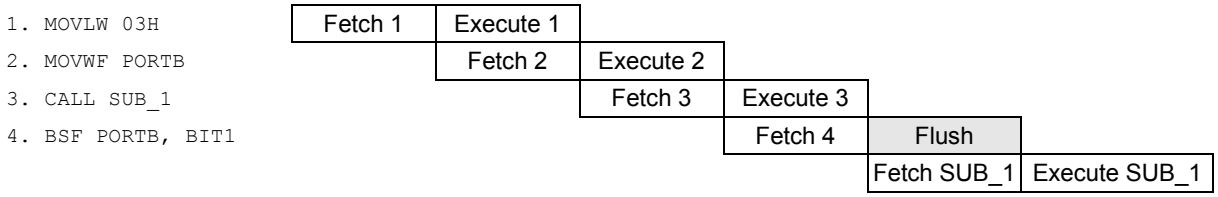
A fetch cycle begins with the PC incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles, since the fetch instruction is “flushed” from the pipeline, while the new instruction is being fetched and then executed.

4.2 Data Memory (SRAM and FSRs)

Data memory is composed of registers or bytes of SRAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers (SFR) and General Purpose Registers (GPR).

The Special Function Registers are registers used by the CPU and peripheral functions for controlling desired operations of the PIC16F526. See Figure 4-1 for details.

The PIC16F526 register file is composed of 16 Special Function Registers and 67 General Purpose Registers.

4.2.1 GENERAL PURPOSE REGISTER FILE

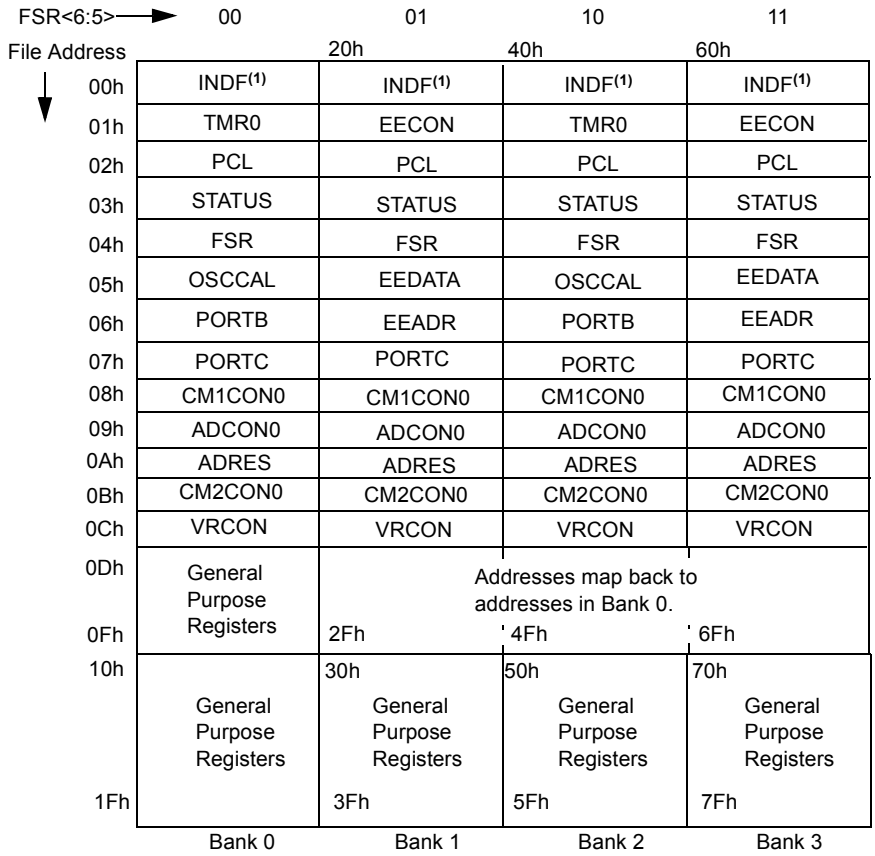
The General Purpose Register file is accessed, either directly or indirectly, through the File Select Register (FSR). See **Section 4.8 "Indirect Data Addressing: INDF and FSR Registers"**.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

FIGURE 4-2: REGISTER FILE MAP



Note 1: Not a physical register. See **Section 4.8 "Indirect Data Addressing: INDF and FSR Registers"**.

4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register, which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A Reset sets the OPTION <7:0> bits.

Note: If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin (i.e., note that TRIS overrides Option control of $\overline{\text{RBPU}}$ and $\overline{\text{RBWU}}$).

REGISTER 4-2: OPTION: OPTION REGISTER

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	T0CS(1)	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{RBWU}}$:** Enable Wake-up On Pin Change bit (RB0, RB1, RB3, RB4)
1 = Disabled
0 = Enabled

bit 6 **$\overline{\text{RBPU}}$:** Enable Weak Pull-ups bit (RB0, RB1, RB3, RB4)
1 = Disabled
0 = Enabled

bit 5 **T0CS:** Timer0 Clock Source Select bit(1)
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: If the T0CS bit is set to '1', it will override the TRIS function on the T0CKI pin.

4.5 OSCCAL Register

The Oscillator Calibration (OSCCAL) register is used to calibrate the 8 MHz internal oscillator macro. It contains 7 bits of calibration that uses a two's complement scheme for controlling the oscillator speed. See Register 4-3 for details.

REGISTER 4-3: OSCCAL: OSCILLATOR CALIBRATION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	U-0
CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—
bit 7							bit 0

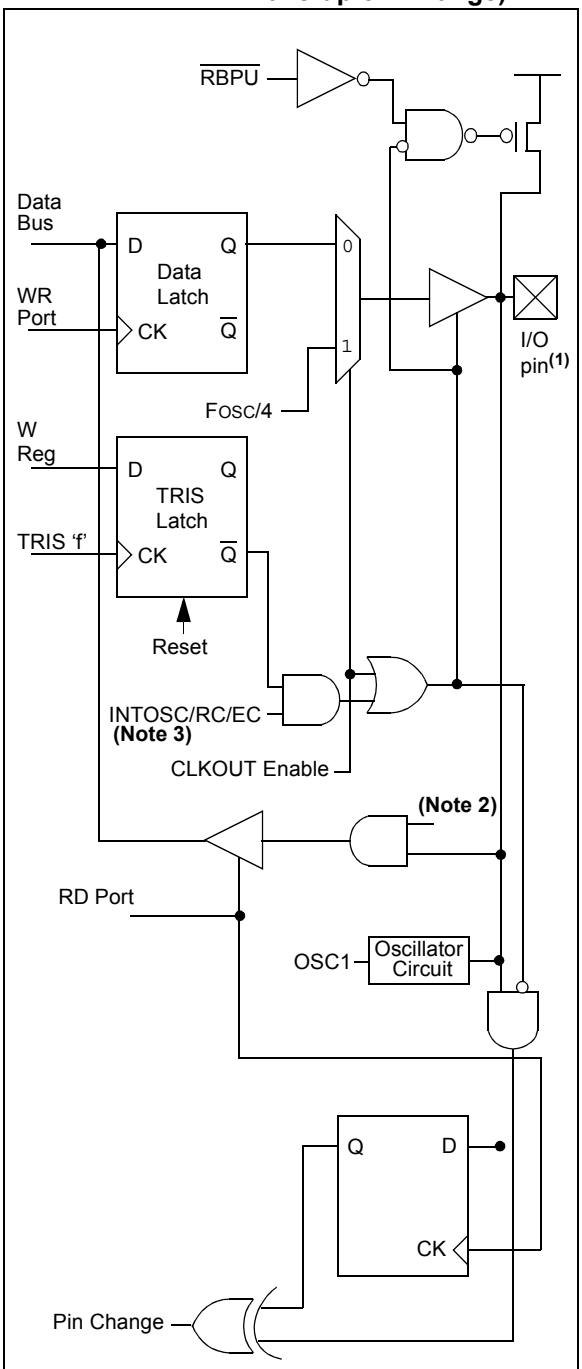
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **CAL<6:0>**: Oscillator Calibration bits

0111111 = Maximum frequency
•
•
•
0000001
0000000 = Center frequency
1111111
•
•
•
1000000 = Minimum frequency

bit 0 **Unimplemented**: Read as '0'

FIGURE 6-4: BLOCK DIAGRAM OF RB4 (with Weak Pull-up and Wake-up on Change)

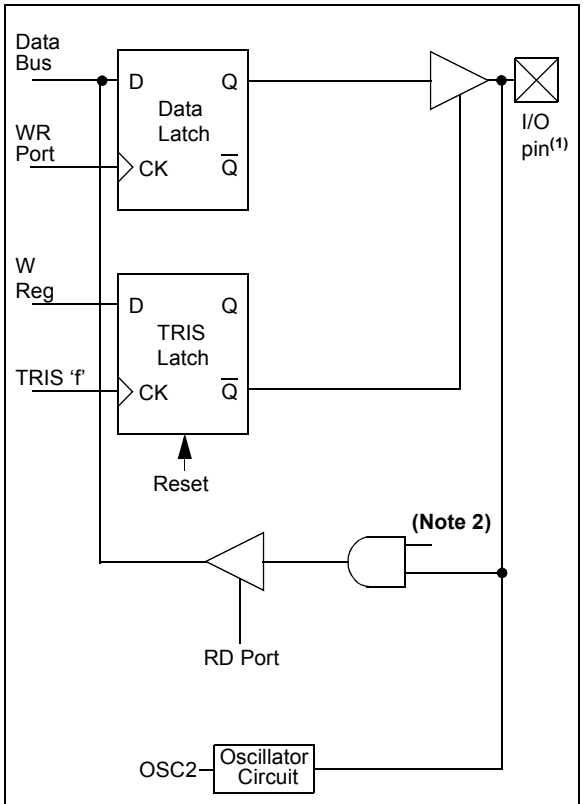


Note 1: I/O pins have protection diodes to VDD and VSS.

2: Input mode is disabled when pin is used for oscillator.

3: Pin is not used for oscillator.

FIGURE 6-5: BLOCK DIAGRAM OF RB5



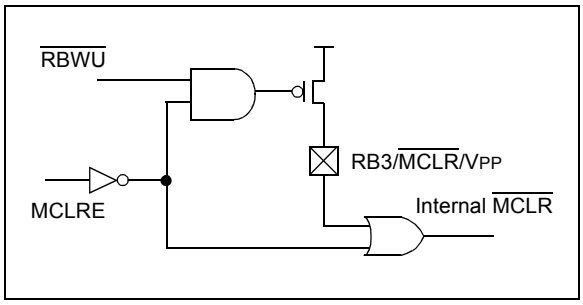
Note 1: I/O pins have protection diodes to VDD and VSS.

2: Input mode is disabled when pin is used for oscillator.

8.3.1 $\overline{\text{MCLR}}$ ENABLE

This Configuration bit, when unprogrammed (left in the '1' state), enables the external $\overline{\text{MCLR}}$ function. When programmed, the $\overline{\text{MCLR}}$ function is tied to the internal V_{DD} and the pin is assigned to be a I/O. See Figure 8-6.

FIGURE 8-6: $\overline{\text{MCLR}}$ SELECT



8.4 Power-on Reset (POR)

The PIC16F526 device incorporates an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until V_{DD} has reached a high enough level for proper operation. To take advantage of the internal POR, program the RB3/$\overline{\text{MCLR}}$/V_{PP} pin as $\overline{\text{MCLR}}$ and tie through a resistor to V_{DD}, or program the pin as RB3. An internal weak pull-up resistor is implemented using a transistor (refer to Table 14-5 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for V_{DD} is specified. See **Section 14.0 "Electrical Characteristics"** for details.

When the device starts normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 8-7.

The Power-on Reset circuit and the Device Reset Timer (see **Section 8.5 "Device Reset Timer (DRT)"**) circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$ to be high. After the time-out period, which is typically 18 ms or 1 ms, it will reset the Reset latch and thus end the on-chip Reset signal.

A power-up example where $\overline{\text{MCLR}}$ is held low is shown in Figure 8-8. V_{DD} is allowed to rise and stabilize before bringing $\overline{\text{MCLR}}$ high. The chip will actually come out of Reset T_{DRT} msec after $\overline{\text{MCLR}}$ goes high.

In Figure 8-9, the on-chip Power-on Reset feature is being used ($\overline{\text{MCLR}}$ and V_{DD} are tied together or the pin is programmed to be RB3. The V_{DD} is stable before the start-up timer times out and there is no problem in getting a proper Reset. However, Figure 8-10 depicts a problem situation where V_{DD} rises too slowly. The time between when the DRT senses that $\overline{\text{MCLR}}$ is high and when $\overline{\text{MCLR}}$ and V_{DD} actually reach their full value, is too long. In this situation, when the start-up timer times out, V_{DD} has not reached the V_{DD} (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 8-9).

Note:	When the device starts normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Notes AN522 *"Power-Up Considerations"* (DS00522) and AN607 *"Power-up Trouble Shooting"* (DS00607).

8.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits (TO, PD, RBWUF, CWUF)

The $\overline{TO}$, $\overline{PD}$ and RBWUF bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) Reset.

TABLE 8-7: $\overline{TO}$/$\overline{PD}$/RBWUF/CWUF STATUS AFTER RESET

CWUF	RBWUF	$\overline{TO}$	$\overline{PD}$	Reset Caused By
0	0	0	0	WDT wake-up from Sleep
0	0	0	u	WDT time-out (not from Sleep)
0	0	1	0	$\overline{MCLR}$ wake-up from Sleep
0	0	1	1	Power-up
0	0	u	u	$\overline{MCLR}$ not during Sleep
0	1	1	0	Wake-up from Sleep on pin change
1	0	1	0	Wake up from Sleep on comparator change

Legend: u = unchanged

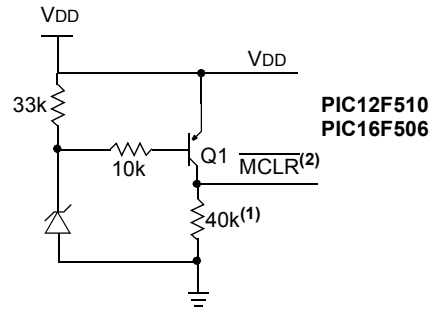
Note 1: The $\overline{TO}$, $\overline{PD}$ and RBWUF bits maintain their status (u) until a Reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$, $\overline{PD}$ and RBWUF Status bits.

8.8 Reset on Brown-out

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC16F526 devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-12 and Figure 8-13.

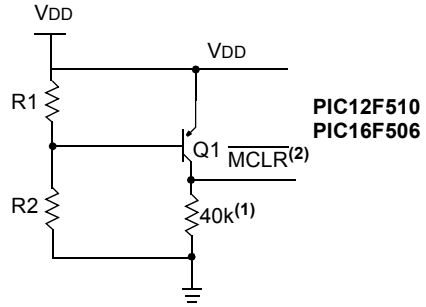
FIGURE 8-12: BROWN-OUT PROTECTION CIRCUIT 1



Note 1: This circuit will activate Reset when V_{DD} goes below Vz + 0.7V (where Vz = Zener voltage).

2: Pin must be configured as $\overline{MCLR}$.

FIGURE 8-13: BROWN-OUT PROTECTION CIRCUIT 2

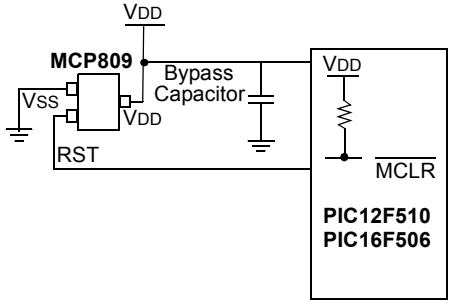


Note 1: This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when V_{DD} is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

2: Pin must be configured as $\overline{MCLR}$.

FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 3



Note: This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. There are 7 different trip point selections to accommodate 5V to 3V systems.

9.1.5 SLEEP

This ADC does not have a dedicated ADC clock, and therefore, no conversion in Sleep is possible. If a conversion is underway and a Sleep command is executed, the GO/$\overline{\text{DONE}}$ and ADON bit will be cleared. This will stop any conversion in process and power-down the ADC module to conserve power. Due to the nature of the conversion process, the ADRES may contain a partial conversion. At least 1 bit must have been converted prior to Sleep to have partial conversion data in ADRES. The ADCS and CHS bits are reset to their default condition; ANS<1:0> = 11 and CHS<1:0> = 11.

- For accurate conversions, TAD must meet the following:
- 500 ns < TAD < 50 μs
- TAD = 1/(FOSC/divisor)

Shaded areas indicate TAD out of range for accurate conversions. If analog input is desired at these frequencies, use INTOSC/8 for the ADC clock source.

TABLE 9-2: TAD FOR ADCS SETTINGS WITH VARIOUS OSCILLATORS

Source	ADCS <1:0>	Divisor	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz	500 kHz	350 kHz	200 kHz	100 kHz	32 kHz
INTOSC	11	4	—	—	.5 μs	1 μs	—	—	—	—	—	—
FOSC	10	4	.2 μs	.25 μs	.5 μs	1 μs	4 μs	8 μs	11 μs	20 μs	40 μs	125 μs
FOSC	01	8	.4 μs	.5 μs	1 μs	2 μs	8 μs	16 μs	23 μs	40 μs	80 μs	250 μs
FOSC	00	16	.8 μs	1 μs	2 μs	4 μs	16 μs	32 μs	46 μs	80 μs	160 μs	500 μs

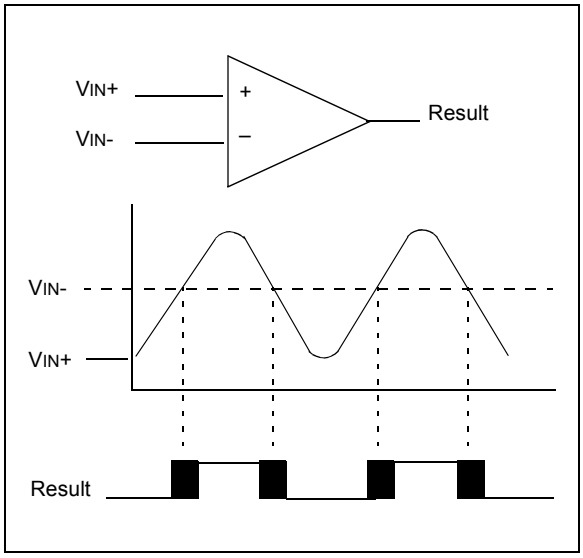
TABLE 9-3: EFFECTS OF SLEEP ON ADCON0

	ANS1	ANS0	ADCS1	ADCS0	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
Entering Sleep	Unchanged	Unchanged	1	1	1	1	0	0
Wake or Reset	1	1	1	1	1	1	0	0

10.1 Comparator Operation

A single comparator is shown in Figure 10-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. The shaded area of the output of the comparator in Figure 10-2 represent the uncertainty due to input offsets and response time. See Table 14-2 for Common Mode Voltage.

FIGURE 10-2: SINGLE COMPARATOR



10.2 Comparator Reference

An internal reference signal may be used depending on the comparator operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 10-2). Please see **Section 11.0 "Comparator Voltage Reference Module"** for internal reference specifications.

10.3 Comparator Response Time

Response time is the minimum time after selecting a new reference voltage or input source before the comparator output is to have a valid level. If the comparator inputs are changed, a delay must be used to allow the comparator to settle to its new state. Please see Table 14-3 for comparator response time specifications.

10.4 Comparator Output

The comparator output is read through the CM1CON0 or CM2CON0 register. This bit is read-only. The comparator output may also be used externally, see Figure 10-1.

Note:	Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

10.5 Comparator Wake-up Flag

The Comparator Wake-up Flag is set whenever all of the following conditions are met:

- $\overline{C1WU}$ = 0 (CM1CON0<0>) or $\overline{C2WU}$ = 0 (CM2CON0<0>)
- CM1CON0 or CM2CON0 has been read to latch the last known state of the C1OUT and C2OUT bit (`MOVF CM1CON0,W`)
- Device is in Sleep
- The output of a comparator has changed state

The wake-up flag may be cleared in software or by another device Reset.

10.6 Comparator Operation During Sleep

When the comparator is enabled it is active. To minimize power consumption while in Sleep mode, turn off the comparator before entering Sleep.

10.7 Effects of Reset

A Power-on Reset (POR) forces the CM2CON0 register to its Reset state. This forces the Comparator input pins to analog Reset mode. Device current is minimized when analog inputs are present at Reset time.

10.8 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 10-3. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

13.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

13.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

13.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

13.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

TABLE 14-2: COMPARATOR SPECIFICATIONS.

Comparator Specifications	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to 125°C					
Characteristics	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
Internal Voltage Reference	VIVRF	0.50	0.60	0.70	V	
Input offset voltage	VOS	—	± 5.0	± 10	mV	
Input common mode voltage*	VCM	0	—	VDD – 1.5	V	
CMRR*	CMRR	55	—	—	db	
Response Time(1)*	TRT	—	150	400	ns	
Comparator Mode Change to Output Valid*	TMC2COV	—	—	10	µs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2 while the other input transitions from VSS to VDD – 1.5V.

TABLE 14-3: COMPARATOR VOLTAGE REFERENCE (VREF) SPECIFICATIONS

Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
CVRES	Resolution	— —	VDD/24* VDD/32	— —	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
	Absolute Accuracy(2)	— —	— —	±1/2* ±1/2*	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
	Unit Resistor Value (R)	— —	2K*	—	Ω	
	Settling Time(1)	—	—	10*	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

2: Do not use reference externally when VDD < 2.7V. Under this condition, reference should only be used with comparator Voltage Common mode observed.

FIGURE 15-2: TYPICAL IDD vs. FOSC OVER VDD (XT, EXTRC mode)

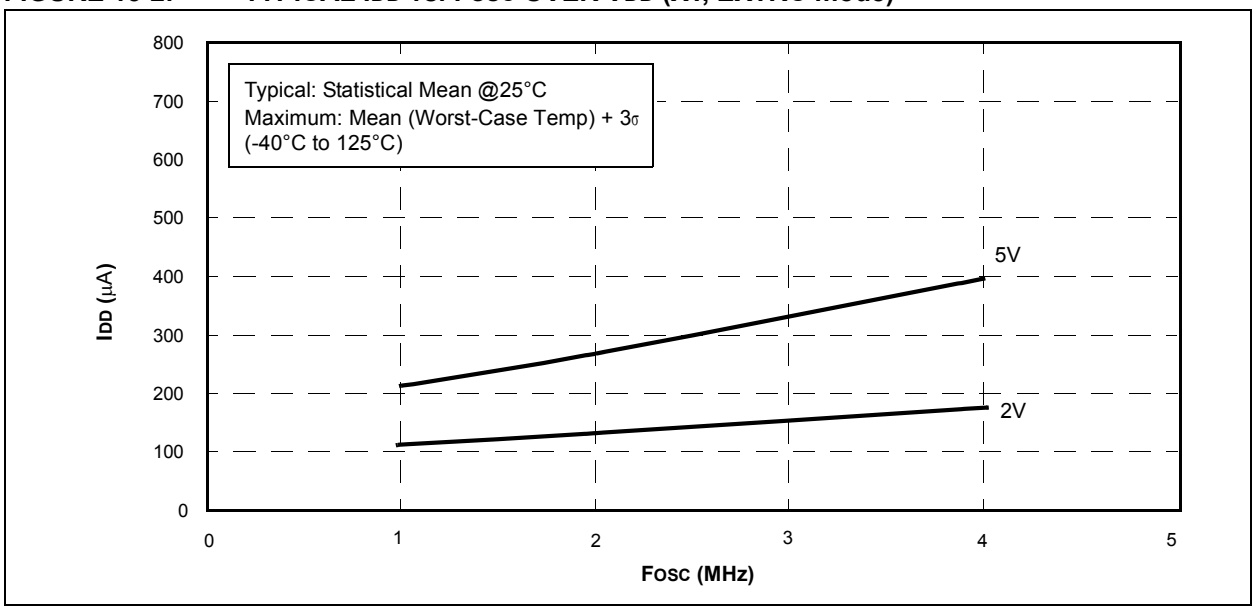


FIGURE 15-3: MAXIMUM IDD vs. FOSC OVER VDD (XT, EXTRC mode)

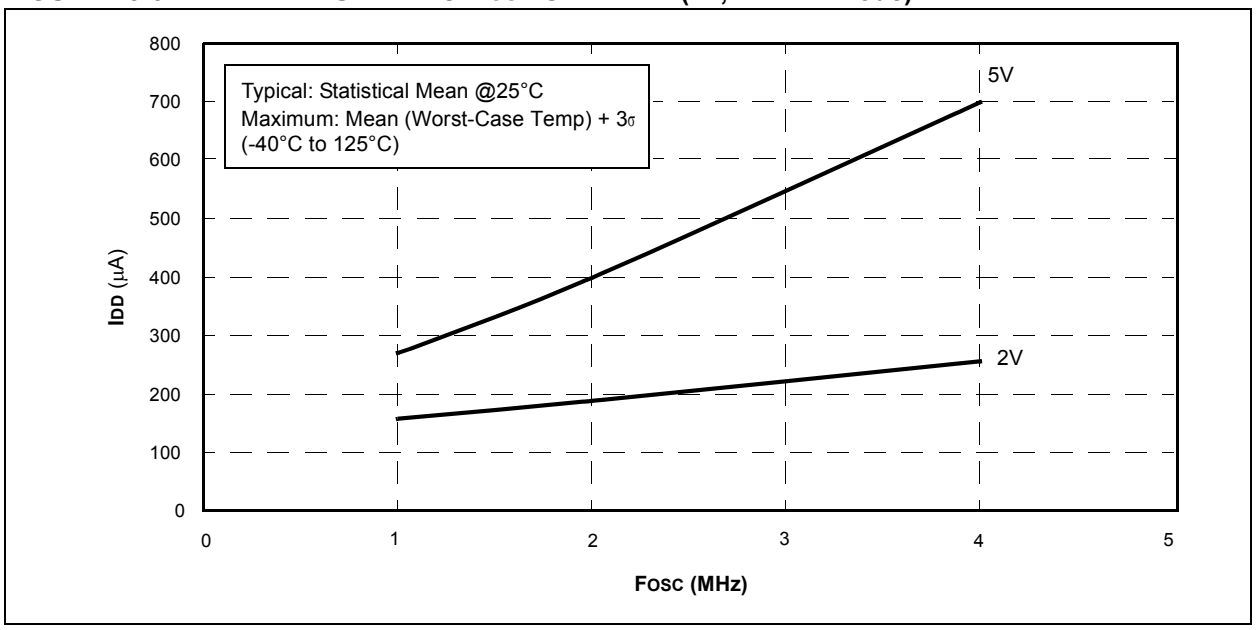


FIGURE 15-4: IDD vs. VDD OVER FOSC (LP MODE)

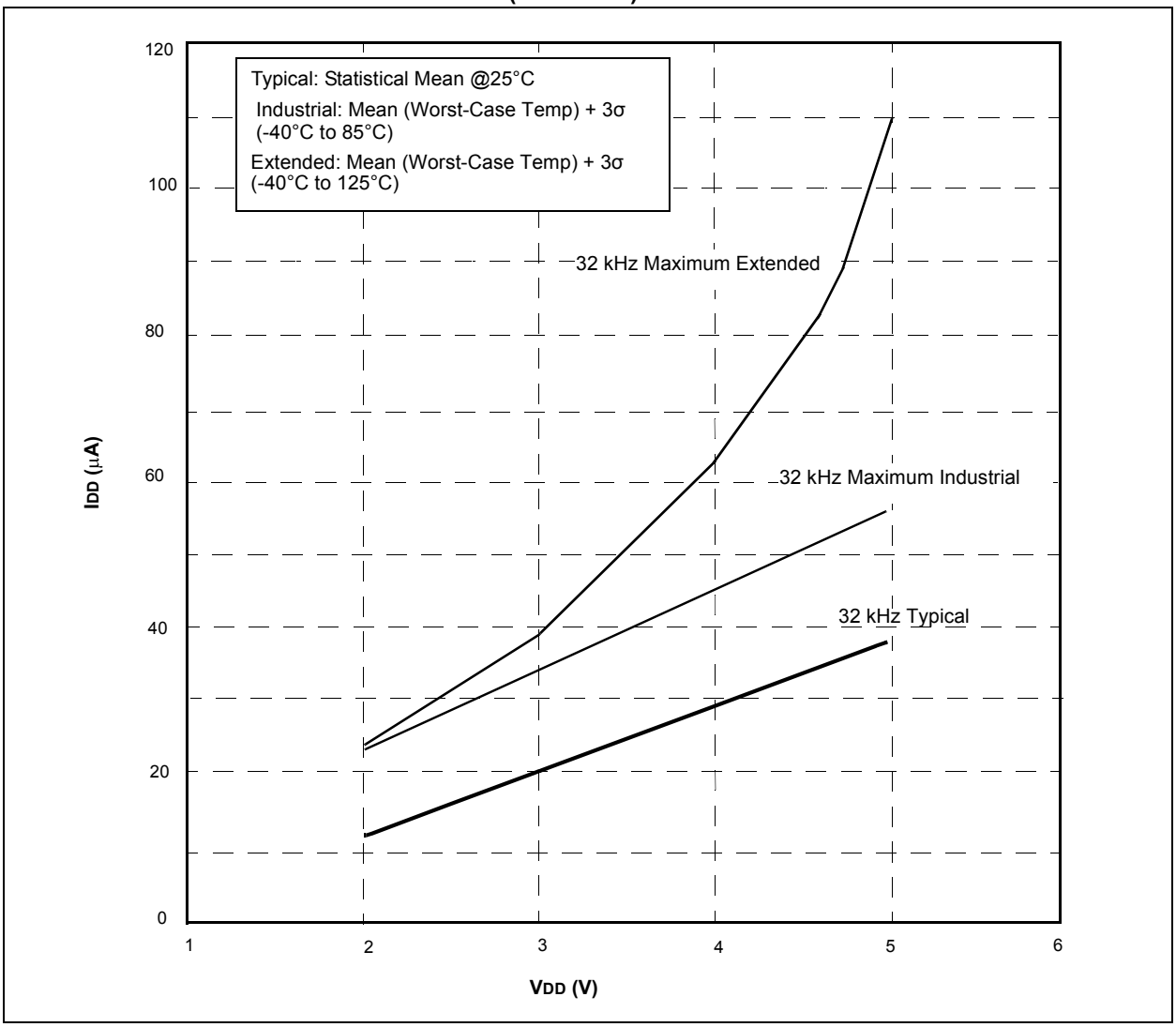


FIGURE 15-15: TTL INPUT THRESHOLD VIN vs. VDD

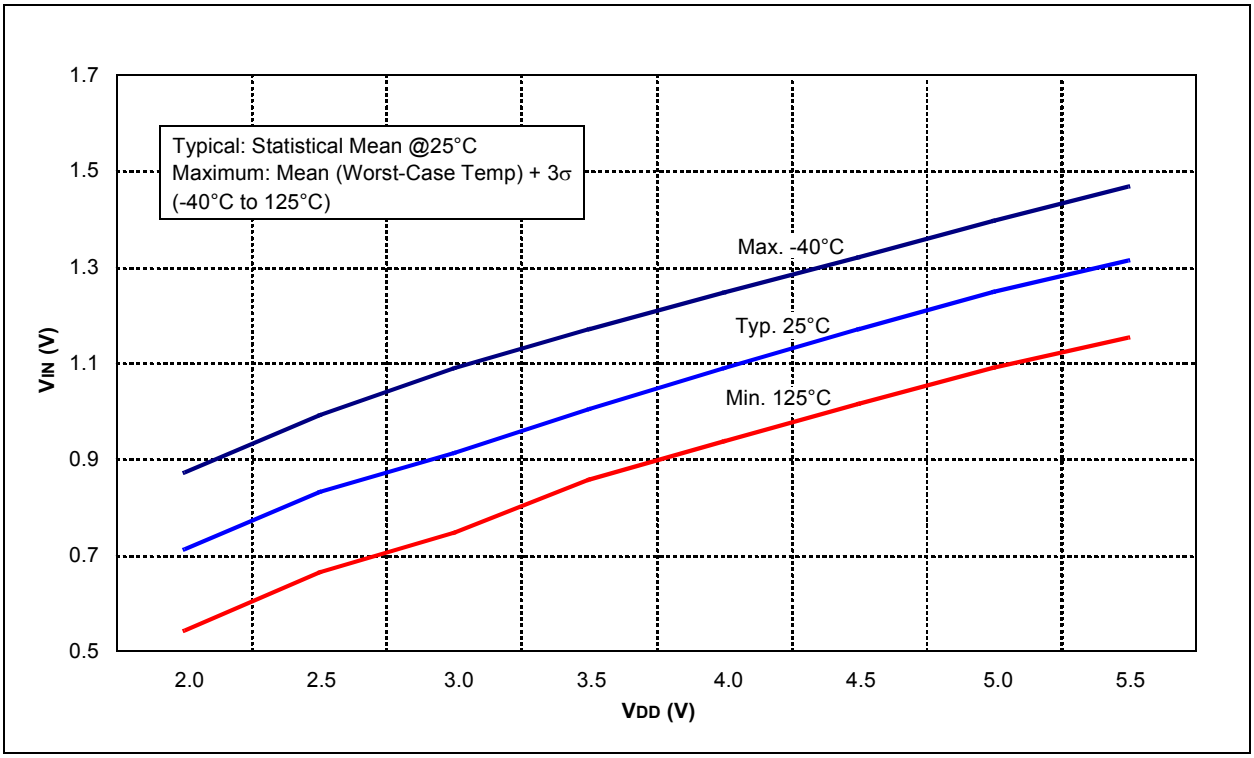
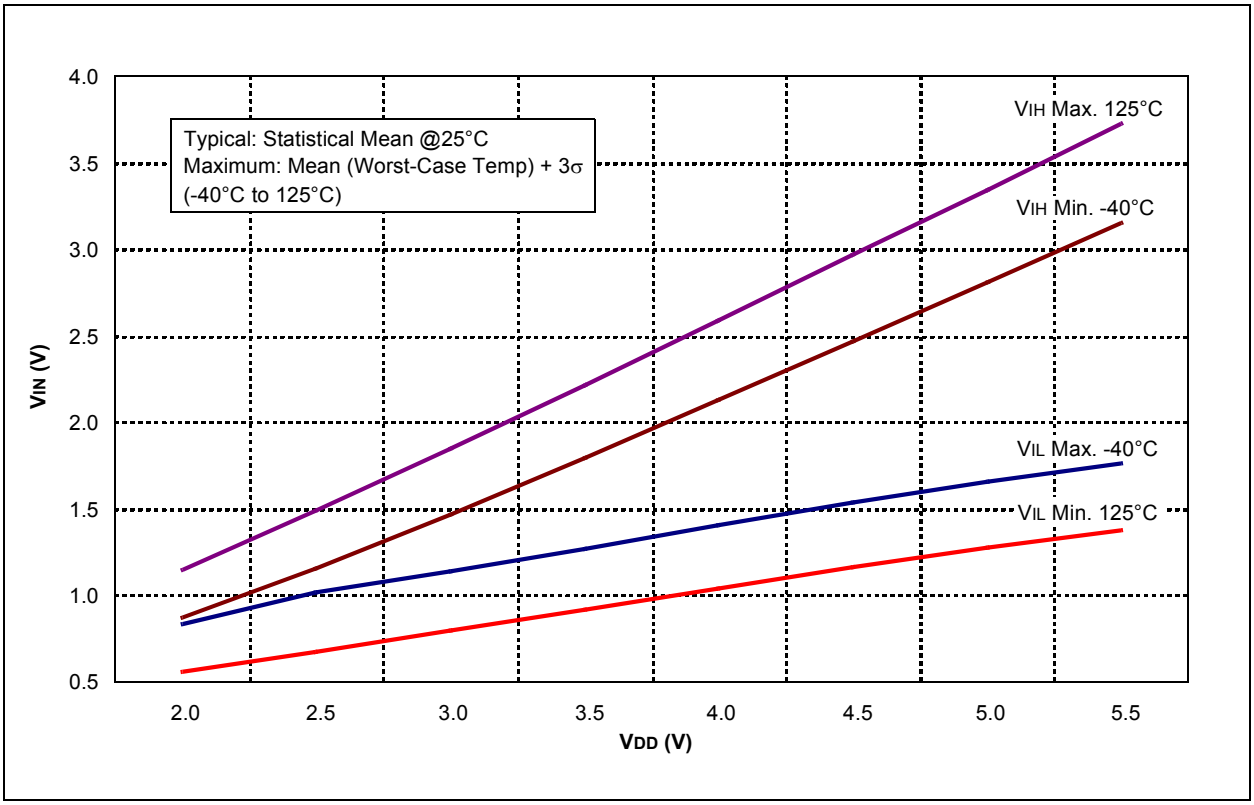
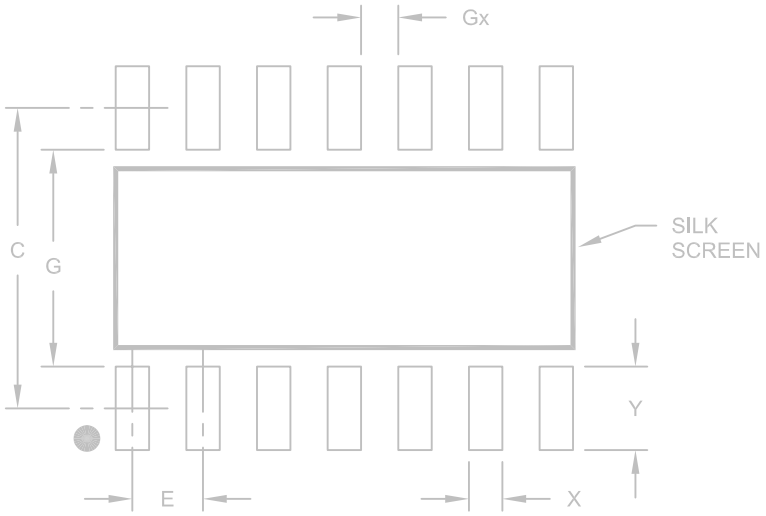


FIGURE 15-16: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD



14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

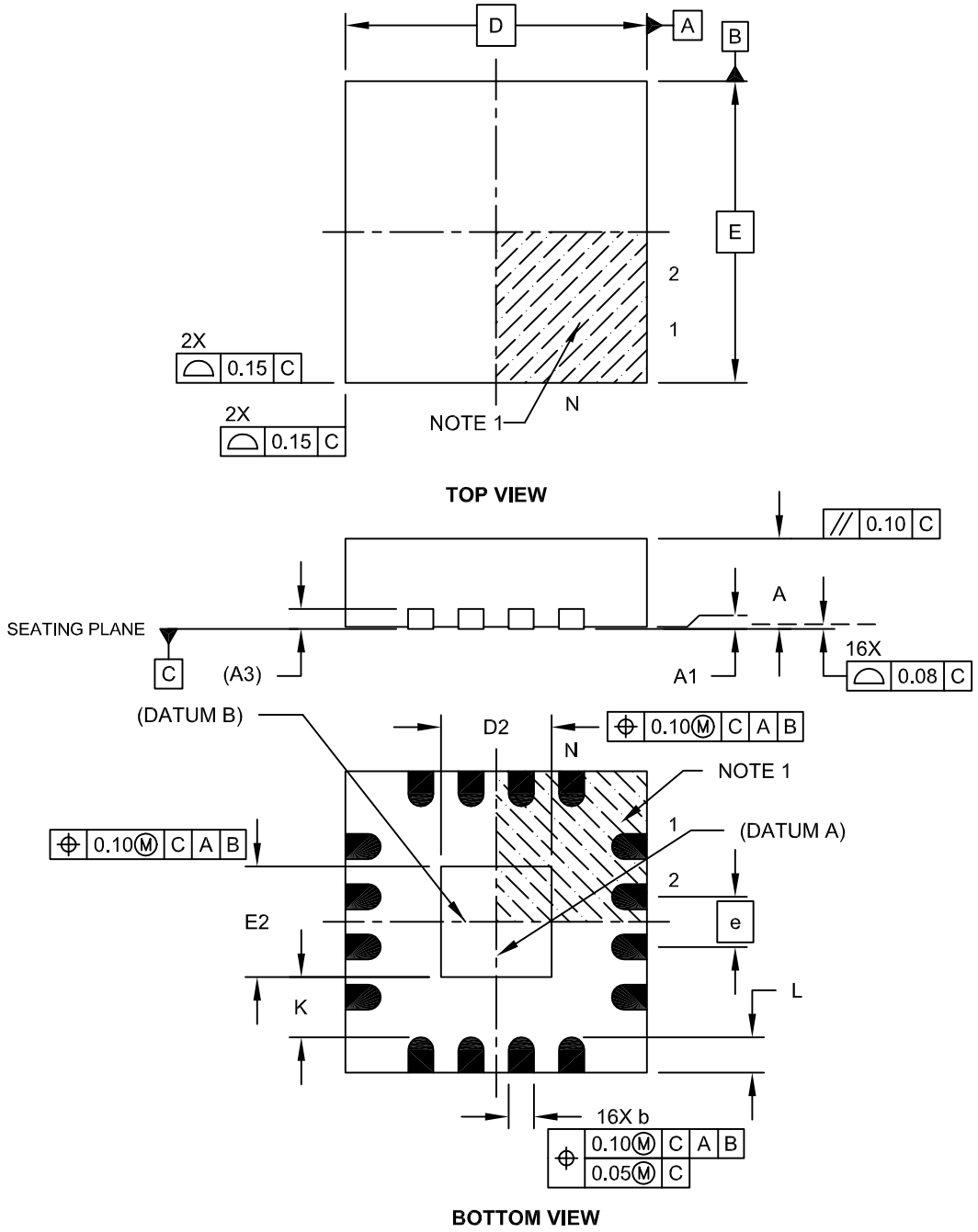
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-142A Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision A (August 2007)

Original release of this document.

Revision B (December 2008)

Added DC and AC Characteristics graphs; Updated Electrical Characteristics section; added I/O diagrams; updated the Flash Data Memory Control Section; made various changes to the Special Features of the CPU Section and made general edits. Miscellaneous updates.

Revision C (July 2009)

Removed “Preliminary” status; Revised Table 6-3: I/O Pins; Revised Table 8-3: Reset Conditions; Revised Table 14-4: A/D Converter Char.

Revision D (March 2010)

Added Package Drawings and Package Marking Information for the 16-Lead Package Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body (QFN); Updated the Product Identification System section.

Revision E (June 2010)

Revised Section 6 (I/O) Figures 6-1, 6-4 and 6-6.

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