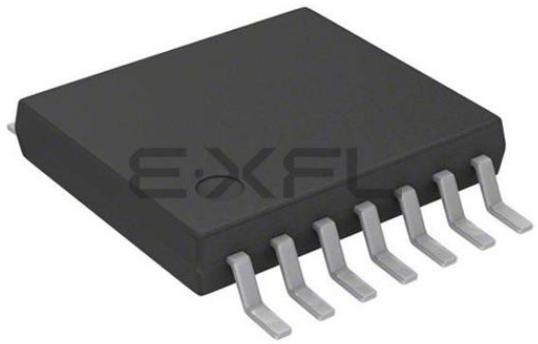


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	67 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 3x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f526-i-st

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16F526 device can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16F526 device uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architectures where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single-word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200 ns @ 20 MHz, 1 μs @ 4 MHz) except for program branches.

Table 3-1 below lists memory supported by the PIC16F526 device.

TABLE 3-1: PIC16F526 MEMORY

Device	Program Memory	Data Memory	
	Flash (words)	SRAM (bytes)	Flash (bytes)
PIC16F526	1024	67	64

The PIC16F526 device can directly or indirectly address its register files and data memory. All Special Function Registers (SFR), including the PC, are mapped in the data memory. The PIC16F526 device has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any Addressing mode. This symmetrical nature and lack of “special optimal situations” make programming with the PIC16F526 device simple, yet efficient. In addition, the learning curve is reduced significantly.

The PIC16F526 device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two’s complement in nature. In two-operand instructions, one operand is typically the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC) and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the `SUBWF` and `ADDWF` instructions for examples.

A simplified block diagram is shown in Figure 3-2, with the corresponding device pins described in Table 3-2.

TABLE 3-2: PIC16F526 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RB0//C1IN+/AN0/ ICSPDAT	RB0	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	C1IN+	AN	—	Comparator 1 input.
	AN0	AN	—	ADC channel input.
	ICSPDAT	ST	CMOS	ICSP™ mode Schmitt Trigger.
RB1/C1IN-/AN1/ ICSPCLK	RB1	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	C1IN-	AN	—	Comparator 1 input.
	AN1	AN	—	ADC channel input.
	ICSPCLK	ST	CMOS	ICSP mode Schmitt Trigger.
RB2/C1OUT/AN2	RB2	TTL	CMOS	Bidirectional I/O pin.
	C1OUT	—	CMOS	Comparator 1 output.
	AN2	AN	—	ADC channel input.
RB3/$\overline{\text{MCLR}}$/V_{PP}	RB3	TTL	—	Input pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear (Reset). When configured as $\overline{\text{MCLR}}$, this pin is an active-low Reset to the device. Voltage on $\overline{\text{MCLR}}$/V_{PP} must not exceed V_{DD} during normal device operation or the device will enter Programming mode. Weak pull-up always on if configured as $\overline{\text{MCLR}}$.
	V_{PP}	HV	—	Programming voltage input.
RB4/OSC2/CLKOUT	RB4	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	OSC2	—	XTAL	Oscillator crystal output. Connections to crystal or resonator in Crystal Oscillator mode (XT, HS and LP modes only, PORTB in other modes).
	CLKOUT	—	CMOS	EXTRC/INTRC CLKOUT pin (F_{OSC}/4).
RB5/OSC1/CLKIN	RB5	TTL	CMOS	Bidirectional I/O pin.
	OSC1	XTAL	—	Oscillator crystal input.
	CLKIN	ST	—	External clock source input.
RC0/C2IN+	RC0	TTL	CMOS	Bidirectional I/O port.
	C2IN+	AN	—	Comparator 2 input.
RC1/C2IN-	RC1	TTL	CMOS	Bidirectional I/O port.
	C2IN-	AN	—	Comparator 2 input.
RC2/CV_{REF}	RC2	TTL	CMOS	Bidirectional I/O port.
	CV_{REF}	—	AN	Programmable Voltage Reference output.
RC3	RC3	TTL	CMOS	Bidirectional I/O port.
RC4/C2OUT	RC4	TTL	CMOS	Bidirectional I/O port.
	C2OUT	—	CMOS	Comparator 2 output.
RC5/T0CKI	RC5	TTL	CMOS	Bidirectional I/O port.
	T0CKI	ST	—	Timer0 Schmitt Trigger input pin.
V_{DD}	V_{DD}	—	P	Positive supply for logic and I/O pins.
V_{SS}	V_{SS}	—	P	Ground reference for logic and I/O pins.

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, HV = High Voltage

4.0 MEMORY ORGANIZATION

The PIC16F526 memories are organized into program memory and data memory (SRAM).The self-writable portion of the program memory called Flash data memory is located at addresses at 400h-43Fh. All Program mode commands that work on the normal Flash memory work on the Flash data memory. This includes bulk erase, row/column/cycling toggles, Load and Read data commands (Refer to **Section 5.0 "Flash Data Memory Control"** for more details). For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one STATUS register bit. For the PIC16F526, with data memory register files of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Select Register (FSR).

4.1 Program Memory Organization for the PIC16F526

The PIC16F526 device has an 11-bit Program Counter (PC) capable of addressing a 2K x 12 program memory space. Program memory is partitioned into user memory, data memory and configuration memory spaces.

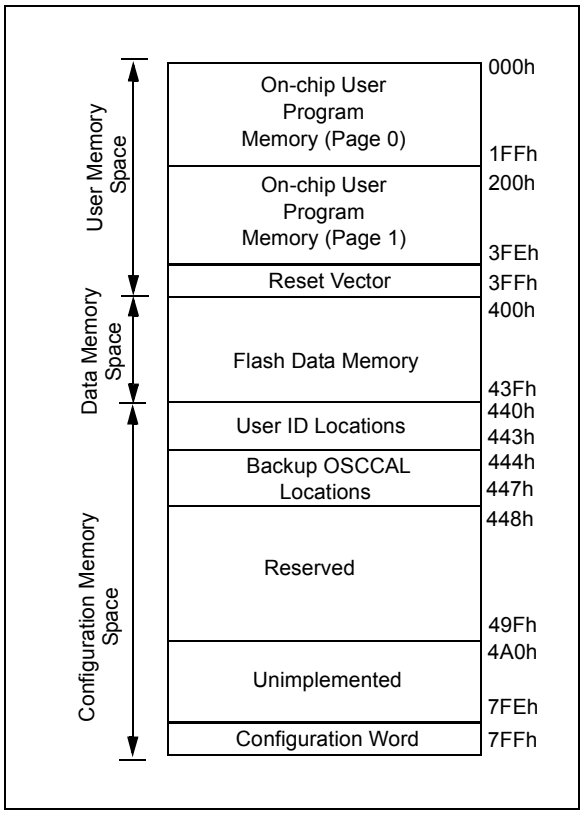
The user memory space is the on-chip user program memory. As shown in Figure 4-1, it extends from 0x000 to 0x3FF and partitions into pages, including Reset vector at address 0x3FF.

The data memory space is the Flash data memory block and is located at addresses PC = 400h-43Fh. All Program mode commands that work on the normal Flash memory work on the Flash data memory block. This includes bulk erase, Load and Read data commands.

The configuration memory space extends from 0x440 to 0x7FF. Locations from 0x448 through 0x49F are reserved. The user ID locations extend from 0x440 through 0x443. The Backup OSCCAL locations extend from 0x444 through 0x447. The Configuration Word is physically located at 0x7FF.

Refer to "*PIC16F526 Memory Programming Specification*" (DS41317) for more details.

FIGURE 4-1: MEMORY MAP



REGISTER 5-3: EECON: FLASH CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:			
S = Bit can only be set			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'.

bit 4 **FREE:** Flash Data Memory Row Erase Enable Bit
- 1 = Program memory row being pointed to by EEADR will be erased on the next write cycle. No write will be performed. This bit is cleared at the completion of the erase operation.
- 0 = Perform write only

bit 3 **WRERR:** Write Error Flag bit
- 1 = A write operation terminated prematurely (by device Reset)
- 0 = Write operation completed successfully

bit 2 **WREN:** Write Enable bit
- 1 = Allows write cycle to Flash data memory
- 0 = Inhibits write cycle to Flash data memory

bit 1 **WR:** Write Control bit
- 1 = Initiate a erase or write cycle
- 0 = Write/Erase cycle is complete

bit 0 **RD:** Read Control bit
- 1 = Initiate a read of Flash data memory
- 0 = Do not read Flash data memory

5.4 Code Protection

Code protection does not prevent the CPU from performing read or write operations on the Flash data memory. Refer to the code protection chapter for more information.

NOTES:

REGISTER 6-2: PORTC: PORTC REGISTER

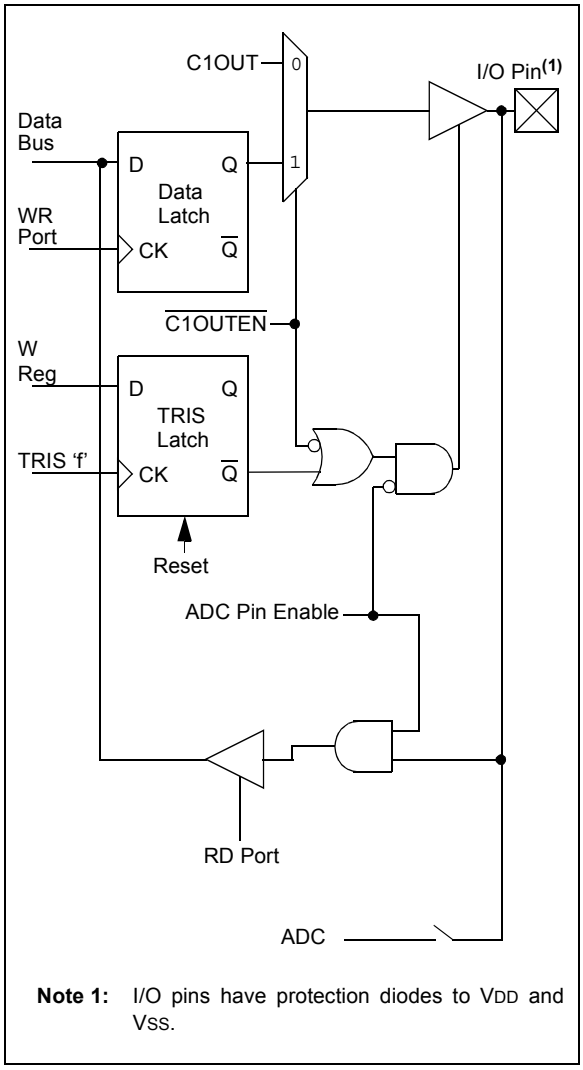
U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

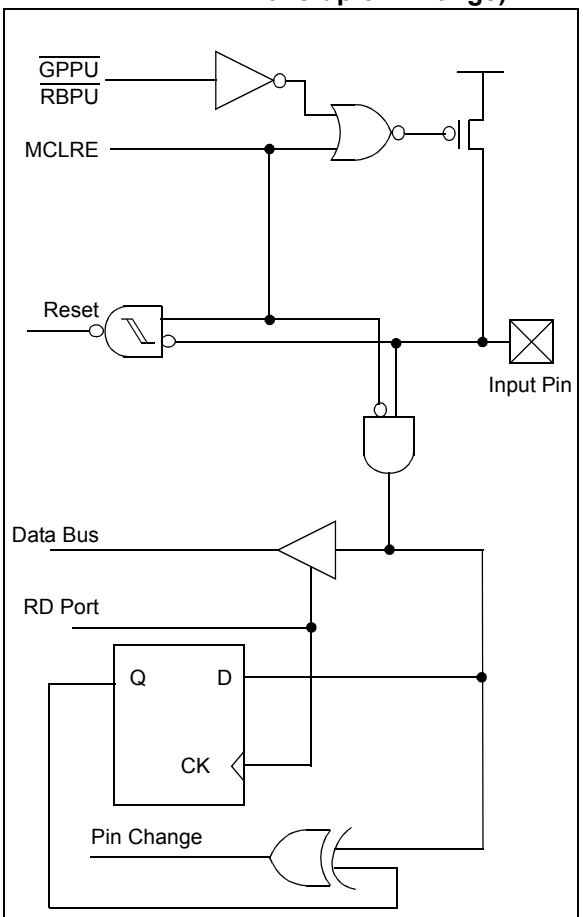
bit 5-0 **RC<5:0>**: PORTC I/O Pin bits
1 = Port pin is >VIH min.
0 = Port pin is <VIL max.

FIGURE 6-2: BLOCK DIAGRAM OF RB2



Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 6-3: BLOCK DIAGRAM OF RB3 (with Weak Pull-up and Wake-up on Change)



Note 1: RB3/MCLR pin has a protection diode to VSS only.

REGISTER 8-1: CONFIG: CONFIGURATION WORD REGISTER

$\overline{CPDF}$	IOSCFS	MCLRE	$\overline{CP}$	WDTE	FOSC2	FOSC1	FOSC0
bit 7							bit 0

bit 7 **$\overline{CPDF}$:** Code Protection bit – Flash Data Memory
1 = Code protection off
0 = Code protection on

bit 6 **IOSCFS:** Internal Oscillator Frequency Select bit
1 = 8 MHz INTOSC frequency
0 = 4 MHz INTOSC frequency

bit 5 **MCLRE:** Master Clear Enable bit
1 = RB3/$\overline{MCLR}$ pin functions as $\overline{MCLR}$
0 = RB3/$\overline{MCLR}$ pin functions as RB3, $\overline{MCLR}$ internally tied to VDD

bit 4 **$\overline{CP}$:** Code Protection bit – User Program Memory
1 = Code protection off
0 = Code protection on

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
000 = LP oscillator and 18 ms DRT
001 = XT oscillator and 18 ms DRT
010 = HS oscillator and 18 ms DRT
011 = EC oscillator with RB4 function on RB4/OSC2/CLKOUT and 1 ms DRT(1)
100 = INTRC with RB4 function on RB4/OSC2/CLKOUT and 1 ms DRT(1)
101 = INTRC with CLKOUT function on RB4/OSC2/CLKOUT and 1 ms DRT(1)
110 = EXTRC with RB4 function on RB4/OSC2/CLKOUT and 1 ms DRT(1)
111 = EXTRC with CLKOUT function on RB4/OSC2/CLKOUT and 1 ms DRT(1)

Note 1: Refer to the "*PIC16F526 Memory Programming Specification*", DS41317 to determine how to access the Configuration Word.

2: DRT length (18 ms or 1 ms) is a function of Clock mode selection. It is the responsibility of the application designer to ensure the use of either 18 ms (nominal) DRT or the 1 ms (nominal) DRT will result in acceptable operation. Refer to **Section 14.1 "DC Characteristics: PIC16F526 (Industrial)"** and **Section 14.2 "DC Characteristics: PIC16F526 (Extended)"** for VDD rise time and stability requirements for this mode of operation.

TABLE 8-4: RESET CONDITION FOR SPECIAL REGISTERS

	STATUS Addr: 03h
Power-on Reset	0001 1xxx
$\overline{\text{MCLR}}$ Reset during normal operation	000u uuuu
$\overline{\text{MCLR}}$ Reset during Sleep	0001 0uuu
WDT Reset during Sleep	0000 0uuu
WDT Reset normal operation	0000 uuuu
Wake-up from Sleep on pin change	1001 0uuu
Wake-up from Sleep on comparator change	0101 0uuu

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as '0'.

NOTES:

FIGURE 11-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

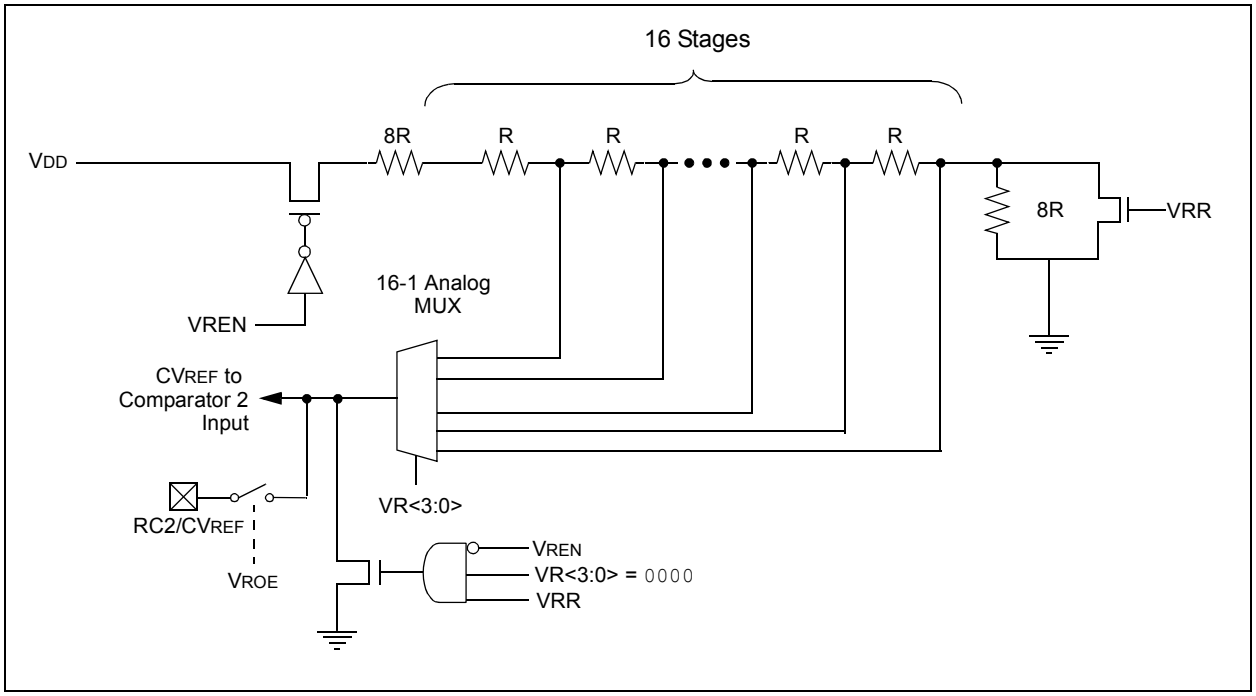


TABLE 11-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	001- 1111	uuu- uuuu
CM1CON0	C1OUT	$\overline{\text{C1OUTEN}}$	C1POL	$\overline{\text{C1T0CS}}$	C1ON	C1NREF	C1PREF	$\overline{\text{C1WU}}$	q111 1111	quuu uuuu
CM2CON0	C2OUT	$\overline{\text{C2OUTEN}}$	C2POL	C2PREF2	C2ON	C2NREF	C2PREF1	$\overline{\text{C2WU}}$	q111 1111	quuu uuuu

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0', q = value depends on condition.

BTFSS **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: $0 \le f \le 31$
$0 \le b < 7$

Operation: skip if (f<b>) = 1

Status Affected: None

Description: If bit 'b' in register 'f' is '1', then the next instruction is skipped.
If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.

CALL **Subroutine Call**

Syntax: [*label*] CALL k

Operands: $0 \le k \le 255$

Operation: (PC) + 1→ Top-of-Stack;
k → PC<7:0>;
(STATUS<6:5>) → PC<10:9>;
0 → PC<8>

Status Affected: None

Description: Subroutine call. First, return address (PC + 1) is PUSHed onto the stack. The eight-bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two-cycle instruction.

CLRF **Clear f**

Syntax: [*label*] CLRF f

Operands: $0 \le f \le 31$

Operation: 00h → (f);
1 → Z

Status Affected: Z

Description: The contents of register 'f' are cleared and the Z bit is set.

CLRW **Clear W**

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W);
1 → Z

Status Affected: Z

Description: The W register is cleared. Zero bit (Z) is set.

CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler (if assigned);
1 → $\overline{TO}$;
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow$ (dest)

Status Affected: Z

Description: The contents of register 'f' are complemented. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

DECF	Decrement f
Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) – 1 → (dest)
Status Affected:	Z
Description:	Decrement register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) – 1 → d; skip if result = 0
Status Affected:	None
Description:	The contents of register ‘f’ are decremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. If the result is ‘0’, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 511$
Operation:	k → PC<8:0>; STATUS<6:5> → PC<10:9>
Status Affected:	None
Description:	GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) + 1 → (dest)
Status Affected:	Z
Description:	The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) + 1 → (dest), skip if result = 0
Status Affected:	None
Description:	The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. If the result is ‘0’, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

IORLW	Inclusive OR literal with W
Syntax:	[*label*] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. (k) → (W)
Status Affected:	Z
Description:	The contents of the W register are OR’ed with the eight-bit literal ‘k’. The result is placed in the W register.

13.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

13.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

13.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

TABLE 14-2: COMPARATOR SPECIFICATIONS.

Comparator Specifications	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to 125°C					
Characteristics	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
Internal Voltage Reference	VIVRF	0.50	0.60	0.70	V	
Input offset voltage	VOS	—	± 5.0	± 10	mV	
Input common mode voltage*	VCM	0	—	VDD – 1.5	V	
CMRR*	CMRR	55	—	—	db	
Response Time(1)*	TRT	—	150	400	ns	
Comparator Mode Change to Output Valid*	TMC2COV	—	—	10	µs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2 while the other input transitions from VSS to VDD – 1.5V.

TABLE 14-3: COMPARATOR VOLTAGE REFERENCE (VREF) SPECIFICATIONS

Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
CVRES	Resolution	— —	VDD/24* VDD/32	— —	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
	Absolute Accuracy(2)	— —	— —	±1/2* ±1/2*	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
	Unit Resistor Value (R)	— —	2K*	—	Ω	
	Settling Time(1)	—	—	10*	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

2: Do not use reference externally when VDD < 2.7V. Under this condition, reference should only be used with comparator Voltage Common mode observed.

TABLE 14-4: A/D CONVERTER CHARACTERISTICS:

A/D Converter Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
A01	NR	Resolution	—	—	8	bit	
A03	EINL	Integral Error	—	—	±1.5	LSb	VDD = 5.0V
A04	EDNL	Differential Error	—	—	-1< EDNL ≤1.7	LSb	No missing codes to 8 bits VDD = 5.0V
A06	EOFF	Offset Error	—	—	±1.5	LSb	VDD = 5.0V
A07	EGN	Gain Error	-0.7	—	+2.2	LSb	VDD = 5.0V
A10	—	Monotonicity	—	guaranteed(1)	—	—	VSS ≤ VAIN ≤ VDD
A25	VAIN	Analog Input Voltage	VSS	—	VDD	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	KΩ	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

TABLE 14-5: PULL-UP RESISTOR RANGES

VDD (Volts)	Temperature (°C)	Min.	Typ.	Max.	Units
RB0/RB1/RB4					
2.0	-40	73K	105K	186K	Ω
	25	73K	113K	187K	Ω
	85	82K	123K	190K	Ω
	125	86K	132k	190K	Ω
5.5	-40	15K	21K	33K	Ω
	25	15K	22K	34K	Ω
	85	19K	26k	35K	Ω
	125	23K	29K	35K	Ω
RB3					
2.0	-40	63K	81K	96K	Ω
	25	77K	93K	116K	Ω
	85	82K	96k	116K	Ω
	125	86K	100K	119K	Ω
5.5	-40	16K	20k	22K	Ω
	25	16K	21K	23K	Ω
	85	24K	25k	28K	Ω
	125	26K	27K	29K	Ω

14.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

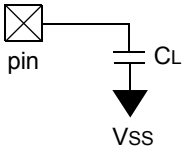
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	Oscillator
cy	Cycle time	os	OSC1
drt	Device Reset Timer	t0	T0CKI
io	I/O port	wdt	Watchdog Timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (high-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 14-3: LOAD CONDITIONS



Legend:

C_L = 50 pF for all pins except OSC2

15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

FIGURE 15-11: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)

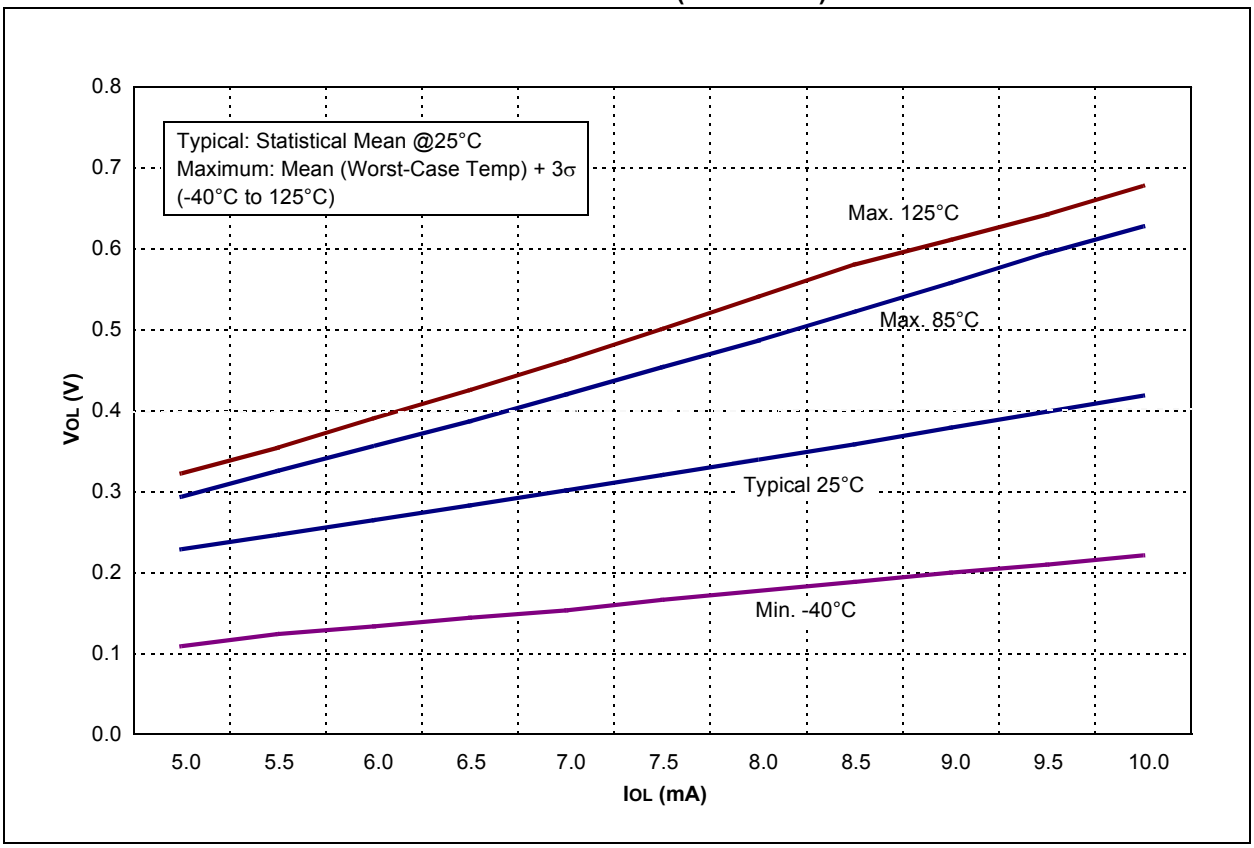
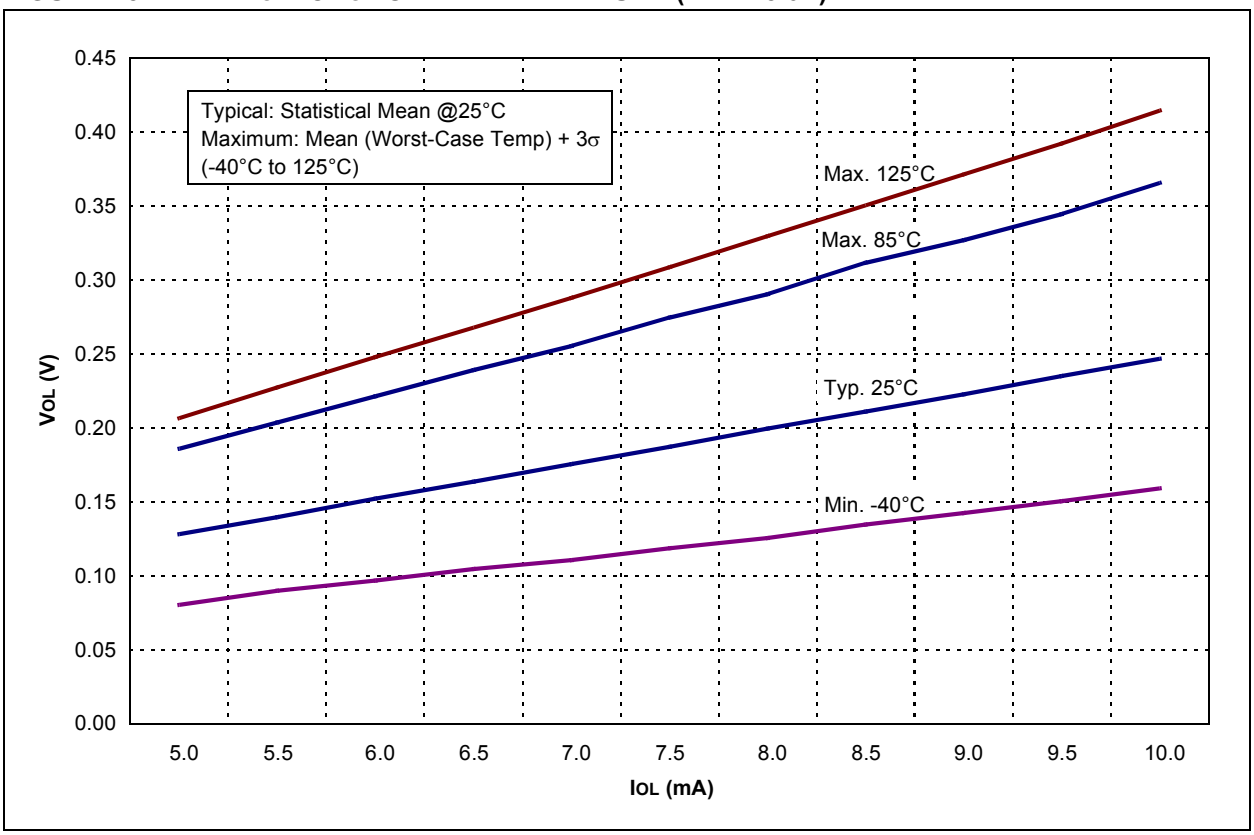
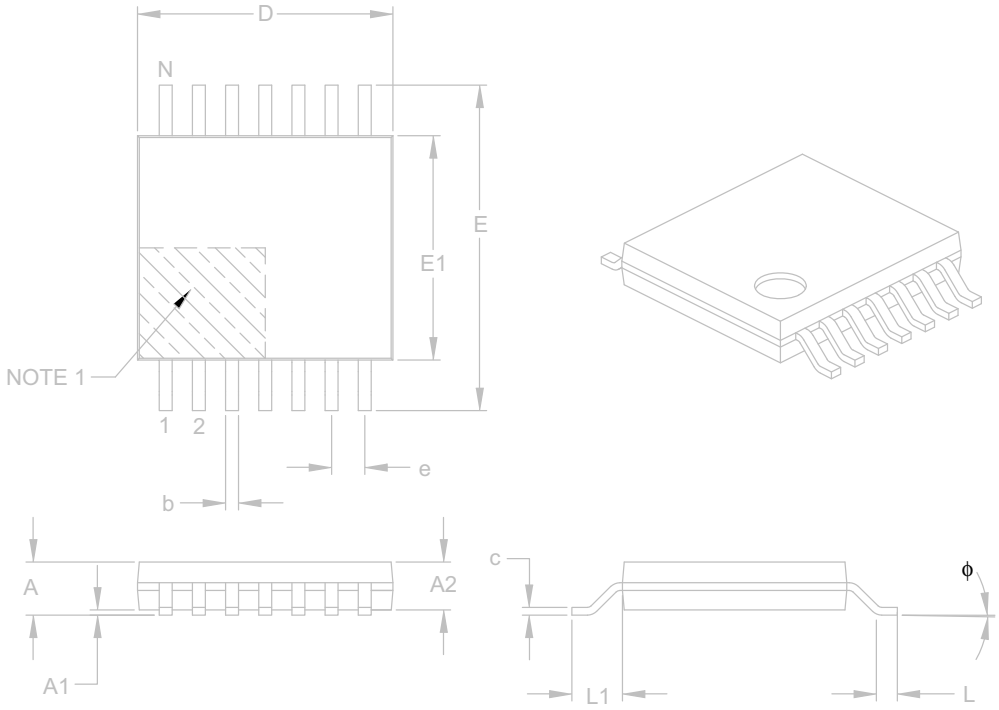


FIGURE 15-12: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)



14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

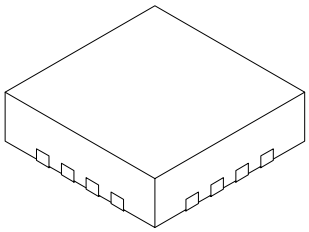
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.00	1.10	1.50
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.00	1.10	1.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.25	0.35	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-142A Sheet 2 of 2