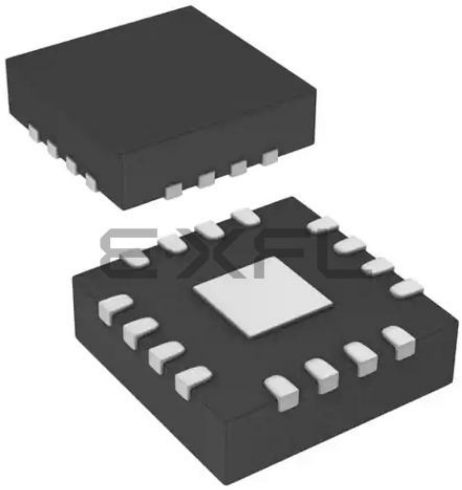

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	67 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 3x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VFQFN Exposed Pad
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f526t-i-mg

14-Pin, 8-Bit Flash Microcontroller

High-Performance RISC CPU:

- Only 33 Single-Word Instructions
- All Single-Cycle Instructions except for Program Branches which are Two-Cycle
- Two-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- Operating Speed:
  - DC – 20 MHz crystal oscillator
  - DC – 200 ns instruction cycle
- On-chip Flash Program Memory:
  - 1024 x 12
- General Purpose Registers (SRAM):
  - 67 x 8
- Flash Data Memory:
  - 64 x 8

Special Microcontroller Features:

- 8 MHz Precision Internal Oscillator:
  - Factory calibrated to ±1%
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debugging (ICD) Support
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed $\overline{\text{MCLR}}$ Input Pin
- Internal Weak Pull-ups on I/O Pins
- Power-Saving Sleep mode
- Wake-Up from Sleep on Pin Change
- Selectable Oscillator Options:
  - INTRC: 4 MHz or 8 MHz precision Internal RC oscillator
  - EXTRC: External low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power-saving, low-frequency crystal
  - EC: High-speed external clock input

Low-Power Features/CMOS Technology:

- Standby current:
  - 100 nA @ 2.0V, typical
- Operating current:
  - 11 μA @ 32 kHz, 2.0V, typical
  - 175 μA @ 4 MHz, 2.0V, typical
- Watchdog Timer current:
  - 1 μA @ 2.0V, typical
  - 7 μA @ 5.0V, typical
- High Endurance Program and Flash Data Memory cells:
  - 100,000 write Program Memory endurance
  - 1,000,000 write Flash Data Memory endurance
  - Program and Flash Data retention: >40 years
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V:
  - Wide temperature range
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

Peripheral Features:

- 12 I/O Pins:
  - 11 I/O pins with individual direction control
  - 1 input-only pin
  - High current sink/source for direct LED drive
  - Wake-up on change
  - Weak pull-ups
- 8-bit Real-time Clock/Counter (TMR0) with 8-bit Programmable Prescaler
- Two Analog Comparators:
  - Comparator inputs and output accessible externally
  - One comparator with 0.6V fixed on-chip absolute voltage reference (V_{REF})
  - One comparator with programmable on-chip voltage reference (V_{REF})
- Analog-to-Digital (A/D) Converter:
  - 8-bit resolution
  - 3-channel external programmable inputs
  - 1-channel internal input to internal absolute 0.6 voltage reference

Device	Program Memory	Data Memory		I/O	Comparators	Timers 8-bit	8-bit A/D Channels
	Flash (words)	SRAM (bytes)	Flash (bytes)				
PIC16F526	1024	67	64	12	2	1	3

NOTES:

TABLE 3-2: PIC16F526 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RB0//C1IN+/AN0/ ICSPDAT	RB0	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	C1IN+	AN	—	Comparator 1 input.
	AN0	AN	—	ADC channel input.
	ICSPDAT	ST	CMOS	ICSP™ mode Schmitt Trigger.
RB1/C1IN-/AN1/ ICSPCLK	RB1	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	C1IN-	AN	—	Comparator 1 input.
	AN1	AN	—	ADC channel input.
	ICSPCLK	ST	CMOS	ICSP mode Schmitt Trigger.
RB2/C1OUT/AN2	RB2	TTL	CMOS	Bidirectional I/O pin.
	C1OUT	—	CMOS	Comparator 1 output.
	AN2	AN	—	ADC channel input.
RB3/$\overline{\text{MCLR}}$/VPP	RB3	TTL	—	Input pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear (Reset). When configured as $\overline{\text{MCLR}}$, this pin is an active-low Reset to the device. Voltage on $\overline{\text{MCLR}}$/VPP must not exceed VDD during normal device operation or the device will enter Programming mode. Weak pull-up always on if configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Programming voltage input.
RB4/OSC2/CLKOUT	RB4	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	OSC2	—	XTAL	Oscillator crystal output. Connections to crystal or resonator in Crystal Oscillator mode (XT, HS and LP modes only, PORTB in other modes).
	CLKOUT	—	CMOS	EXTRC/INTRC CLKOUT pin (FOSC/4).
RB5/OSC1/CLKIN	RB5	TTL	CMOS	Bidirectional I/O pin.
	OSC1	XTAL	—	Oscillator crystal input.
	CLKIN	ST	—	External clock source input.
RC0/C2IN+	RC0	TTL	CMOS	Bidirectional I/O port.
	C2IN+	AN	—	Comparator 2 input.
RC1/C2IN-	RC1	TTL	CMOS	Bidirectional I/O port.
	C2IN-	AN	—	Comparator 2 input.
RC2/CVREF	RC2	TTL	CMOS	Bidirectional I/O port.
	CVREF	—	AN	Programmable Voltage Reference output.
RC3	RC3	TTL	CMOS	Bidirectional I/O port.
RC4/C2OUT	RC4	TTL	CMOS	Bidirectional I/O port.
	C2OUT	—	CMOS	Comparator 2 output.
RC5/T0CKI	RC5	TTL	CMOS	Bidirectional I/O port.
	T0CKI	ST	—	Timer0 Schmitt Trigger input pin.
VDD	VDD	—	P	Positive supply for logic and I/O pins.
VSS	VSS	—	P	Ground reference for logic and I/O pins.

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, HV = High Voltage

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

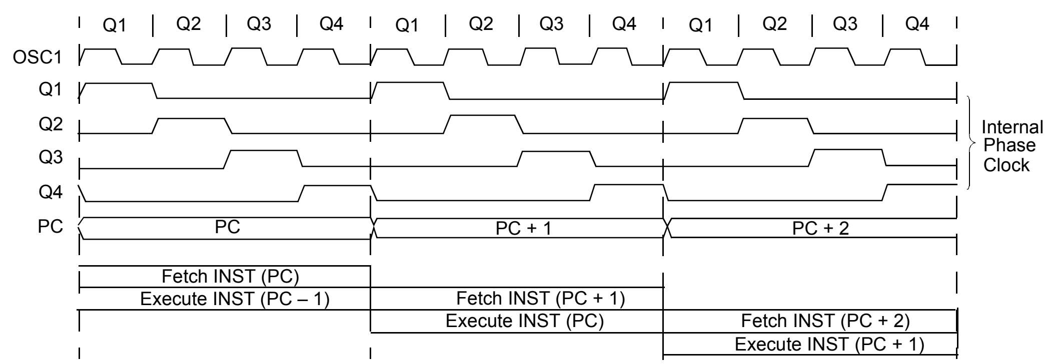
3.2 Instruction Flow/Pipelining

An instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the PC to change (e.g., `GOTO`), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the PC incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

1. `MOVLW 03H`	Fetch 1	Execute 1				
2. `MOVWF PORTB`		Fetch 2	Execute 2			
3. `CALL SUB_1`			Fetch 3	Execute 3		
4. `BSF PORTB, BIT1`				Fetch 4	Flush	
					Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles, since the fetch instruction is “flushed” from the pipeline, while the new instruction is being fetched and then executed.

5.2.2 WRITING TO FLASH DATA MEMORY

Once a cell is erased, new data can be written. Program execution is suspended during the write cycle. The following sequence must be performed for a single byte write.

1. Load EEADR with the address.
2. Load EEDATA with the data to write.
3. Set the WREN bit to enable write access to the array.
4. Set the WR bit to initiate the erase cycle.

If the WR bit is not set in the instruction cycle after the WREN bit is set, the WREN bit will be cleared in hardware.

Sample code that follows this procedure is included in Example 3.

EXAMPLE 3: WRITING A FLASH DATA MEMORY ROW

```
BANKSEL   EEADR
MOVLW     EE_ADR_WRITE     ; LOAD ADDRESS
MOVWF     EEADR            ;
MOVLW     EE_DATA_TO_WRITE ; LOAD DATA
MOVWF     EEDATA           ; INTO EEDATA REGISTER
BSF       EECON,WREN       ; ENABLE WRITES
BSF       EECON,WR         ; INITITATE ERASE
```

> **Note 1:** Only a series of BSF commands will work to enable the memory write sequence documented in Example 2. No other sequence of commands will work, no exceptions.
>
> **2:** For reads, erases and writes to the Flash data memory, there is no need to insert a `NOP` into the user code as is done on mid-range devices. The instruction immediately following the “`BSF EECON,WR/RD`” will be fetched and executed properly.

5.3 Write Verify

Depending on the application, good programming practice may dictate that data written to the Flash data memory be verified. Example 4 is an example of a write verify.

EXAMPLE 4: WRITE VERIFY OF FLASH DATA MEMORY

```
MOVF    EEDATA, W    ;EEDATA has not changed
                     ;from previous write
BSF     EECON, RD    ;Read the value written
XORWF   EEDATA, W    ;
BTFSS   STATUS, Z    ;Is data the same
GOTO    WRITE_ERR    ;No, handle error
                     ;Yes, continue
```

REGISTER 5-1: EEDATA: FLASH DATA REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EEDATA7	EEDATA6	EEDATA5	EEDATA4	EEDATA3	EEDATA2	EEDATA1	EEDATA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **EEDATA<7:0>**: 8-bits of data to be read from/written to data Flash

REGISTER 5-2: EEADR: FLASH ADDRESS REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’.

bit 5-0 **EEADR<5:0>**: 6-bits of data to be read from/written to data Flash

REGISTER 5-3: EECON: FLASH CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:			
S = Bit can only be set			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’.

bit 4 **FREE:** Flash Data Memory Row Erase Enable Bit
- 1 = Program memory row being pointed to by EEADR will be erased on the next write cycle. No write will be performed. This bit is cleared at the completion of the erase operation.
- 0 = Perform write only

bit 3 **WRERR:** Write Error Flag bit
- 1 = A write operation terminated prematurely (by device Reset)
- 0 = Write operation completed successfully

bit 2 **WREN:** Write Enable bit
- 1 = Allows write cycle to Flash data memory
- 0 = Inhibits write cycle to Flash data memory

bit 1 **WR:** Write Control bit
- 1 = Initiate a erase or write cycle
- 0 = Write/Erase cycle is complete

bit 0 **RD:** Read Control bit
- 1 = Initiate a read of Flash data memory
- 0 = Do not read Flash data memory

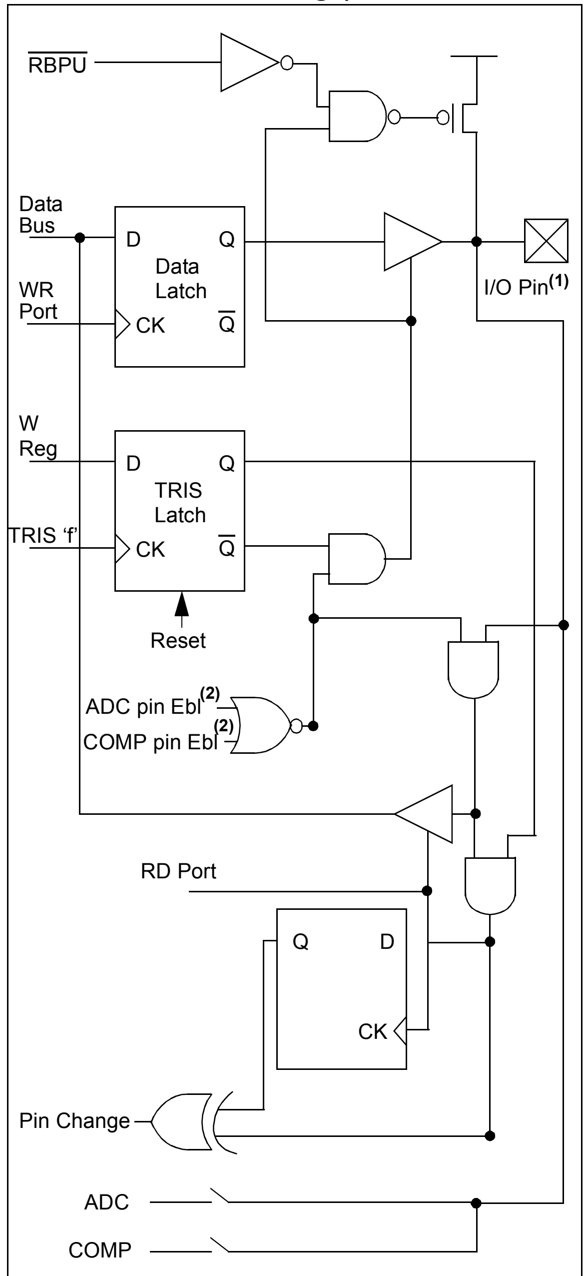
5.4 Code Protection

Code protection does not prevent the CPU from performing read or write operations on the Flash data memory. Refer to the code protection chapter for more information.

6.4 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 6-1. All port pins, except RB3 which is input-only, may be used for both input and output operations. For input operations, these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= `0`). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except RB3) can be programmed individually as input or output.

FIGURE 6-1: BLOCK DIAGRAM OF RB0 AND RB1 (with Weak Pull-up and Wake-up on Change)



Note 1: I/O pins have protection diodes to VDD and VSS.

2: Pin enabled as analog for ADC or comparator.

TABLE 6-2: SUMMARY OF PORT REGISTERS

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRIS	—	—	I/O Control Register (PORTB, PORTC)						--11 1111	--11 1111
N/A	OPTION	$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03h	STATUS	RBWUF	CWUF	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	qq0q quuu(1)
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: Shaded cells are not used by PORT registers, read as '0'. – = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

TABLE 6-3: I/O PINS ORDER OF PRECEDENCE

Priority	RB0	RB1	RB2	RB3	RC0	RC1	RC2	RC4	RC5
1	AN0	AN1	AN2	RB3/$\overline{\text{MCLR}}$	C2IN+	C2IN-	CVREF	C2OUT	T0CKI
2	C1IN+	C1IN-	C1OUT	—	TRISC	TRISC	TRISC	TRISC	TRISC
3	TRISB	TRISB	TRISB	—	—	—	—	—	—

6.5 I/O Programming Considerations

6.5.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The `BCF` and `BSF` instructions, for example, read the entire port into the CPU, execute the bit operation and rewrite the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a `BSF` operation on bit 5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit 5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit 0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 6-1 shows the effect of two sequential Read-Modify-Write instructions (e.g., `BCF`, `BSF`, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired OR", "wired AND"). The resulting high output currents may damage the chip.

EXAMPLE 6-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT(e.g. DSTEMP)

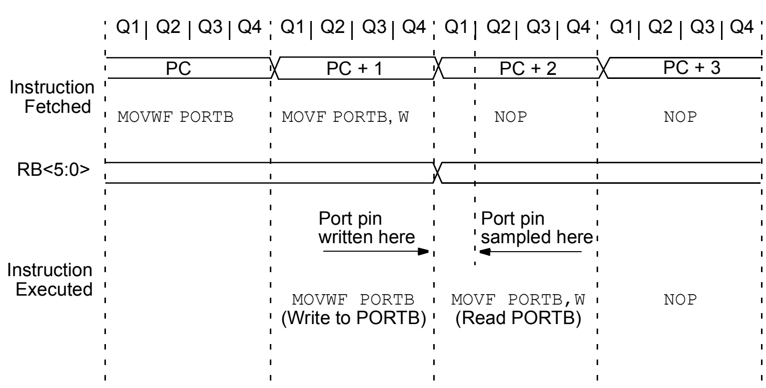
```
;Initial PORTB Settings
;PORTB<5:3> Inputs
;PORTB<2:0> Outputs
;
;                PORTB latch  PORTB pins
;                ----------   ----------
 BCF    PORTB, 5 ;--01 -ppp   --11 pppp
 BCF    PORTB, 4 ;--10 -ppp   --11 pppp
 MOVLW  007h;
 TRIS   PORTB    ;--10 -ppp   --11 pppp
;
```

Note 1: The user may have expected the pin values to be '`--00 pppp`'. The 2nd `BCF` caused RB5 to be latched as the pin value (High).

6.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 6-11). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a `NOP` or another instruction not accessing this I/O port.

FIGURE 6-11: SUCCESSIVE I/O OPERATION



This example shows a write to PORTB followed by a read from PORTB.

Data setup time = (0.25 T_{CY} – T_{PD})

where: T_{CY} = instruction cycle.

T_{PD} = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.

7.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
  - Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit of the OPTION register. In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

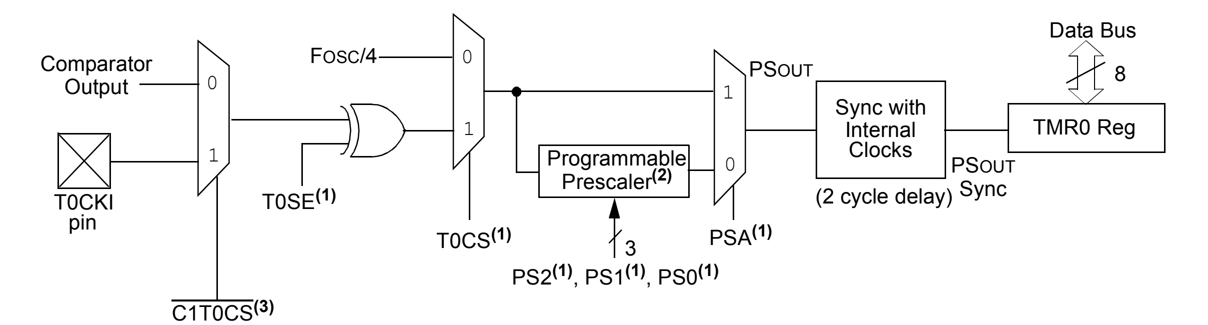
There are two types of Counter mode. The first Counter mode uses the T0CKI pin to increment Timer0. It is selected by setting the T0CS bit of the OPTION register, setting the $\overline{\text{C1T0CS}}$ bit of the CM1CON0 register and setting the $\overline{\text{C1OUTEN}}$ bit of the CM1CON0 register. In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit of the OPTION register determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 7.1 "Using Timer0 with an External Clock"**.

The second Counter mode uses the output of the comparator to increment Timer0. It can be entered in two different ways. The first way is selected by setting the T0CS bit of the OPTION register, and clearing the $\overline{\text{C1T0CS}}$ bit of the CM1CON0 register ($\overline{\text{C1OUTEN}}$ [CM1CON0<6>] does not affect this mode of operation). This enables an internal connection between the comparator and the Timer0.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit, PSA of the OPTION register. Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. **Section 7.2 "Prescaler"** details the operation of the prescaler.

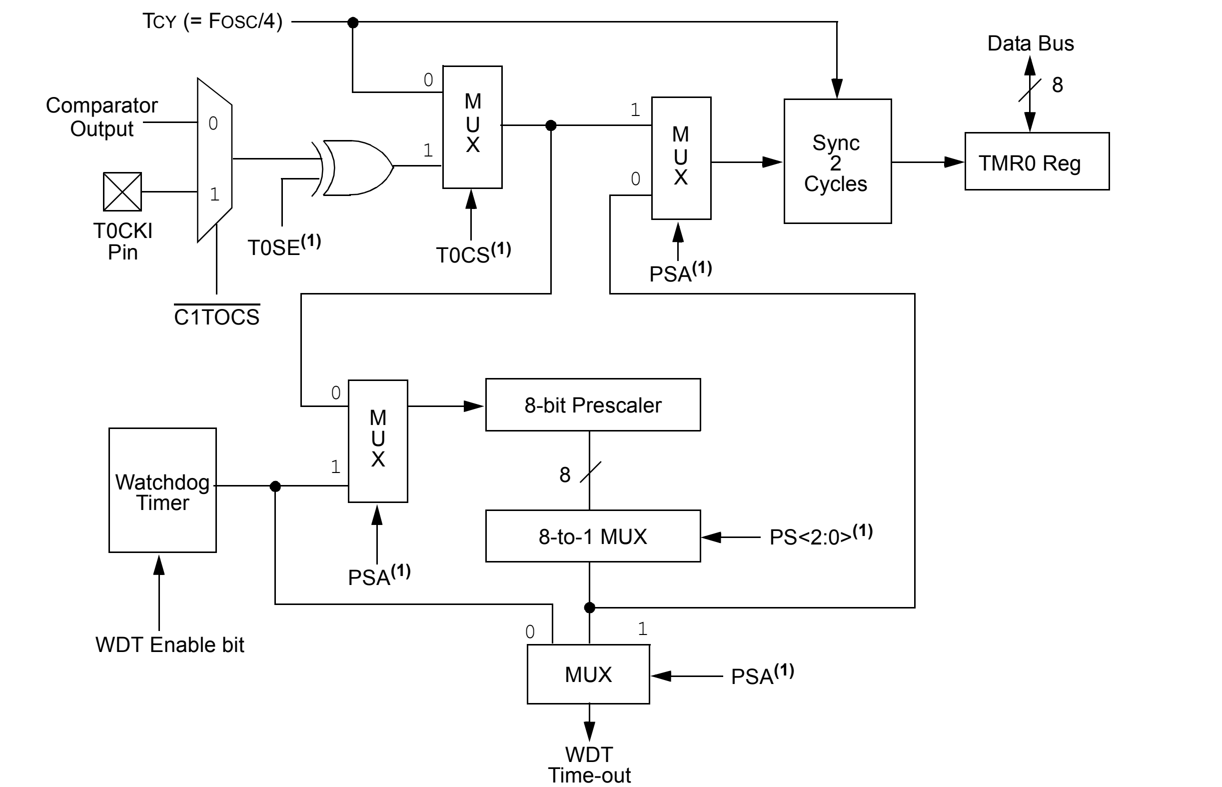
A summary of registers associated with the Timer0 module is found in Table 7-1.

FIGURE 7-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer.
3: The $\overline{\text{C1T0CS}}$ bit is in the CM1CON0 register.

FIGURE 7-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

NOTES:

REGISTER 8-1: CONFIG: CONFIGURATION WORD REGISTER

$\overline{\text{CPDF}}$	IOSCFS	MCLRE	$\overline{\text{CP}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 7							bit 0

bit 7 **$\overline{\text{CPDF}}$:** Code Protection bit – Flash Data Memory
`1` = Code protection off
`0` = Code protection on

bit 6 **IOSCFS:** Internal Oscillator Frequency Select bit
`1` = 8 MHz INTOSC frequency
`0` = 4 MHz INTOSC frequency

bit 5 **MCLRE:** Master Clear Enable bit
`1` = RB3/$\overline{\text{MCLR}}$ pin functions as $\overline{\text{MCLR}}$
`0` = RB3/$\overline{\text{MCLR}}$ pin functions as RB3, $\overline{\text{MCLR}}$ internally tied to V_{DD}

bit 4 **$\overline{\text{CP}}$:** Code Protection bit – User Program Memory
`1` = Code protection off
`0` = Code protection on

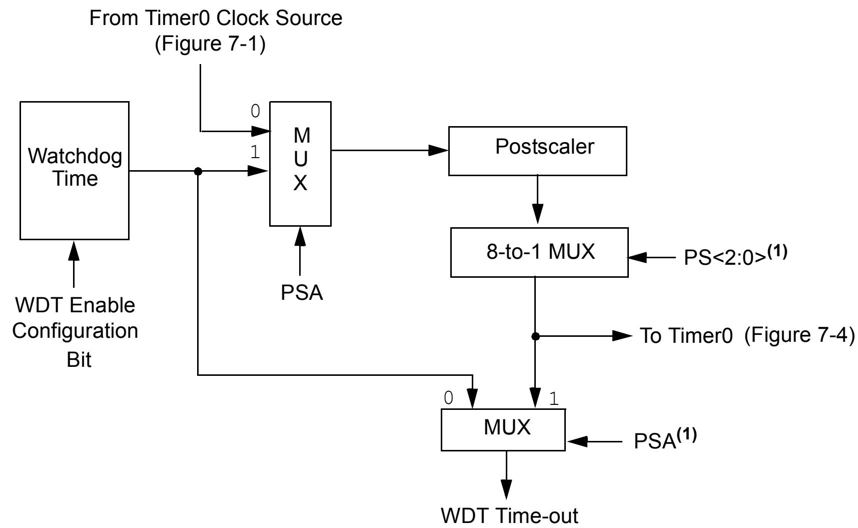
bit 3 **WDTE:** Watchdog Timer Enable bit
`1` = WDT enabled
`0` = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
`000` = LP oscillator and 18 ms DRT
`001` = XT oscillator and 18 ms DRT
`010` = HS oscillator and 18 ms DRT
`011` = EC oscillator with RB4 function on RB4/OSC2/CLKOUT and 1 ms DRT[(1)]
`100` = INTRC with RB4 function on RB4/OSC2/CLKOUT and 1 ms DRT[(1)]
`101` = INTRC with CLKOUT function on RB4/OSC2/CLKOUT and 1 ms DRT[(1)]
`110` = EXTRC with RB4 function on RB4/OSC2/CLKOUT and 1 ms DRT[(1)]
`111` = EXTRC with CLKOUT function on RB4/OSC2/CLKOUT and 1 ms DRT[(1)]

Note 1: Refer to the "*PIC16F526 Memory Programming Specification*", DS41317 to determine how to access the Configuration Word.

2: DRT length (18 ms or 1 ms) is a function of Clock mode selection. It is the responsibility of the application designer to ensure the use of either 18 ms (nominal) DRT or the 1 ms (nominal) DRT will result in acceptable operation. Refer to **Section 14.1 "DC Characteristics: PIC16F526 (Industrial)"** and **Section 14.2 "DC Characteristics: PIC16F526 (Extended)"** for V_{DD} rise time and stability requirements for this mode of operation.

FIGURE 8-11: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: PSA, PS<2:0> are bits in the OPTION register.

TABLE 8-6: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	OPTION	$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded boxes = Not used by Watchdog Timer.

NOTES:

RETLW — Return with Literal in W

Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RLF — Rotate Left f through Carry

Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.

RRF — Rotate Right f through Carry

Syntax:	[*label*] RRF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

SLEEP — Enter SLEEP Mode

Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT; 0 → WDT prescaler; 1 → $\overline{TO}$; 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$, RBWUF
Description:	Time-out Status bit ($\overline{TO}$) is set. The Power-down Status bit ($\overline{PD}$) is cleared. RBWUF is unaffected. The WDT and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped. See **Section 8.9 "Power-down Mode (Sleep)"** on Sleep for more details.

SUBWF — Subtract W from f

Syntax:	[*label*] SUBWF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(f) – (W) → (dest)
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

SWAPF — Swap Nibbles in f

Syntax:	[*label*] SWAPF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(f<3:0>) → (dest<7:4>); (f<7:4>) → (dest<3:0>)
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W register. If 'd' is '1', the result is placed in register 'f'.

FIGURE 14-1: PIC16F526 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C

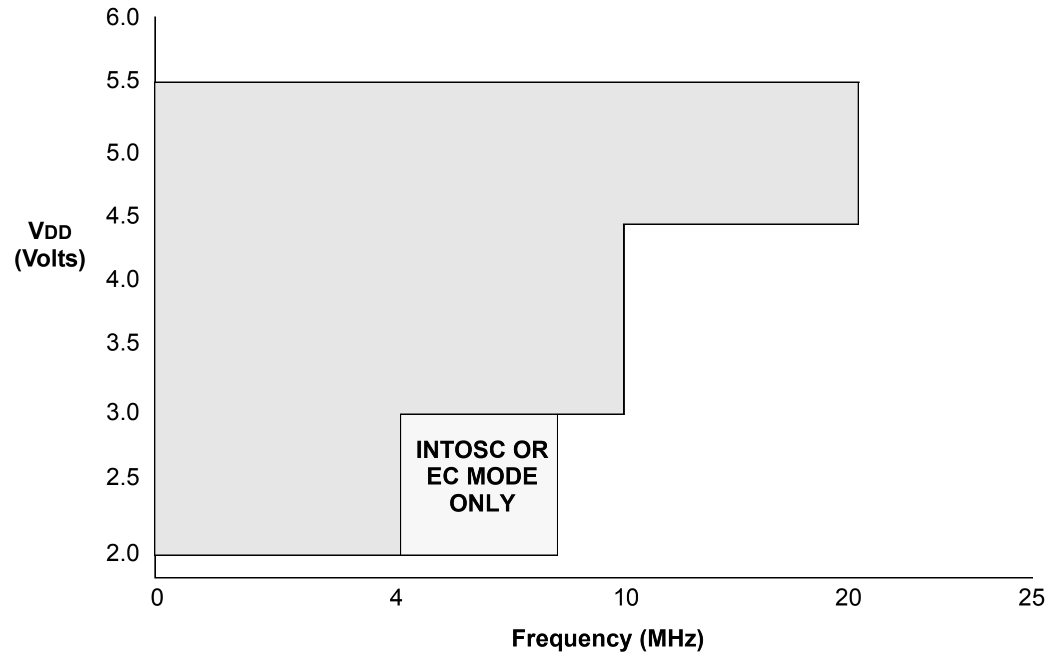


FIGURE 14-2: MAXIMUM OSCILLATOR FREQUENCY TABLE

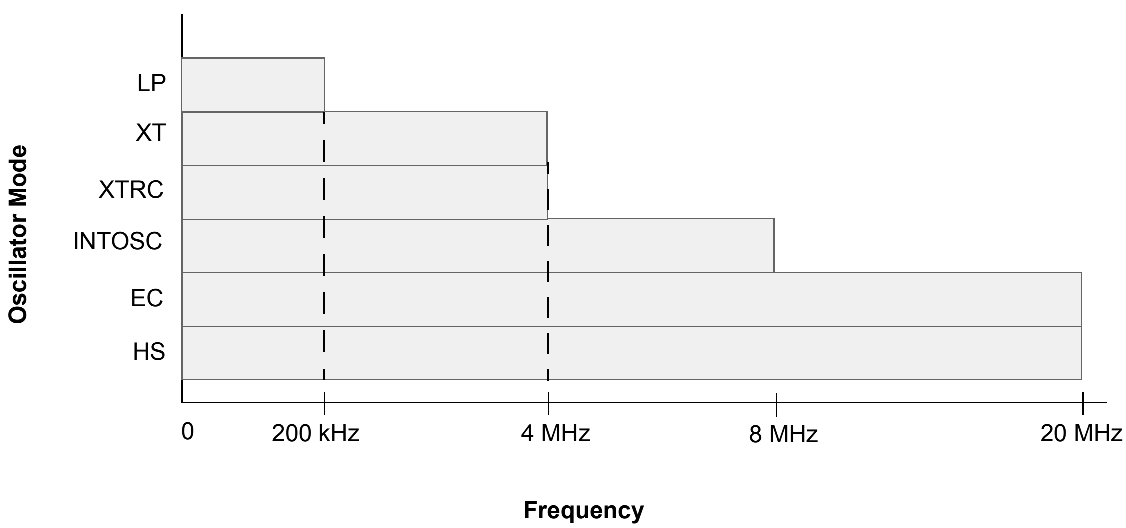


TABLE 14-7: CALIBRATED INTERNAL RC FREQUENCIES

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial), -40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in **Section 14.1 "DC Characteristics: PIC16F526 (Industrial)"**					
Param No.	**Sym.**	**Characteristic**	**Freq. Tolerance**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
F10	FOSC	Internal Calibrated INTOSC Frequency(1)	± 1%	7.92	8.00	8.08	MHz	3.5V, +25°C
			± 2%	7.84	8.00	8.16	MHz	2.5V ≤ VDD ≤ 5.5V 0°C ≤ TA ≤ +85°C
			± 5%	7.60	8.00	8.40	MHz	2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ +85°C (Ind.) -40°C ≤ TA ≤ +125°C (Ext.)

* These parameters are characterized but not tested.

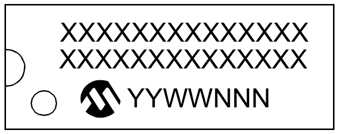
† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 uF and 0.01 uF values in parallel are recommended.

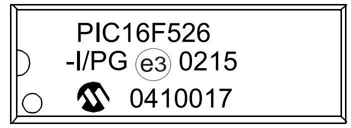
16.0 PACKAGING INFORMATION

16.1 Package Marking Information

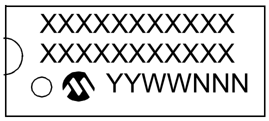
14-Lead PDIP (300 mil)



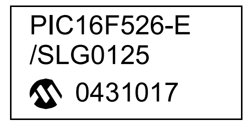
Example



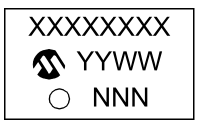
14-Lead SOIC (3.90 mm)



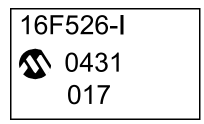
Example



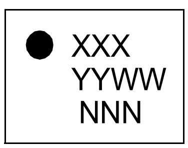
14-Lead TSSOP (4.4 mm)



Example



16-Lead QFN



Example

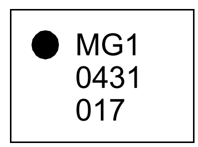


TABLE 16-1: 16-LEAD 3X3 QFN (MG) TOP MARKING

Part Number	Marking
PIC16F526-I/MG	MG1
PIC16F526-E/MG	MG2

Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
e3	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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