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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x14b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb11f16es0-b-qfn32r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1. Feature List

The EFM8LB1 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - · Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 72 MHz maximum operating frequency
- Memory:
 - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
 - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- · Power:
 - Internal LDO regulator for CPU core voltage
 - · Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
 - Up to 25 pins 5 V tolerant under bias
 - Selectable state retention through reset events
 - · Flexible peripheral crossbar for peripheral routing
 - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- · Clock Sources:
 - Internal 72 MHz oscillator with accuracy of ±2%
 - Internal 24.5 MHz oscillator with ±2% accuracy
 - · Internal 80 kHz low-frequency oscillator
 - External CMOS clock option
 - External crystal/RC oscillator (up to 25 MHz)

- Analog:
 - 14/12/10-Bit Analog-to-Digital Converter (ADC)
 - Internal calibrated temperature sensor (±3 °C)
 - 4 x 12-Bit Digital-to-Analog Converters (DAC)
 - 2 x Low-current analog comparators with adjustable reference
- Communications and Digital Peripherals:
 - 2 x UART, up to 3 Mbaud
 - SPI™ Master / Slave, up to 12 Mbps
 - SMBus™/I2C™ Master / Slave, up to 400 kbps
 - I²C High-Speed Slave, up to 3.4 Mbps
 - 16-bit CRC unit, supporting automatic CRC of flash at 256byte boundaries
 - 4 Configurable Logic Units
- · Timers/Counters and PWM:
 - 6-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes
 - 6 x 16-bit general-purpose timers
 - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
 - · Full memory and register inspection
 - Four hardware breakpoints, single-stepping
- Pre-programmed UART or SMBus bootloader

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8LB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified (pending) and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	 Core halted All peripherals clocked and fully operational Code resumes execution on wake event 	Set IDLE bit in PCON0	Any interrupt
Suspend	 Core and peripheral clocks halted HFOSC0 and HFOSC1 oscillators stopped Regulator in normal bias mode for fast wake Timer 3 and 4 may clock from LFOSC0 Code resumes execution on wake event 	 Switch SYSCLK to HFOSC0 Set SUSPEND bit in PCON1 	 Timer 4 Event SPI0 Activity I2C0 Slave Activity Port Match Event Comparator 0 Falling Edge CLUn Interrupt-Enabled Event
Stop	 All internal power nets shut down Pins retain state Exit on any reset source 	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Snooze	 Core and peripheral clocks halted HFOSC0 and HFOSC1 oscillators stopped Regulator in low bias current mode for energy savings Timer 3 and 4 may clock from LFOSC0 Code resumes execution on wake event 	 Switch SYSCLK to HFOSC0 Set SNOOZE bit in PCON1 	 Timer 4 Event SPI0 Activity I2C0 Slave Activity Port Match Event Comparator 0 Falling Edge CLUn Interrupt-Enabled Event
Shutdown	 All internal power nets shut down Pins retain state Exit on pin or power-on reset 	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	RSTb pin resetPower-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- · Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- · Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- · External port pins are forced to a known state.
- · Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- · Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- · Watchdog timer reset
- · Missing clock detector reset
- · Flash error reset

3.9 Debugging

The EFM8LB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader or an SMBus bootloader. These bootloaders reside in the code security page, which is the last page of code flash; they can be erased if they are not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [Application Notes] tile.



Figure 3.2. Flash Memory Map with Bootloader - 62.5 KB Devices

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5
SMBus	P0.2 – SDA ¹
	P0.3 – SCL ¹

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
ADC0 ⁴	I _{ADC}	High Speed Mode	—	1275	1700	μA
		1 Msps, 12-bit conversions				
		Normal bias settings				
		V _{DD} = 3.0 V				
		Low Power Mode	—	390	530	μA
		350 ksps, 12-bit conversions				
		Low power bias settings				
		V _{DD} = 3.0 V				
Internal ADC0 Reference ⁵	I _{VREFFS}	High Speed Mode		700	790	μA
		Low Power Mode	_	170	210	μA
On-chip Precision Reference	I _{VREFP}		—	75	—	μA
Temperature Sensor	I _{TSENSE}		—	68	120	μA
Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3) ⁶	I _{DAC}		_	125		μA
Comparators (CMP0, CMP1)	I _{CMP}	CPMD = 11	_	0.5	_	μA
		CPMD = 10	_	3		μA
		CPMD = 01		10	_	μA
		CPMD = 00	—	25	—	μA
Comparator Reference	I _{CPREF}		—	24	—	μA
Voltage Supply Monitor (VMON0)	I _{VMON}		—	15	20	μA

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.

- 2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.
- 3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.
- 4. ADC0 power excludes internal reference supply current.
- 5. The internal reference is enabled as-needed when operating the ADC in low power mode. Total ADC + Reference current will depend on sampling rate.

6. DAC supply current for each enabled DA and not including external load on pin.

4.1.13 Comparators

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Response Time, CPMD = 00	t _{RESP0}	+100 mV Differential		100	_	ns
(Highest Speed)		-100 mV Differential		150	_	ns
Response Time, CPMD = 11 (Low-	t _{RESP3}	+100 mV Differential		1.5	_	μs
est Power)		-100 mV Differential		3.5	_	μs
Positive Hysteresis	HYS _{CP+}	CPHYP = 00		0.4	_	mV
Mode 0 (CPMD = 00)		CPHYP = 01		8		mV
		CPHYP = 10		16		mV
		CPHYP = 11		32	_	mV
Negative Hysteresis	HYS _{CP-}	CPHYN = 00		-0.4		mV
Mode 0 (CPMD = 00)		CPHYN = 01		-8	_	mV
		CPHYN = 10	_	-16	_	mV
		CPHYN = 11		-32	_	mV
Positive Hysteresis	HYS _{CP+}	CPHYP = 00	_	0.5	_	mV
Mode 1 (CPMD = 01)		CPHYP = 01	_	6	_	mV
		CPHYP = 10	_	12	_	mV
		CPHYP = 11	_	24	_	mV
Negative Hysteresis	HYS _{CP-}	CPHYN = 00	_	-0.5	_	mV
Mode 1 (CPMD = 01)		CPHYN = 01	_	-6	_	mV
		CPHYN = 10	_	-12	_	mV
		CPHYN = 11	_	-24	_	mV
Positive Hysteresis	HYS _{CP+}	CPHYP = 00	_	0.7	_	mV
Mode 2 (CPMD = 10)		CPHYP = 01	_	4.5	_	mV
		CPHYP = 10	_	9	_	mV
		CPHYP = 11	_	18	_	mV
Negative Hysteresis	HYS _{CP-}	CPHYN = 00	_	-0.6	_	mV
Mode 2 (CPMD = 10)		CPHYN = 01	_	-4.5	_	mV
		CPHYN = 10	_	-9	_	mV
		CPHYN = 11	_	-18	_	mV
Positive Hysteresis	HYS _{CP+}	CPHYP = 00	_	1.5	_	mV
Mode 3 (CPMD = 11)		CPHYP = 01	_	4	_	mV
		CPHYP = 10	_	8	_	mV
		CPHYP = 11		16	_	mV

Table 4.13. Comparators

4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Output High Voltage (High Drive)	V _{OH}	I_{OH} = -7 mA, $V_{IO} \ge 3.0$ V	V _{IO} - 0.7	_	_	V
		I_{OH} = -3.3 mA, 2.2 V ≤ V_{IO} < 3.0 V	V _{IO} x 0.8	_	-	V
		I_{OH} = -1.8 mA, 1.71 V \leq V _{IO} < 2.2 V				
Output Low Voltage (High Drive)	V _{OL}	I _{OL} = 13.5 mA, V _{IO} ≥ 3.0 V		_	0.6	V
		I_{OL} = 7 mA, 2.2 V ≤ V_{IO} < 3.0 V	—	_	V _{IO} x 0.2	V
		I_{OL} = 3.6 mA, 1.71 V \leq V _{IO} < 2.2 V				
Output High Voltage (Low Drive)	V _{OH}	I _{OH} = -4.75 mA, V _{IO} ≥ 3.0 V	V _{IO} - 0.7	_	—	V
		I_{OH} = -2.25 mA, 2.2 V ≤ V _{IO} < 3.0 V	V _{IO} x 0.8	_	—	V
		I_{OH} = -1.2 mA, 1.71 V \leq V _{IO} < 2.2 V				
Output Low Voltage (Low Drive)	V _{OL}	I _{OL} = 6.5 mA, V _{IO} ≥ 3.0 V	—	_	0.6	V
		I_{OL} = 3.5 mA, 2.2 V ≤ V_{IO} < 3.0 V	—		V _{IO} x 0.2	V
		I_{OL} = 1.8 mA, 1.71 V \leq V _{IO} < 2.2 V				
Input High Voltage	VIH		0.7 x	_	_	V
			V _{IO}			
Input Low Voltage	VIL		_		0.3 x	V
					V _{IO}	
Pin Capacitance	C _{IO}			7	_	pF
Weak Pull-Up Current	I _{PU}	V _{DD} = 3.6	-30	-20	-10	μA
(V _{IN} = 0 V)						
Input Leakage (Pullups off or Ana- log)	I _{LK}	$GND < V_{IN} < V_{IO}$	-1.1	_	4	μΑ
Input Leakage Current with V _{IN}	I _{LK}	$V_{IO} < V_{IN} < V_{IO} + 2.5 V$	0	5	150	μA
anove AIO		Any pin except P3.0, P3.1, P3.2, or P3.3				

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.



Figure 5.2. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number	DO O	Multifum etian 1/0	N	DOMATO	
	P0.0		res		VREF
				IN I 1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
2	VIO	I/O Supply Power Input			
3	VDD	Supply Power Input			
4	RSTb /	Active-low Reset /			
	C2CK	C2 Debug Clock			
5	P3.7 /	Multifunction I/O /			
	C2D	C2 Debug Data			
6	P3.4	Multifunction I/O			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19
					CMP1P.8
					CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18
					CMP1P.7
					CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17
					CMP1P.6
					CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.16
				CLU1B.15	CMP1P.5
				CLU2B.15	CMP1N.5
				CLU3A.15	

Table 6.1. Pin Definitions for EFM8LB1x-QFN32

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2 2	Multifunction I/O	Vec		ADC0 15
	1 2.2				CMP1P 4
					CMP1N 4
				CLU2B 14	
				CLU3A 14	
16	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.14
				I2C0 SCL	CMP1P.3
				CLU1B.14	CMP1N.3
				CLU2A.15	
				CLU3B.15	
17	P2.0	Multifunction I/O	Yes	P2MAT.0	CMP1P.2
				I2C0 SDA	CMP1N.2
				 CLU1A.14	
				CLU2A.14	
				CLU3B.14	
18	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.13
				CLU0B.15	CMP0P.9
				CLU1B.13	CMP0N.9
				CLU2A.13	
19	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.12
				CLU0A.15	
				CLU1B.12	
				CLU2A.12	
20	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.11
				CLU0B.14	
				CLU1A.13	
				CLU2B.13	
21	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.10
				CLU0A.14	
				CLU1A.12	
				CLU2B.12	
22	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.9
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
29	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.2
				INT0.4	CMP0P.2
				INT1.4	CMP0N.2
				UART0_TX	
				CLU0A.10	
				CLU1A.8	
				CLU3B.10	
30	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.9	
				CLU3A.9	
31	P0.2	Multifunction I/O	Yes	P0MAT.2	XTAL1
				INT0.2	ADC0.1
				INT1.2	CMP0P.1
				CLU0OUT	CMP0N.1
				CLU0A.9	
				CLU2B.8	
				CLU3A.8	
32	P0.1	Multifunction I/O	Yes	P0MAT.1	ADC0.0
				INT0.1	CMP0P.0
				INT1.1	CMP0N.0
				CLU0B.8	AGND
				CLU2A.9	
				CLU3B.9	
Center	GND	Ground			

Pin	Pin Name	Description	Crossbar Capability	Additional Digital	Analog Functions
Number					
6	P3.7 /	Multifunction I/O /			
	C2D	C2 Debug Data			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19
					CMP1P.8
					CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18
					CMP1P.7
					CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17
					CMP1P.6
					CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.16
				CLU1B.15	CMP1P.5
				CLU2B.15	CMP1N.5
				CLU3A.15	
15	P2.2	Multifunction I/O	Yes	P2MAT.2	ADC0.15
				CLU2OUT	CMP1P.4
				CLU1A.15	CMP1N.4
				CLU2B.14	
				CLU3A.14	
16	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.14
				I2C0_SCL	CMP1P.3
				CLU1B.14	CMP1N.3
				CLU2A.15	
				CLU3B.15	
17	P2.0	Multifunction I/O	Yes	P2MAT.0	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb /	Active-low Reset /			
	C2CK	C2 Debug Clock			
6	P3.0 /	Multifunction I/O /			
	C2D	C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3	DAC3
				CLU1B.15	
				CLU2B.15	
				CLU3A.15	
8	P2.2	Multifunction I/O	Yes	P2MAT.2	DAC2
				CLU1A.15	
				CLU2B.14	
				CLU3A.14	
9	P2.1	Multifunction I/O	Yes	P2MAT.1	DAC1
				CLU1B.14	
				CLU2A.15	
				CLU3B.15	
10	P2.0	Multifunction I/O	Yes	P2MAT.0	DAC0
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	
11	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.11
				CLU3OUT	CMP1P.5
				CLU0A.15	CMP1N.5
				CLU1B.12	
				CLU2A.12	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
11	P2.1	Multifunction I/O	Yes	P2MAT.1	DAC1
				CLU1B.14	
				CLU2A.15	
				CLU3B.15	
12	P2.0	Multifunction I/O	Yes	P2MAT.0	DAC0
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	
13	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.12
				CLU0B.15	CMP1P.6
				CLU1B.13	CMP1N.6
				CLU2A.13	
14	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.11
				CLU3OUT	CMP1P.5
				CLU0A.15	CMP1N.5
				CLU1B.12	
				CLU2A.12	
15	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.10
				CLU2OUT	CMP1P.4
				CLU0B.14	CMP1N.4
				CLU1A.13	
				CLU2B.13	
16	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.9
				I2C0_SCL	CMP1P.3
				CLU0A.14	CMP1N.3
				CLU1A.12	
				CLU2B.12	
17	P1.3	Multifunction I/O	Yes	P1MAT.3	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1 2	Multifunction I/O	Yes	Ρ1ΜΔΤ 2	
	1 1.2				1000.0
				CLU1A 11	
				CLU2B 10	
				CI U3A 12	
19	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	
				CLU1B.10	
				CLU2A.11	
				CLU3B.13	
20	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU0A.12	
				CLU1A.10	
				CLU2A.10	
				CLU3B.12	
21	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU1OUT	CMP1P.1
				CLU0B.11	CMP1N.1
				CLU1B.9	
				CLU3A.11	
22	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	CMP1P.0
				CLU0A.11	CMP1N.0
				CLU1B.8	
				CLU3A.10	
23	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
				CLU3B.11	

Dimension	Min	Мах
Note:		
1. All dimensions shown are in millimeters	(mm) unless otherwise noted.	
2. Dimensioning and Tolerancing is per the	e ANSI Y14.5M-1994 specification.	
3. This Land Pattern Design is based on the	ne IPC-7351 guidelines.	
4. All dimensions shown are at Maximum cation Allowance of 0.05mm.	Material Condition (MMC). Least Material Cor	ndition (LMC) is calculated based on a Fabri-
 All metal pads are to be non-solder mas minimum, all the way around the pad. 	k defined (NSMD). Clearance between the so	older mask and the metal pad is to be 60 μm
6. A stainless steel, laser-cut and electro-p	oolished stencil with trapezoidal walls should b	be used to assure good solder paste release.
7. The stencil thickness should be 0.125 m	nm (5 mils).	
8. The ratio of stencil aperture to land pad	size should be 1:1 for all perimeter pads.	
9. A 2 x 2 array of 1.10 mm square openin	gs on a 1.30 mm pitch should be used for the	center pad.
· · · · · · · · · · · · · · · · · · ·	5	

- 10. A No-Clean, Type-3 solder paste is recommended.
- 11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

9.2 QFN24 PCB Land Pattern



Figure 9.2. QFN24 PCB Land Pattern Drawing

Table 9.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Мах	
C1	3.00		
C2	3.00		
e	0.4 REF		
X1	0.20		
X2	1.80		
Y1	0.80		
Y2	1.80		
Y3	0.4		
f	2.50 REF		
с	0.25	0.35	

Dimension	Min	Мах
Note:		
1. All dimensions shown are in millimeters	(mm) unless otherwise noted.	
2. Dimensioning and Tolerancing is per the	e ANSI Y14.5M-1994 specification.	
3. This Land Pattern Design is based on th	e IPC-SM-782 guidelines.	
 All metal pads are to be non-solder mas minimum, all the way around the pad. 	k defined (NSMD). Clearance between the so	lder mask and the metal pad is to be 60 μm
5. A stainless steel, laser-cut and electro-p	olished stencil with trapezoidal walls should b	be used to assure good solder paste release.
6. The stencil thickness should be 0.125 m	ım (5 mils).	
7. The ratio of stencil aperture to land pad	size should be 1:1 for all perimeter pads.	
8. A 2 x 1 array of 0.7 mm x 1.6 mm openi	ngs on a 0.9 mm pitch should be used for the	center pad.
9. A No-Clean, Type-3 solder paste is reco	mmended.	

10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 QFN24 Package Marking



Figure 9.3. QFN24 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

11. Revision History

11.1 Revision 1.01

October 21st, 2016

Updated QFN24 center pad stencil description.

11.2 Revision 1.0

September 6th, 2016

Updated part numbers to revision B.

Updated many specifications with full characterization data.

Added a note regarding which DACs are available to Table 2.1 Product Selection Guide on page 2.

Added specifications for 4.1.16 SMBus.

Added bootloader pinout information to 3.10 Bootloader.

Added CRC Calculation Time to 4.1.4 Flash Memory.

11.3 Revision 0.5

February 10th, 2016

Updated Figure 5.2 Debug Connection Diagram on page 32 to move the pull-up resistor on C2D / RSTb to after the series resistor instead of before.

Added S0 devices and information about the SMBus bootloader in 3.10 Bootloader.

Added a reference to AN945: EFM8 Factory Bootloader User Guide in 3.10 Bootloader.

Added mention of the pre-programmed bootloaders in 1. Feature List.

Updated all part numbers to revision B.

Added the C oscillator, which is now available on revision B.

Adjusted C1, C2, X2, Y2, and Y1 maximums for 7.2 QFN32 PCB Land Pattern.

Adjusted package markings for QFN32 and QSOP24 packages.

Filled in TBD minimum and maximum values for DAC Differential Nonlinearity in Table 4.12 DACs on page 24.

11.4 Revision 0.4

Updated specification tables based on current device characterization status and production test limits.

Added bootloader section.

Added typical connection diagrams.

Corrected CLU connections in pin function tables.

11.5 Revision 0.3

Added information on the bootloader to 3.10 Bootloader.

Updated some characterization TBD values.

11.6 Revision 0.1

Initial release.

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