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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25К х 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x14b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f32e-b-qfn32r

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2. Ordering Information



Figure 2.1. EFM8LB1 Part Numbering

All EFM8LB1 family members have the following features:

- CIP-51 Core running up to 72 MHz
- Three Internal Oscillators (72 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- · 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- Six 16-bit Timers
- Four Configurable Logic Units
- 14-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, temperature sensor, channel sequencer, and directto-XRAM data transfer
- Two Analog Comparators
- 16-bit CRC Unit
- AEC-Q100 qualified (pending)

In addition to these features, each part number in the EFM8LB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Voltage DACs	Comparator 0 Inputs	Comparator 1 Inputs	Bootloader Type	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8LB12F64E-B-QFN32	64	4352	29	20	4	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB12F64E-B-QFP32	64	4352	28	20	4	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB12F64E-B-QFN24	64	4352	20	12	4	6	6	UART	Yes	-40 to +105 °C	QFN24

Table 2.1. Product Selection Guide

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	 Core halted All peripherals clocked and fully operational Code resumes execution on wake event 	Set IDLE bit in PCON0	Any interrupt
Suspend	 Core and peripheral clocks halted HFOSC0 and HFOSC1 oscillators stopped Regulator in normal bias mode for fast wake Timer 3 and 4 may clock from LFOSC0 Code resumes execution on wake event 	 Switch SYSCLK to HFOSC0 Set SUSPEND bit in PCON1 	 Timer 4 Event SPI0 Activity I2C0 Slave Activity Port Match Event Comparator 0 Falling Edge CLUn Interrupt-Enabled Event
Stop	 All internal power nets shut down Pins retain state Exit on any reset source 	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Snooze	 Core and peripheral clocks halted HFOSC0 and HFOSC1 oscillators stopped Regulator in low bias current mode for energy savings Timer 3 and 4 may clock from LFOSC0 Code resumes execution on wake event 	 Switch SYSCLK to HFOSC0 Set SNOOZE bit in PCON1 	 Timer 4 Event SPI0 Activity I2C0 Slave Activity Port Match Event Comparator 0 Falling Edge CLUn Interrupt-Enabled Event
Shutdown	 All internal power nets shut down Pins retain state Exit on pin or power-on reset 	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	RSTb pin resetPower-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- · Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- · Support for slave mode only
- · Clock low extending (clock stretching) to interface with faster masters
- · Hardware support for 7-bit slave address recognition
- Transmit and receive FIFOs (two byte) to help increase throughput in faster applications
- · Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- · Automatic CRC of flash contents on one or more 256-byte blocks
- · Initial seed selection of 0x0000 or 0xFFFF

Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- · Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- · Units may be operated synchronously or asynchronously
- · May be cascaded together to perform more complicated logic functions
- · Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- · Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- · Asynchronous output may be used to wake from low-power states

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- · Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- · External port pins are forced to a known state.
- · Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- · Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- · Watchdog timer reset
- · Missing clock detector reset
- · Flash error reset

3.9 Debugging

The EFM8LB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Idle Mode Wake-up Time	t _{IDLEWK}		2	_	3	SYSCLKs
Suspend Mode Wake-up Time	t _{SUS-}	SYSCLK = HFOSC0	_	170	_	ns
	PENDWK	CLKDIV = 0x00				
Snooze Mode Wake-up Time	t _{SLEEPWK}	SYSCLK = HFOSC0	—	12	—	μs
		CLKDIV = 0x00				

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit			
High Frequency Oscillator 0 (24.5 MHz)									
Oscillator Frequency	f _{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz			
Power Supply Sensitivity	PSS _{HFOS} C0	T _A = 25 °C	_	0.5	_	%/V			
Temperature Sensitivity	TS _{HFOSC0}	V _{DD} = 3.0 V	_	40	_	ppm/°C			
High Frequency Oscillator 1 (72 N	High Frequency Oscillator 1 (72 MHz)								
Oscillator Frequency	f _{HFOSC1}	Full Temperature and Supply Range	70.5	72	73.5	MHz			
Power Supply Sensitivity	PSS _{HFOS} C1	T _A = 25 °C	_	300	_	ppm/V			
Temperature Sensitivity	TS _{HFOSC1}	V _{DD} = 3.0 V	—	103	—	ppm/°C			
Low Frequency Oscillator (80 kHz	z)								
Oscillator Frequency	f _{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz			
Power Supply Sensitivity	PSS _{LFOSC}	T _A = 25 °C	—	0.05	—	%/V			
Temperature Sensitivity	TS _{LFOSC}	V _{DD} = 3.0 V	—	65	—	ppm/°C			

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Resolution	N _{bits}	14 Bit Mode		14		Bits
		12 Bit Mode 12				Bits
		10 Bit Mode		10		Bits
Throughput Rate	f _S	14 Bit Mode	—	_	900	ksps
(High Speed Mode)		12 Bit Mode	_	_	1	Msps
		10 Bit Mode	—	—	1.125	Msps
Throughput Rate	f _S	14 Bit Mode	—	—	320	ksps
(Low Power Mode)		12 Bit Mode	—	_	340	ksps
		10 Bit Mode	—	—	360	ksps
Tracking Time	t _{TRK}	High Speed Mode	217.8 ¹	—	_	ns
		Low Power Mode	450	_	_	ns
Power-On Time	t _{PWR}		1.2	_	_	μs
SAR Clock Frequency	f _{SAR}	High Speed Mode	_	_	18.36	MHz
		Low Power Mode	_	_	12.25	MHz
Conversion Time ²	t _{CNV}	14-Bit Conversion,	14-Bit Conversion,		0.81	
		SAR Clock =18 MHz,				
		System Clock = 72 MHz.				
		12-Bit Conversion,		0.7		
		SAR Clock =18 MHz,				
		System Clock = 72 MHz.				
		10-Bit Conversion,		0.59		μs
		SAR Clock =18 MHz,				
		System Clock = 72 MHz.				
Sample/Hold Capacitor	C _{SAR}	Gain = 1	_	5.2	_	pF
		Gain = 0.75	_	3.9	_	pF
		Gain = 0.5	—	2.6	_	pF
		Gain = 0.25	_	1.3	_	pF
Input Pin Capacitance	C _{IN}	High Quality Input	_	20	_	pF
		Normal Input	—	20	_	pF
Input Mux Impedance R _{MUX}		High Quality Input	—	330	_	Ω
		Normal Input	_	550	—	Ω
Voltage Reference Range	V _{REF}		1	_	V _{IO}	V
Input Voltage Range ³	V _{IN}		0 — V _{REF} / Gain		V _{REF} / Gain	V

Parameter	Symbol	Clocks						
SMBus Operating Frequency	f _{SMB}	f _{CSO} / 3						
Bus Free Time Between STOP and START Conditions	t _{BUF}	2 / f _{CSO}						
Hold Time After (Repeated) START Condition	t _{HD:STA}	1 / f _{CSO}						
Repeated START Condition Setup Time	t _{SU:STA}	2 / f _{CSO}						
STOP Condition Setup Time	t _{SU:STO}	2 / f _{CSO}						
Clock Low Period	t _{LOW}	1 / f _{CSO}						
Clock High Period	t _{HIGH}	2 / f _{CSO}						
Note: 1. f _{CSO} is the SMBus peripheral clock source overflow frequency.	Note: 1 feed is the SMBus peripheral clock source overflow frequency							

Table 4.17. SMBus Peripheral Timing Formulas (Master Mode)



Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit		
Thermal Resistance	θ _{JA}	J _A QFN24 Packages		30	_	°C/W		
		QFN32 Packages	—	26	_	°C/W		
		QFP32 Packages	—	80	—	°C/W		
		QSOP24 Packages	—	65	—	°C/W		
Note:								

1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 31 shows a typical connection diagram for the power pins of the device.



Figure 5.1. Power Connection Diagram

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number					
23	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	CMP0P.8
				CLU1A.11	CMP0N.8
				CLU2B.10	
				CLU3A.12	
24	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	CMP0P.7
				CLU1B.10	CMP0N.7
				CLU2A.11	
				CLU3B.13	
25	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU1OUT	CMP0P.6
				CLU0A.12	CMP0N.6
				CLU1A.10	CMP1P.1
				CLU2A.10	CMP1N.1
				CLU3B.12	
26	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU0B.11	CMP1P.0
				CLU1B.9	CMP1N.0
				CLU3A.11	
27	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	
				CLU0A.11	
				CLU1B.8	
				CLU3A.10	
28	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
				CLU3B.11	



Figure 6.2. EFM8LB1x-QFP32 Pinout

Table 6.2.	Pin Definitions	for EFM8LB1x	-QFP32
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Pin Numbor	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number					
1	P0.0	Multifunction I/O	Yes	POMAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb /	Active-low Reset /			
	С2СК	C2 Debug Clock			

Pin	Pin Name	Description	Crossbar Capability	Additional Digital	Analog Functions
Number					
6	P3.7 /	Multifunction I/O /			
	C2D	C2 Debug Data			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19
					CMP1P.8
					CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18
					CMP1P.7
					CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17
					CMP1P.6
					CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.16
				CLU1B.15	CMP1P.5
				CLU2B.15	CMP1N.5
				CLU3A.15	
15	P2.2	Multifunction I/O	Yes	P2MAT.2	ADC0.15
				CLU2OUT	CMP1P.4
				CLU1A.15	CMP1N.4
				CLU2B.14	
				CLU3A.14	
16	P2.1	Multifunction I/O	Yes	P2MAT.1	ADC0.14
				I2C0_SCL	CMP1P.3
				CLU1B.14	CMP1N.3
				CLU2A.15	
				CLU3B.15	
17	P2.0	Multifunction I/O	Yes	P2MAT.0	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU1A.14	
				CLU2A.14	
				CLU3B.14	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
25	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU1OUT	CMP0P.6
				CLU0A.12	CMP0N.6
				CLU1A.10	CMP1P.1
				CLU2A.10	CMP1N.1
				CLU3B.12	
26	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU0B.11	CMP1P.0
				CLU1B.9	CMP1N.0
				CLU3A.11	
27	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	
				CLU0A.11	
				CLU1B.8	
				CLU3A.10	
28	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
				CLU3B.11	
29	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.2
				INT0.4	CMP0P.2
				INT1.4	CMP0N.2
				UART0_TX	
				CLU0A.10	
				CLU1A.8	
				CLU3B.10	





Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number					
1	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.9	
				CLU3A.9	

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1 2	Multifunction I/O	Yes	Ρ1ΜΔΤ 2	
	1 1.2				1000.0
				CLU1A 11	
				CLU2B 10	
				CI U3A 12	
19	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	
				CLU1B.10	
				CLU2A.11	
				CLU3B.13	
20	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU0A.12	
				CLU1A.10	
				CLU2A.10	
				CLU3B.12	
21	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU1OUT	CMP1P.1
				CLU0B.11	CMP1N.1
				CLU1B.9	
				CLU3A.11	
22	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	CMP1P.0
				CLU0A.11	CMP1N.0
				CLU1B.8	
				CLU3A.10	
23	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
				CLU3B.11	

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions



Figure 7.1. QFN32 Package Drawing

Dimension	Min	Тур	Мах		
A	0.45	0.50	0.55		
A1	0.00	0.035	0.05		
b	0.15	0.20	0.25		
D	4.00 BSC.				
D2	2.80 2.90 3.00				
е	0.40 BSC.				
E	4.00 BSC.				
E2	2.80	3.00			
L	0.20	0.30	0.40		
ааа		_	0.10		
bbb	_	—	0.10		
ССС		—	0.08		
ddd	_	_	0.10		
eee	—	—	0.10		
999			0.05		

Table 7.1. QFN32 Package Dimensions





The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions



Figure 9.1. QFN24 Package Drawing

Dimension	Min	Тур	Мах	
A	0.8 0.85		0.9	
A1	0.00	—	0.05	
A2	—	0.65	—	
A3	0.203 REF			
b	0.15 0.2 0.25			
b1	0.25	0.3	0.35	
D	3.00 BSC			
E	3.00 BSC			

9.2 QFN24 PCB Land Pattern



Figure 9.2. QFN24 PCB Land Pattern Drawing

Table 9.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Мах		
C1	3.00			
C2	3.00			
e	0.4 REF			
X1	0.20			
X2	1.80			
Y1	0.80			
Y2	1.80			
Y3	0.4			
f	2.50 REF			
с	0.25	0.35		



Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

Table of Contents

1.	Feature List		. 1
2.	Ordering Information		. 2
3.	System Overview		. 4
	3.1 Introduction.		. 4
	3.2 Power		. 5
	3.3 I/O		. 5
	3.4 Clocking		. 6
	3.5 Counters/Timers and PWM		. 6
	3.6 Communications and Other Digital Peripherals		7
		•	10
		·	.10
		•	. 1 1
		•	. 1 1
	3.10 Bootloader	·	.12
4.	Electrical Specifications	•	14
	4.1 Electrical Characteristics		.14
	4.1.1 Recommended Operating Conditions		.14
	4.1.2 Power Consumption	·	.15
	4.1.3 Reset and Supply Monitor	•	.17
	4.1.4 Flash Memory	·	.17
	4.1.5 Power Management Timing	·	.18
		·	.18
		·	.19
		·	.19
	4.1.9 ADC	•	.20
	4 1 11 Temperature Sensor	·	.22
	4 1 12 DACs	•	.20
	4.1.13 Comparators	÷	.25
	4.1.14 Configurable Logic		.26
	4.1.15 Port I/O		.27
	4.1.16 SMBus		.28
	4.2 Thermal Conditions		.29
	4.3 Absolute Maximum Ratings		.30
5.	Typical Connection Diagrams		31
	5.1 Power		.31
	5.2 Debug		.32
	5.3 Other Connections		.32
6.	Pin Definitions	-	33
	6.1 EFM8LB1x-QFN32 Pin Definitions		.33