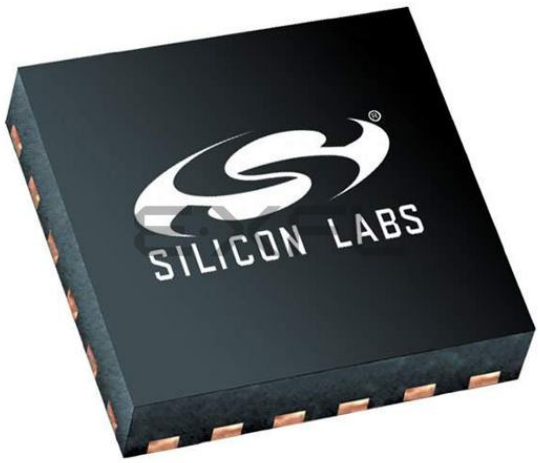

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x14b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f32es0-b-qfn24r

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Voltage DACs	Comparator 0 Inputs	Comparator 1 Inputs	Bootloader Type	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8LB12F64E-B-QSOP24	64	4352	21	13	4	6	7	UART	Yes	-40 to +105 °C	QSOP24
EFM8LB12F64ES0-B-QFN32	64	4352	29	20	4	10	9	SMBus	Yes	-40 to +105 °C	QFN32
EFM8LB12F64ES0-B-QFN24	64	4352	20	12	4	6	6	SMBus	Yes	-40 to +105 °C	QFN24
EFM8LB12F32E-B-QFN32	32	2304	29	20	4	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB12F32E-B-QFP32	32	2304	28	20	4	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB12F32E-B-QFN24	32	2304	20	12	4	6	6	UART	Yes	-40 to +105 °C	QFN24
EFM8LB12F32E-B-QSOP24	32	2304	21	13	4	6	7	UART	Yes	-40 to +105 °C	QSOP24
EFM8LB12F32ES0-B-QFN32	32	2304	29	20	4	10	9	SMBus	Yes	-40 to +105 °C	QFN32
EFM8LB12F32ES0-B-QFN24	32	2304	20	12	4	6	6	SMBus	Yes	-40 to +105 °C	QFN24
EFM8LB11F32E-B-QFN32	32	2304	29	20	2[1]	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB11F32E-B-QFP32	32	2304	28	20	2[1]	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB11F32E-B-QFN24	32	2304	20	12	2[1]	6	6	UART	Yes	-40 to +105 °C	QFN24
EFM8LB11F32E-B-QSOP24	32	2304	21	13	2[1]	6	7	UART	Yes	-40 to +105 °C	QSOP24
EFM8LB11F32ES0-B-QFN32	32	2304	29	20	2[1]	10	9	SMBus	Yes	-40 to +105 °C	QFN32
EFM8LB11F32ES0-B-QFN24	32	2304	20	12	2[1]	6	6	SMBus	Yes	-40 to +105 °C	QFN24
EFM8LB11F16E-B-QFN32	16	1280	29	20	2[1]	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB11F16E-B-QFP32	16	1280	28	20	2[1]	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB11F16E-B-QFN24	16	1280	20	12	2[1]	6	6	UART	Yes	-40 to +105 °C	QFN24
EFM8LB11F16E-B-QSOP24	16	1280	21	13	2[1]	6	7	UART	Yes	-40 to +105 °C	QSOP24
EFM8LB11F16ES0-B-QFN32	16	1280	29	20	2[1]	10	9	SMBus	Yes	-40 to +105 °C	QFN32
EFM8LB11F16ES0-B-QFN24	16	1280	20	12	2[1]	6	6	SMBus	Yes	-40 to +105 °C	QFN24
EFM8LB10F16E-B-QFN32	16	1280	29	20	0	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB10F16E-B-QFP32	16	1280	28	20	0	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB10F16E-B-QFN24	16	1280	20	12	0	6	6	UART	Yes	-40 to +105 °C	QFN24
EFM8LB10F16E-B-QSOP24	16	1280	21	13	0	6	7	UART	Yes	-40 to +105 °C	QSOP24
EFM8LB10F16ES0-B-QFN32	16	1280	29	20	0	10	9	SMBus	Yes	-40 to +105 °C	QFN32
EFM8LB10F16ES0-B-QFN24	16	1280	20	12	0	6	6	SMBus	Yes	-40 to +105 °C	QFN24

Note:

1. DAC0 and DAC1 are enabled on devices with 2 DACs available.

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader or an SMBus bootloader. These bootloaders reside in the code security page, which is the last page of code flash; they can be erased if they are not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [**Application Notes**] tile.

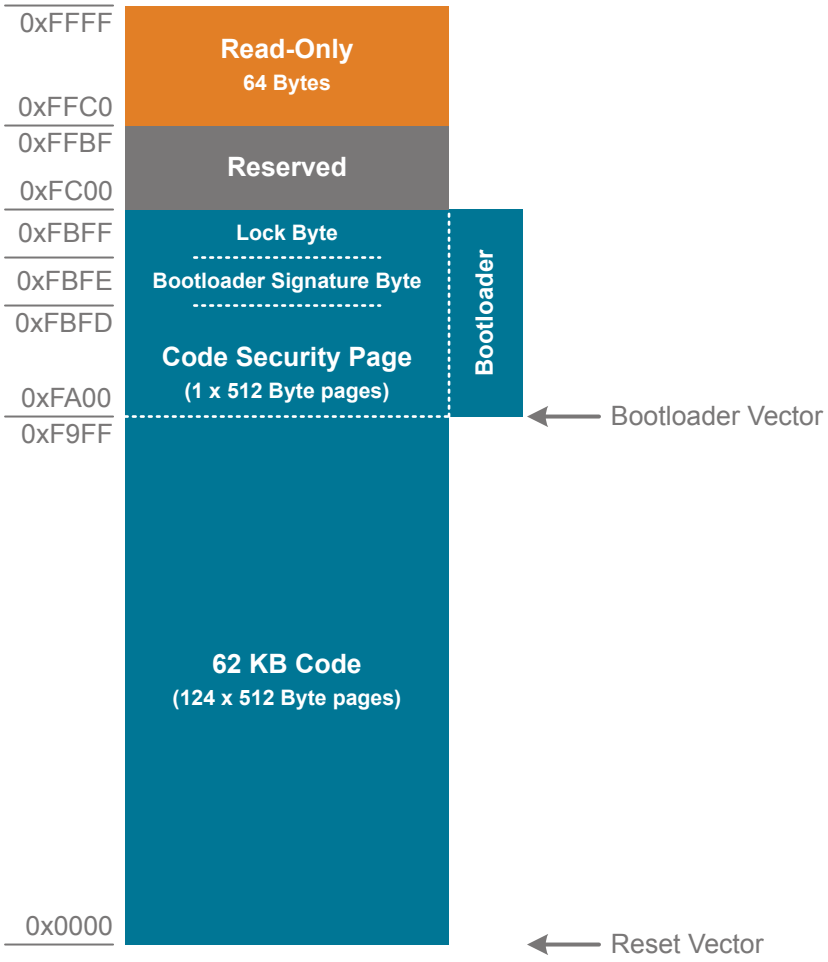


Figure 3.2. Flash Memory Map with Bootloader — 62.5 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5
SMBus	P0.2 – SDA[1]
	P0.3 – SCL[1]

Bootloader	Pins for Bootload Communication
Note: 1. The STK uses these pins for another purpose, so there is a special SMBus bootloader build for the STK only included in *AN945: EFM8 Factory Bootloader User Guide* that uses P1.2 (SDA) and P1.3 (SCL).	

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QFN32	P3.7 / C2D
QFP32	P3.7 / C2D
QFN24	P3.0 / C2D
QSOP24	P3.0 / C2D

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 14, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.2	—	3.6	V
Operating Supply Voltage on VIO[2, 3]	V_{IO}		2.2	—	V_{DD}	V
System Clock Frequency	f_{SYSCLK}		0	—	73.5	MHz
Operating Ambient Temperature	T_A		-40	—	105	°C

Note:

1. All voltages with respect to GND
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.
3. GPIO levels are undefined whenever VIO is less than 1 V.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode-Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 72 MHz (HFOSC1)[2]	—	12.9	15	mA
		F_{SYSCLK} = 24.5 MHz (HFOSC0)[2]	—	4.2	5	mA
		F_{SYSCLK} = 1.53 MHz (HFOSC0)[2]	—	625	1050	µA
		F_{SYSCLK} = 80 kHz[3]	—	155	575	µA
Idle Mode-Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 72 MHz (HFOSC1)[2]	—	9.6	11.1	mA
		F_{SYSCLK} = 24.5 MHz (HFOSC0)[2]	—	3.14	3.8	mA
		F_{SYSCLK} = 1.53 MHz (HFOSC0)[2]	—	520	950	µA
		F_{SYSCLK} = 80 kHz[3]	—	135	550	µA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I_{DD}	LFO Running	—	125	545	µA
		LFO Stopped	—	120	535	µA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I_{DD}	LFO Running	—	23	430	µA
		LFO Stopped	—	19	425	µA
Stop Mode—Core halted and all clocks stopped,Internal LDO On, Supply monitor off.	I_{DD}		—	120	535	µA
Shutdown Mode—Core halted and all clocks stopped,Internal LDO Off, Supply monitor off.	I_{DD}		—	0.2	2.1	µA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 24.5 MHz, T_A = 25 °C	—	120	135	µA
High-Frequency Oscillator 1	I_{HFOSC1}	Operating at 72 MHz, T_A = 25 °C	—	1285	1340	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	3.7	6	µA

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

4.1.8 Crystal Oscillator

Table 4.8. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		0.02	—	25	MHz
Crystal Drive Current	I_{XTAL}	XFCN = 0	—	0.5	—	µA
		XFCN = 1	—	1.5	—	µA
		XFCN = 2	—	4.8	—	µA
		XFCN = 3	—	14	—	µA
		XFCN = 4	—	40	—	µA
		XFCN = 5	—	120	—	µA
		XFCN = 6	—	550	—	µA
		XFCN = 7	—	2.6	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Rejection Ratio	$PSRR_{ADC}$	At 1 kHz	—	66	—	dB
		At 1 MHz	—	43	—	dB
DC Performance						
Integral Nonlinearity	INL	14 Bit Mode	-3.5[4]	-1.2 / +5	8.5[4]	LSB
		12 Bit Mode	-1.9	-0.35 / +1	1.9	LSB
		10 Bit Mode	-0.6	±0.2	0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	14 Bit Mode	-1[4]	±1	2.5[4]	LSB
		12 Bit Mode	-0.9	±0.3	0.9	LSB
		10 Bit Mode	-0.5	±0.2	0.5	LSB
Offset Error[5]	E_{OFF}	14 Bit Mode	-8[4]	-2.5	8[4]	LSB
		12 Bit Mode	-2	0	2	LSB
		10 Bit Mode	-1	0	1	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.011	—	LSB/°C
Slope Error	E_M	14 Bit Mode	-15[4]	—	15[4]	LSB
		12 Bit Mode	-2.6	—	2.6	LSB
		10 Bit Mode	-1.1	—	1.1	LSB
Dynamic Performance 10 kHz Sine Wave Input 1 dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	14 Bit Mode	66[4]	72	—	dB
		12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61	—	dB
Signal-to-Noise Plus Distortion	SNDR	14 Bit Mode	66[4]	72	—	dB
		12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	14 Bit Mode	—	-74	—	dB
		12 Bit Mode	—	-72	—	dB
		10 Bit Mode	—	-69	—	dB
Spurious-Free Dynamic Range	SFDR	14 Bit Mode	—	74	—	dB
		12 Bit Mode	—	74	—	dB
		10 Bit Mode	—	71	—	dB

Note:

1. This time is equivalent to four periods of a clock running at 18 MHz + 2%.
2. Conversion Time does not include Tracking Time. Total Conversion Time is:

   Total Conversion Time = [RPT × (ADTK + NUMBITS + 1) × T(SARCLK)] + (T(ADCCLK) × 4)

   where RPT is the number of conversions represented by the ADRPT field and ADCCLK is the clock selected for the ADC.
3. Absolute input pin voltage is limited by the V_{IO} supply.
4. Measured with characterization data and not production tested.
5. The offset is determined using curve fitting since the specification is measured using linear search where the intercept is always positive.

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-chip Precision Reference						
Valid Supply Range	V_{DD}	1.2 V Output	2.2	—	3.6	V
		2.4 V Output	2.7	—	3.6	V
Output Voltage	V_{REFP}	1.2 V Output, V_{DD} = 3.3 V, T = 25 °C	1.195	1.2	1.205	V
		1.2 V Output	1.18	1.2	1.22	V
		2.4 V Output, V_{DD} = 3.3 V, T = 25 °C	2.39	2.4	2.41	V
		2.4 V Output	2.36	2.4	2.44	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 µF tantalum + 0.1 µF ceramic bypass on VREF pin	—	3	—	ms
		0.1 µF ceramic bypass on VREF pin	—	100	—	µs
Load Regulation	LR_{VREFP}	VREF = 2.4 V, Load = 0 to 200 µA to GND	—	8	—	µV/µA
		VREF = 1.2 V, Load = 0 to 200 µA to GND	—	5	—	µV/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to GND	0.1	—	—	µF
Short-circuit current	ISC_{VREFP}		—	—	8	mA
Power Supply Rejection	$PSRR_{VREFP}$		—	75	—	dB
External Reference						
Input Current	I_{EXTREF}	ADC Sample Rate = 1 Msps; VREF = 3.0 V	—	5	—	µA

4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Uncalibrated Offset	V_{OFF}	T_A = 0 °C	—	751	—	mV
Uncalibrated Offset Error[1]	E_{OFF}	T_A = 0 °C	—	19	—	mV
Slope	M		—	2.82	—	mV/°C
Slope Error[1]	E_M		—	29	—	µV/°C
Linearity	LIN	T = 0 °C to 70 °C	—	-0.1 to 0.15	—	°C
		T = -20 °C to 85 °C	—	-0.2 to 0.35	—	°C
		T = -40 °C to 105 °C	—	-0.4 to 0.8	—	°C
Turn-on Time	t_{ON}		—	3.5	—	µs
Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset[2, 3]	E_{TOT}	T = 0 °C to 70 °C	-2.6	—	1.8	°C
		T = -20 °C to 85 °C	-2.9	—	2.7	°C
		T = -40 °C to 105 °C	-3.2	—	4.2	°C

Note:

1. Represents one standard deviation from the mean.
2. The factory-calibrated offset value is stored in the read-only area of flash in locations 0xFFD4 (low byte) and 0xFFD5 (high byte). The 14-bit result represents the output of the ADC when sampling the temp sensor using the 1.65 V internal voltage reference.
3. The temp sensor error includes the offset calibration error, slope error, and linearity error. The values are based upon characterization and are not tested across temperature in production. The values represent three standard deviations above and below the mean. Additional information on achieving high measurement accuracy is available in AN929: Accurate Temperature Sensing with the EFM8 Laser Bee MCU Family.

4.1.12 DACs

Table 4.12. DACs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}			12		Bits
Throughput Rate	f_S		—	—	200	ksps
Integral Nonlinearity	INL	DAC0 and DAC2	-10	-1.77 / 1.56	10	LSB
		DAC1 and DAC3	-11.5	-2.73 / 1.11	11.5	LSB
Differential Nonlinearity	DNL		-1	—	1	LSB
Output Noise	VREF = 2.4 V f_S = 0.1 Hz to 300 kHz		—	110	—	μV_{RMS}
Slew Rate	SLEW		—	±1	—	V/µs
Output Settling Time to 1% Full-scale	t_{SETTLE}	V_{OUT} change between 25% and 75% Full Scale	—	2.6	5	µs
Power-on Time	t_{PWR}		—	—	10	µs
Voltage Reference Range	V_{REF}		1.15	—	V_{DD}	V
Power Supply Rejection Ratio	PSRR	DC, V_{OUT} = 50% Full Scale	—	78	—	dB
Total Harmonic Distortion	THD	V_{OUT} = 10 kHz sine wave, 10% to 90%	54	—	—	dB
Offset Error	E_{OFF}	VREF = 2.4 V	-8	0	8	LSB
Full-Scale Error	E_{FS}	VREF = 2.4 V	-13	±5	13	LSB
External Load Impedance	R_{LOAD}		2	—	—	kΩ
External Load Capacitance[1]	C_{LOAD}		—	—	100	pF
Load Regulation		V_{OUT} = 50% Full Scale I_{OUT} = -2 to 2 mA	—	100	1300	µV/mA

Note:

1. No minimum external load capacitance is required. However, under low loading conditions, it is possible for the DAC output to glitch during start-up. If smooth start-up is required, the minimum loading capacitance at the pin should be a minimum of 10 pF.

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 31 shows a typical connection diagram for the power pins of the device.

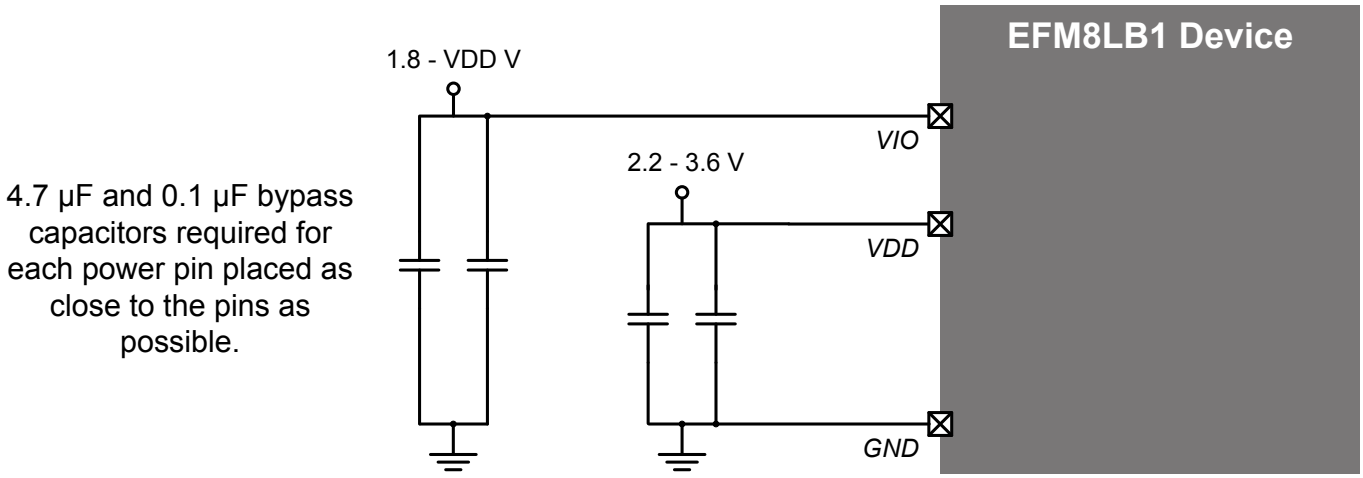


Figure 5.1. Power Connection Diagram

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
29	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8 CLU3B.10	ADC0.2 CMP0P.2 CMP0N.2
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
Center	GND	Ground			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	P3.7 / C2D	Multifunction I/O / C2 Debug Data			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19 CMP1P.8 CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18 CMP1P.7 CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17 CMP1P.6 CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	ADC0.16 CMP1P.5 CMP1N.5
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2

6.3 EFM8LB1x-QFN24 Pin Definitions

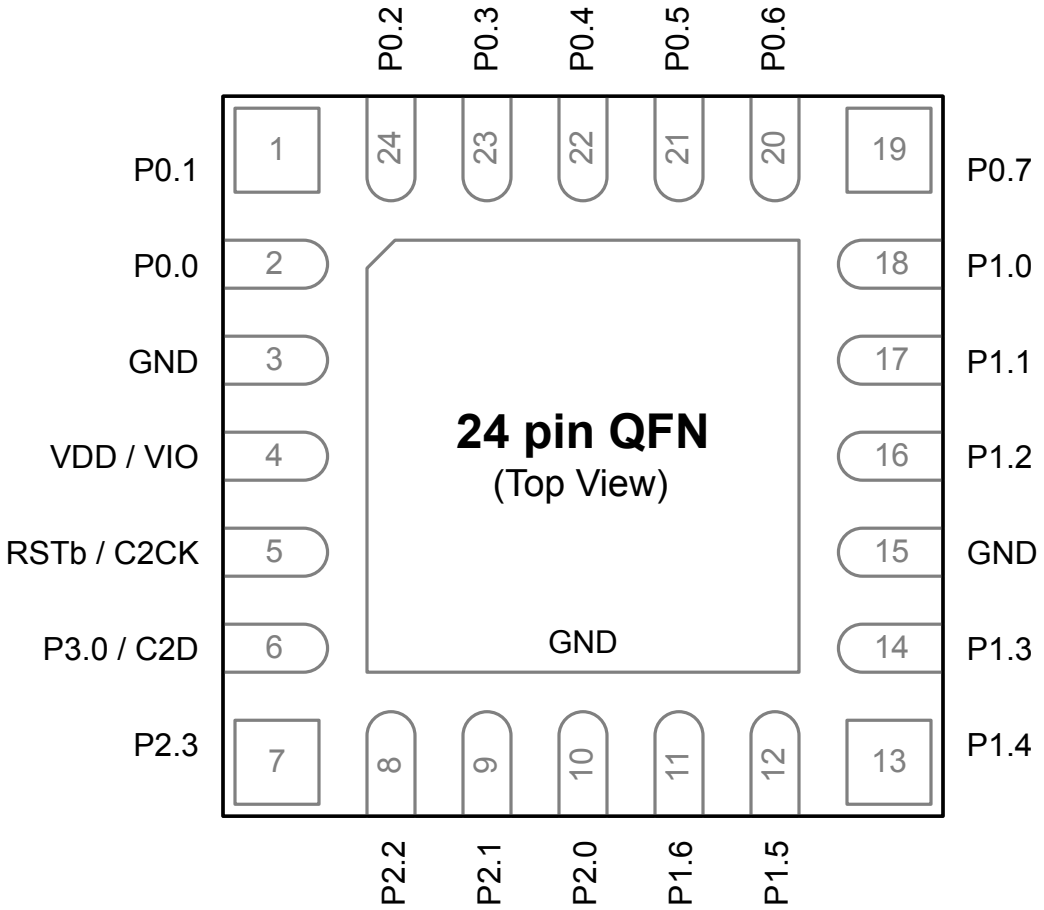


Figure 6.3. EFM8LB1x-QFN24 Pinout

Table 6.3. Pin Definitions for EFM8LB1x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

6.4 EFM8LB1x-QSOP24 Pin Definitions

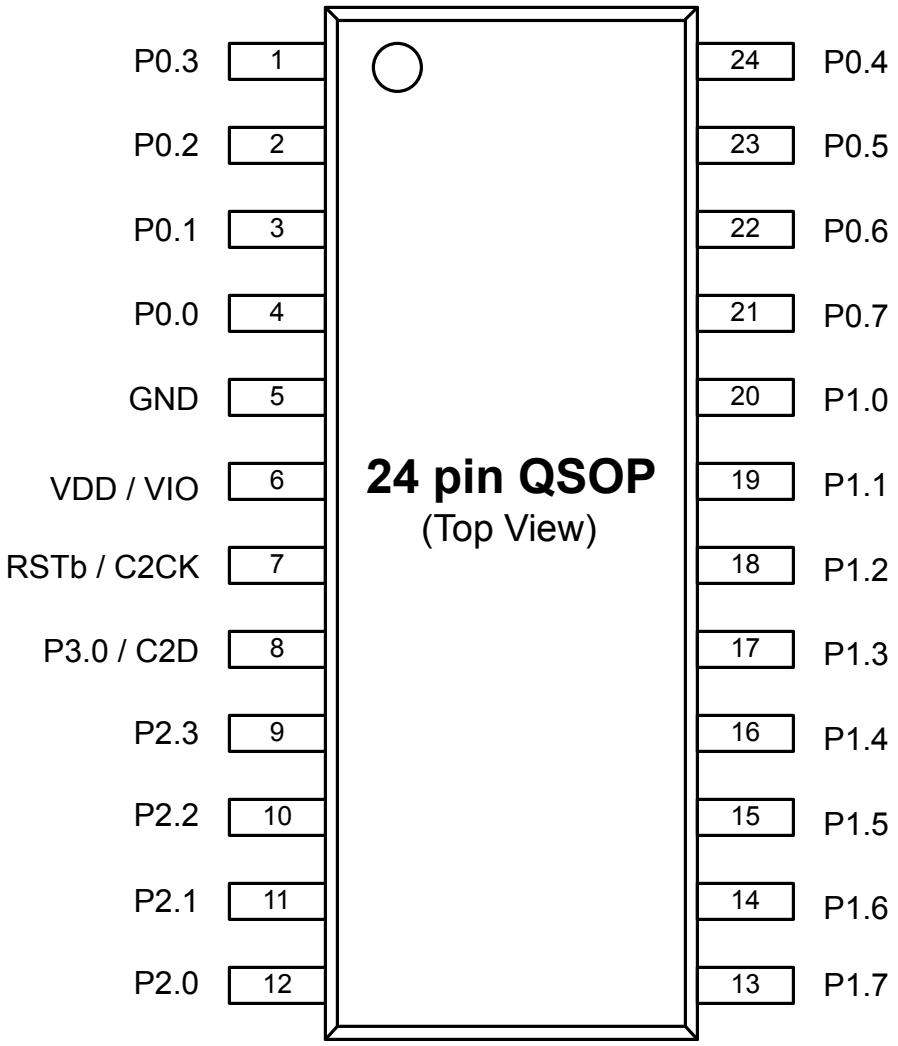


Figure 6.4. EFM8LB1x-QSOP24 Pinout

Table 6.4. Pin Definitions for EFM8LB1x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
11	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
12	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
13	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.12 CMP1P.6 CMP1N.6
14	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5
15	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13	ADC0.10 CMP1P.4 CMP1N.4
16	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12	ADC0.9 CMP1P.3 CMP1N.3
17	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions

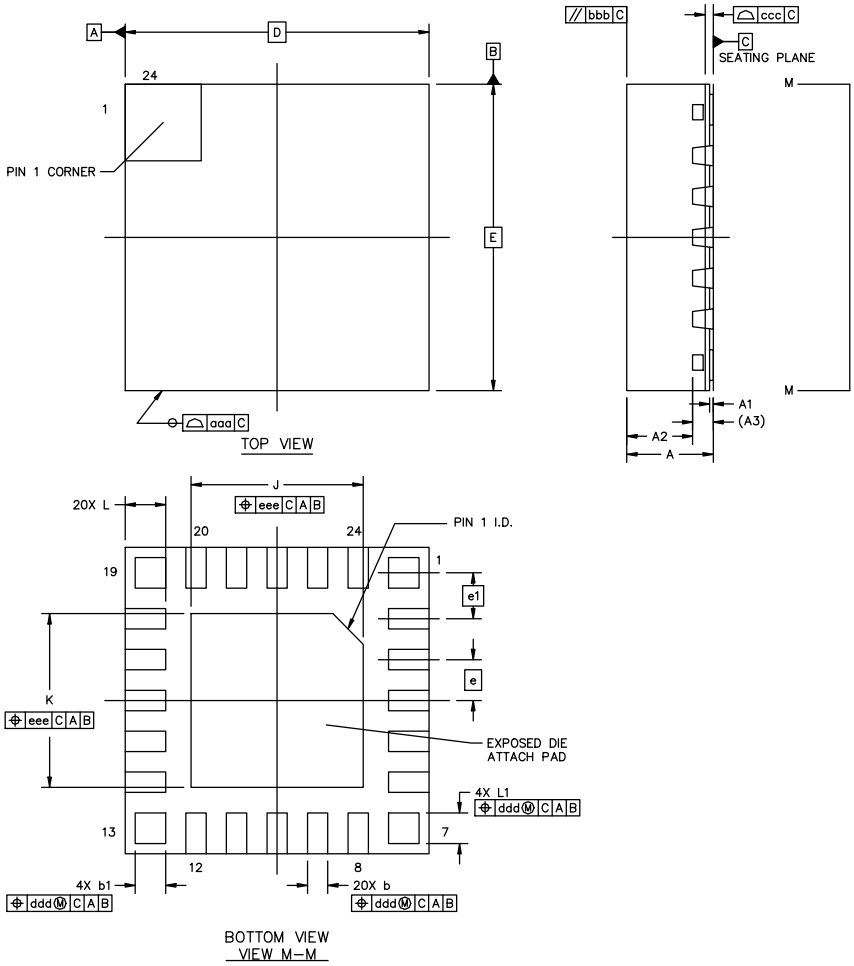


Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D		3.00 BSC	
E		3.00 BSC	

9.2 QFN24 PCB Land Pattern

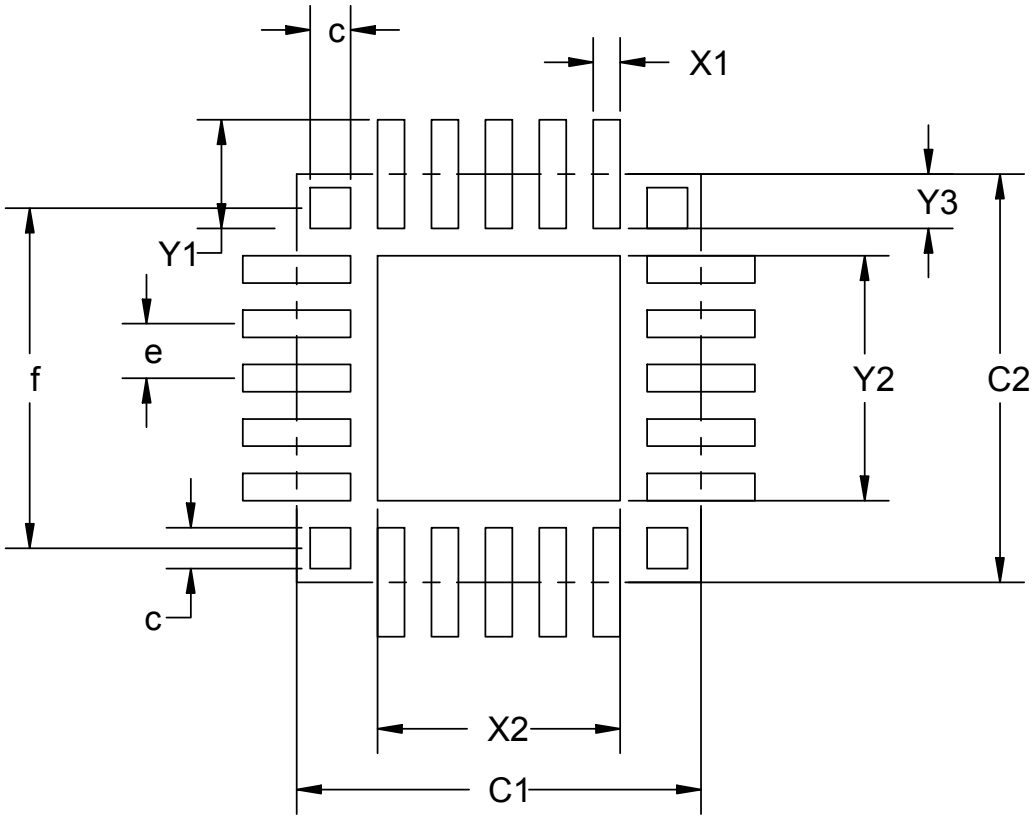


Figure 9.2. QFN24 PCB Land Pattern Drawing

Table 9.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.00	
C2	3.00	
e	0.4 REF	
X1	0.20	
X2	1.80	
Y1	0.80	
Y2	1.80	
Y3	0.4	
f	2.50 REF	
c	0.25	0.35

10. QSOP24 Package Specifications

10.1 QSOP24 Package Dimensions

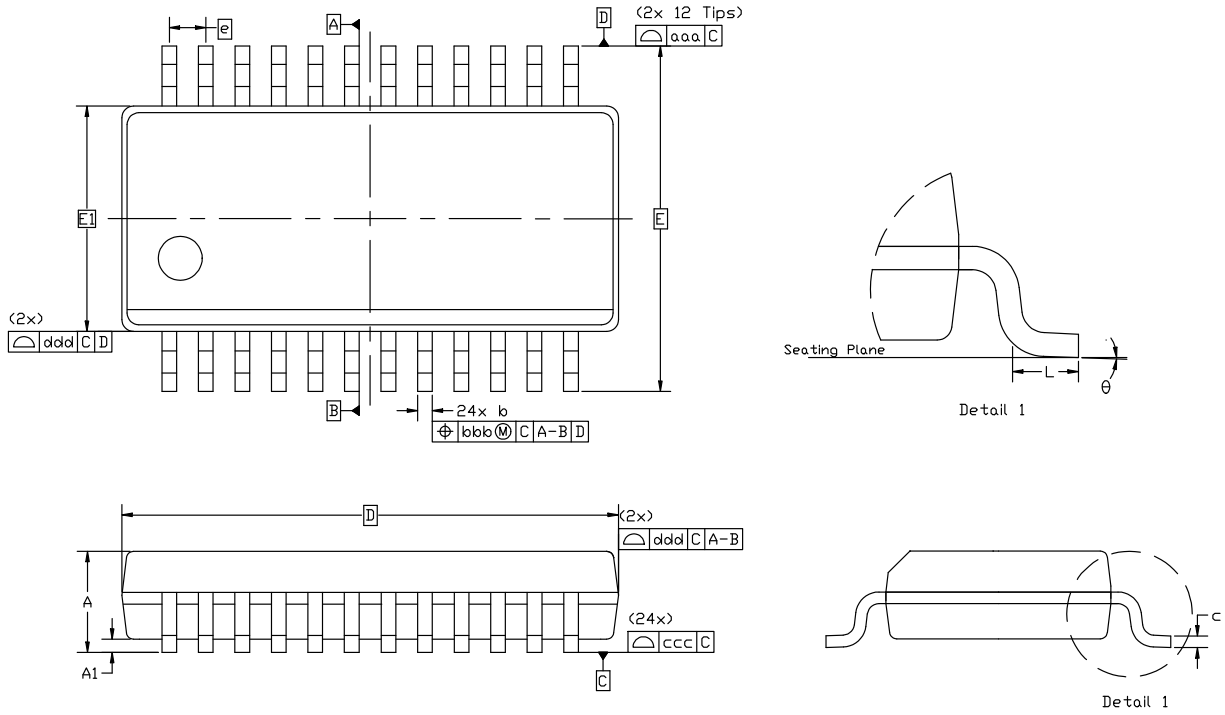
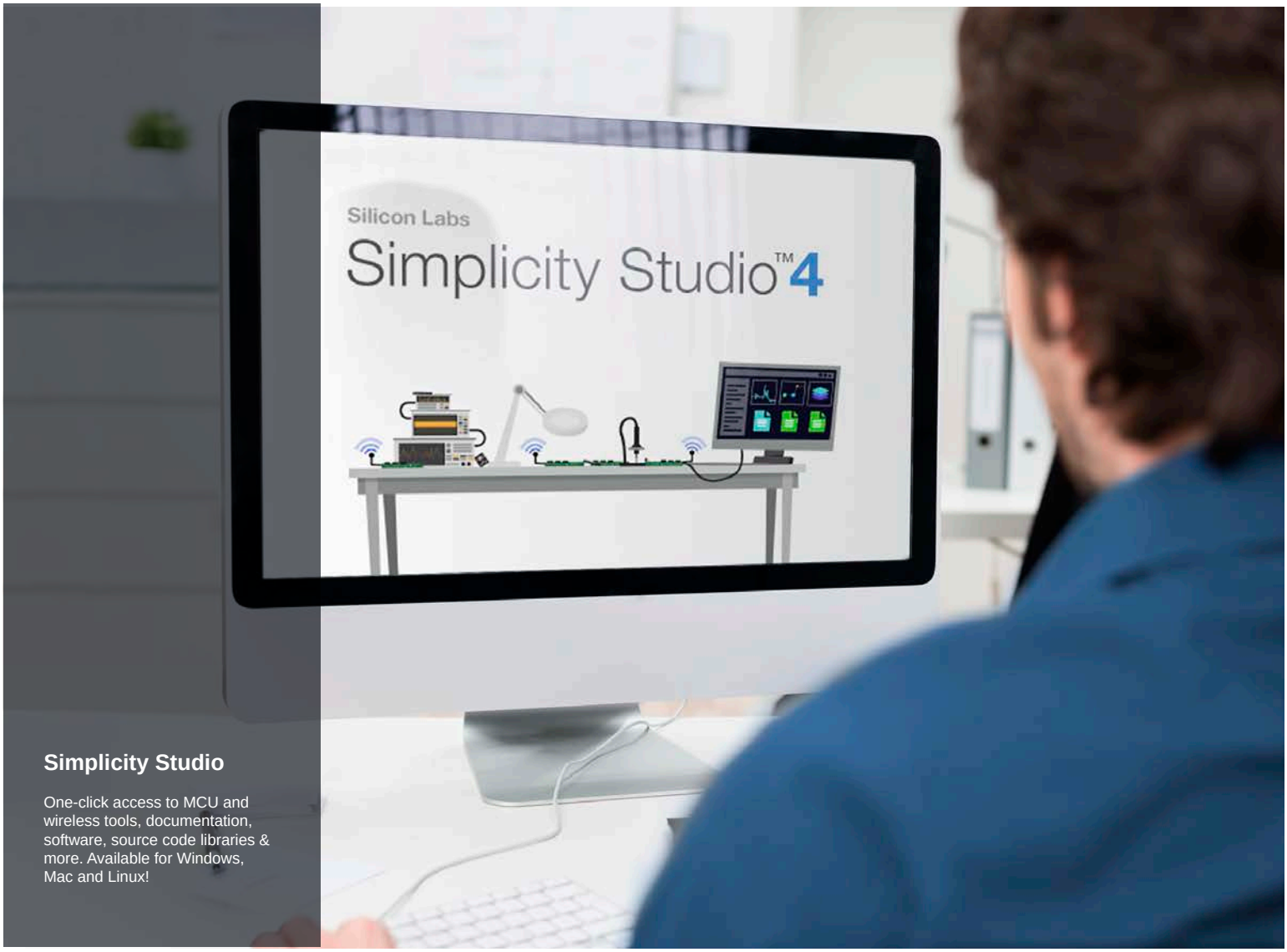


Figure 10.1. QSOP24 Package Drawing

Table 10.1. QSOP24 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27
theta	0°	—	8°



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