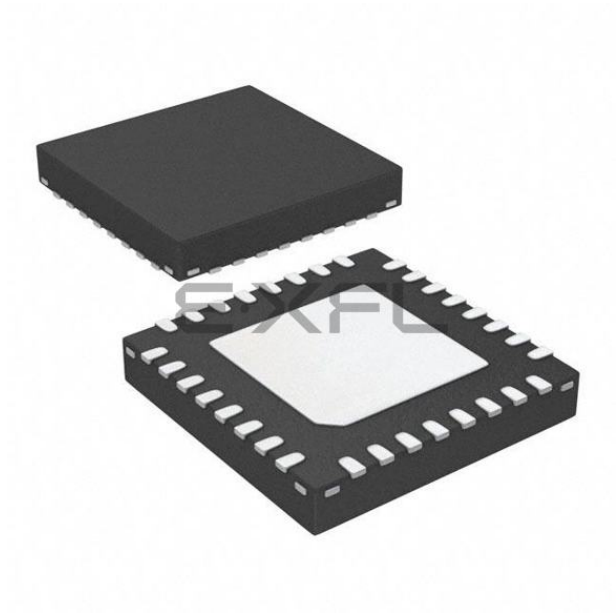
Silicon Labs - EFM8LB12F64E-B-QFN32 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x14b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f64e-b-qfn32

2. Ordering Information

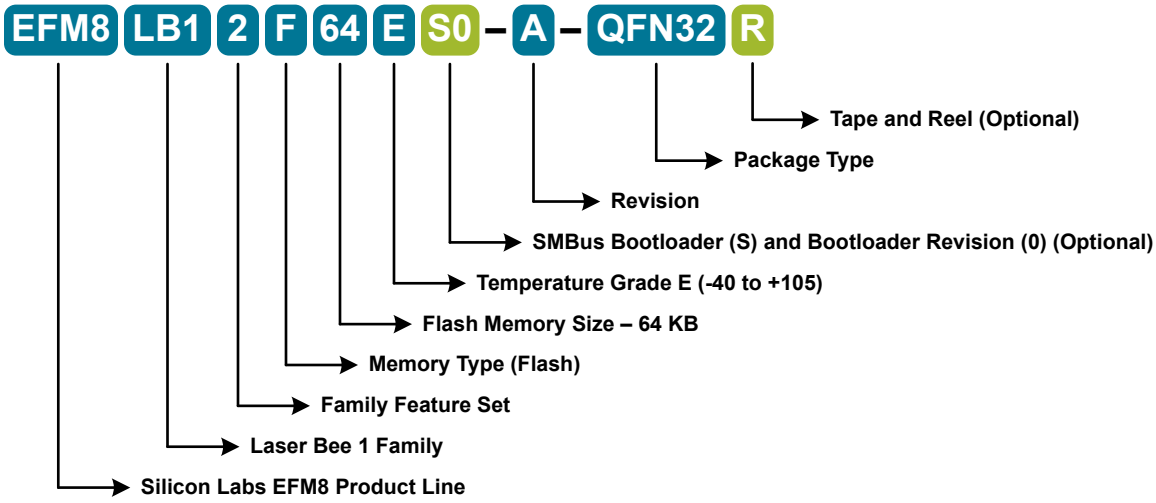

Figure 2.1. EFM8LB1 Part Numbering

All EFM8LB1 family members have the following features:

- CIP-51 Core running up to 72 MHz
- Three Internal Oscillators (72 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- Six 16-bit Timers
- Four Configurable Logic Units
- 14-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, temperature sensor, channel sequencer, and direct-to-XRAM data transfer
- Two Analog Comparators
- 16-bit CRC Unit
- AEC-Q100 qualified (pending)

In addition to these features, each part number in the EFM8LB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Voltage DACs	Comparator 0 Inputs	Comparator 1 Inputs	Bootloader Type	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8LB12F64E-B-QFN32	64	4352	29	20	4	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB12F64E-B-QFP32	64	4352	28	20	4	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB12F64E-B-QFN24	64	4352	20	12	4	6	6	UART	Yes	-40 to +105 °C	QFN24

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Voltage DACs	Comparator 0 Inputs	Comparator 1 Inputs	Bootloader Type	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8LB12F64E-B-QSOP24	64	4352	21	13	4	6	7	UART	Yes	-40 to +105 °C	QSOP24
EFM8LB12F64ES0-B-QFN32	64	4352	29	20	4	10	9	SMBus	Yes	-40 to +105 °C	QFN32
EFM8LB12F64ES0-B-QFN24	64	4352	20	12	4	6	6	SMBus	Yes	-40 to +105 °C	QFN24
EFM8LB12F32E-B-QFN32	32	2304	29	20	4	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB12F32E-B-QFP32	32	2304	28	20	4	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB12F32E-B-QFN24	32	2304	20	12	4	6	6	UART	Yes	-40 to +105 °C	QFN24
EFM8LB12F32E-B-QSOP24	32	2304	21	13	4	6	7	UART	Yes	-40 to +105 °C	QSOP24
EFM8LB12F32ES0-B-QFN32	32	2304	29	20	4	10	9	SMBus	Yes	-40 to +105 °C	QFN32
EFM8LB12F32ES0-B-QFN24	32	2304	20	12	4	6	6	SMBus	Yes	-40 to +105 °C	QFN24
EFM8LB11F32E-B-QFN32	32	2304	29	20	2[1]	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB11F32E-B-QFP32	32	2304	28	20	2[1]	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB11F32E-B-QFN24	32	2304	20	12	2[1]	6	6	UART	Yes	-40 to +105 °C	QFN24
EFM8LB11F32E-B-QSOP24	32	2304	21	13	2[1]	6	7	UART	Yes	-40 to +105 °C	QSOP24
EFM8LB11F32ES0-B-QFN32	32	2304	29	20	2[1]	10	9	SMBus	Yes	-40 to +105 °C	QFN32
EFM8LB11F32ES0-B-QFN24	32	2304	20	12	2[1]	6	6	SMBus	Yes	-40 to +105 °C	QFN24
EFM8LB11F16E-B-QFN32	16	1280	29	20	2[1]	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB11F16E-B-QFP32	16	1280	28	20	2[1]	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB11F16E-B-QFN24	16	1280	20	12	2[1]	6	6	UART	Yes	-40 to +105 °C	QFN24
EFM8LB11F16E-B-QSOP24	16	1280	21	13	2[1]	6	7	UART	Yes	-40 to +105 °C	QSOP24
EFM8LB11F16ES0-B-QFN32	16	1280	29	20	2[1]	10	9	SMBus	Yes	-40 to +105 °C	QFN32
EFM8LB11F16ES0-B-QFN24	16	1280	20	12	2[1]	6	6	SMBus	Yes	-40 to +105 °C	QFN24
EFM8LB10F16E-B-QFN32	16	1280	29	20	0	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB10F16E-B-QFP32	16	1280	28	20	0	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB10F16E-B-QFN24	16	1280	20	12	0	6	6	UART	Yes	-40 to +105 °C	QFN24
EFM8LB10F16E-B-QSOP24	16	1280	21	13	0	6	7	UART	Yes	-40 to +105 °C	QSOP24
EFM8LB10F16ES0-B-QFN32	16	1280	29	20	0	10	9	SMBus	Yes	-40 to +105 °C	QFN32
EFM8LB10F16ES0-B-QFN24	16	1280	20	12	0	6	6	SMBus	Yes	-40 to +105 °C	QFN24

Note:

1. DAC0 and DAC1 are enabled on devices with 2 DACs available.

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	• Core and peripheral clocks halted • HFOSC0 and HFOSC1 oscillators stopped • Regulator in normal bias mode for fast wake • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SUSPEND bit in PCON1	• Timer 4 Event • SPI0 Activity • I2C0 Slave Activity • Port Match Event • Comparator 0 Falling Edge • CLUn Interrupt-Enabled Event
Stop	• All internal power nets shut down • Pins retain state • Exit on any reset source	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Snooze	• Core and peripheral clocks halted • HFOSC0 and HFOSC1 oscillators stopped • Regulator in low bias current mode for energy savings • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SNOOZE bit in PCON1	• Timer 4 Event • SPI0 Activity • I2C0 Slave Activity • Port Match Event • Comparator 0 Falling Edge • CLUn Interrupt-Enabled Event
Shutdown	• All internal power nets shut down • Pins retain state • Exit on pin or power-on reset	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	• RSTb pin reset • Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

3.9 Debugging

The EFM8LB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode-Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 72 MHz (HFOSC1)[2]	—	12.9	15	mA
		F_{SYSCLK} = 24.5 MHz (HFOSC0)[2]	—	4.2	5	mA
		F_{SYSCLK} = 1.53 MHz (HFOSC0)[2]	—	625	1050	µA
		F_{SYSCLK} = 80 kHz[3]	—	155	575	µA
Idle Mode-Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 72 MHz (HFOSC1)[2]	—	9.6	11.1	mA
		F_{SYSCLK} = 24.5 MHz (HFOSC0)[2]	—	3.14	3.8	mA
		F_{SYSCLK} = 1.53 MHz (HFOSC0)[2]	—	520	950	µA
		F_{SYSCLK} = 80 kHz[3]	—	135	550	µA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I_{DD}	LFO Running	—	125	545	µA
		LFO Stopped	—	120	535	µA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I_{DD}	LFO Running	—	23	430	µA
		LFO Stopped	—	19	425	µA
Stop Mode—Core halted and all clocks stopped,Internal LDO On, Supply monitor off.	I_{DD}		—	120	535	µA
Shutdown Mode—Core halted and all clocks stopped,Internal LDO Off, Supply monitor off.	I_{DD}		—	0.2	2.1	µA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 24.5 MHz, T_A = 25 °C	—	120	135	µA
High-Frequency Oscillator 1	I_{HFOSC1}	Operating at 72 MHz, T_A = 25 °C	—	1285	1340	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	3.7	6	µA

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		1.95	2.05	2.15	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to V_{DD} > 2.2 V	10	—	—	µs
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	50	—	µs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} >1 MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1,2]	t_{WRITE}	One Byte, F_{SYSCLK} = 24.5 MHz	19	20	21	µs
Erase Time[1,2]	t_{ERASE}	One Page, F_{SYSCLK} = 24.5 MHz	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming[3]	V_{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
CRC Calculation Time	t_{CRC}	One 256-Byte Block SYSCLK = 48 MHz	—	5.5	—	µs

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{SUS-PENDWK}$	SYSCLK = HFOSC0 CLKDIV = 0x00	—	170	—	ns
Snooze Mode Wake-up Time	$t_{SLEEPWK}$	SYSCLK = HFOSC0 CLKDIV = 0x00	—	12	—	µs

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	PSS_{HFOSC0}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{HFOSC0}	V_{DD} = 3.0 V	—	40	—	ppm/°C
High Frequency Oscillator 1 (72 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	70.5	72	73.5	MHz
Power Supply Sensitivity	PSS_{HFOSC1}	T_A = 25 °C	—	300	—	ppm/V
Temperature Sensitivity	TS_{HFOSC1}	V_{DD} = 3.0 V	—	103	—	ppm/°C
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.0 V	—	65	—	ppm/°C

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-chip Precision Reference						
Valid Supply Range	V_{DD}	1.2 V Output	2.2	—	3.6	V
		2.4 V Output	2.7	—	3.6	V
Output Voltage	V_{REFP}	1.2 V Output, V_{DD} = 3.3 V, T = 25 °C	1.195	1.2	1.205	V
		1.2 V Output	1.18	1.2	1.22	V
		2.4 V Output, V_{DD} = 3.3 V, T = 25 °C	2.39	2.4	2.41	V
		2.4 V Output	2.36	2.4	2.44	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 µF tantalum + 0.1 µF ceramic bypass on VREF pin	—	3	—	ms
		0.1 µF ceramic bypass on VREF pin	—	100	—	µs
Load Regulation	LR_{VREFP}	VREF = 2.4 V, Load = 0 to 200 µA to GND	—	8	—	µV/µA
		VREF = 1.2 V, Load = 0 to 200 µA to GND	—	5	—	µV/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to GND	0.1	—	—	µF
Short-circuit current	ISC_{VREFP}		—	—	8	mA
Power Supply Rejection	$PSRR_{VREFP}$		—	75	—	dB
External Reference						
Input Current	I_{EXTREF}	ADC Sample Rate = 1 Msps; VREF = 3.0 V	—	5	—	µA

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.

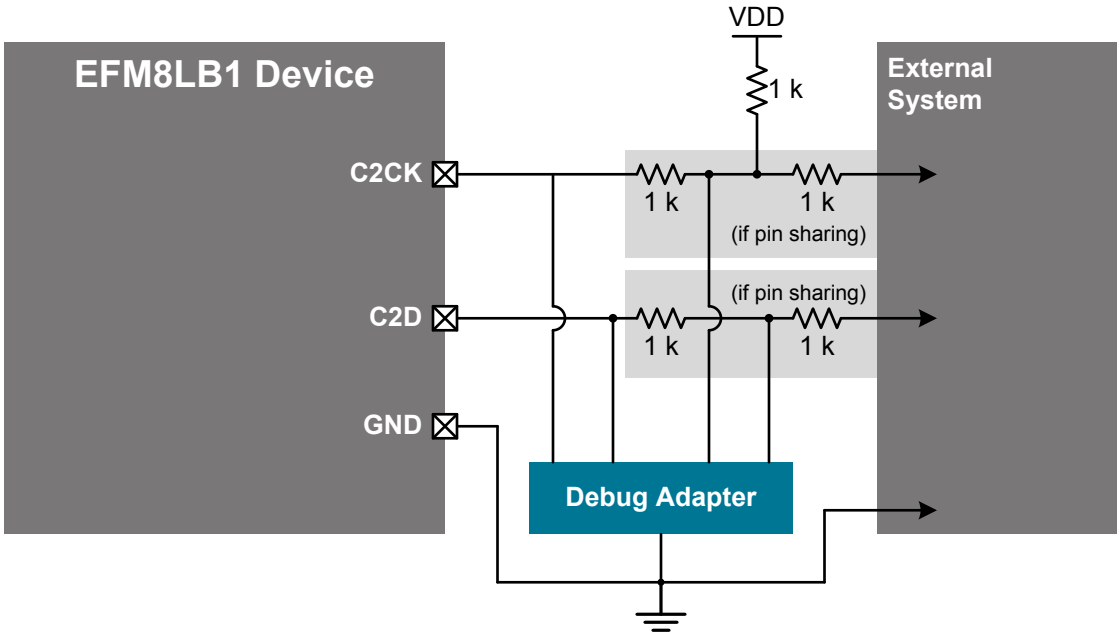

Figure 5.2. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Table 6.1. Pin Definitions for EFM8LB1x-QFN32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	VIO	I/O Supply Power Input			
3	VDD	Supply Power Input			
4	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
5	P3.7 / C2D	Multifunction I/O / C2 Debug Data			
6	P3.4	Multifunction I/O			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19 CMP1P.8 CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18 CMP1P.7 CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17 CMP1P.6 CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	ADC0.16 CMP1P.5 CMP1N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3

6.2 EFM8LB1x-QFP32 Pin Definitions

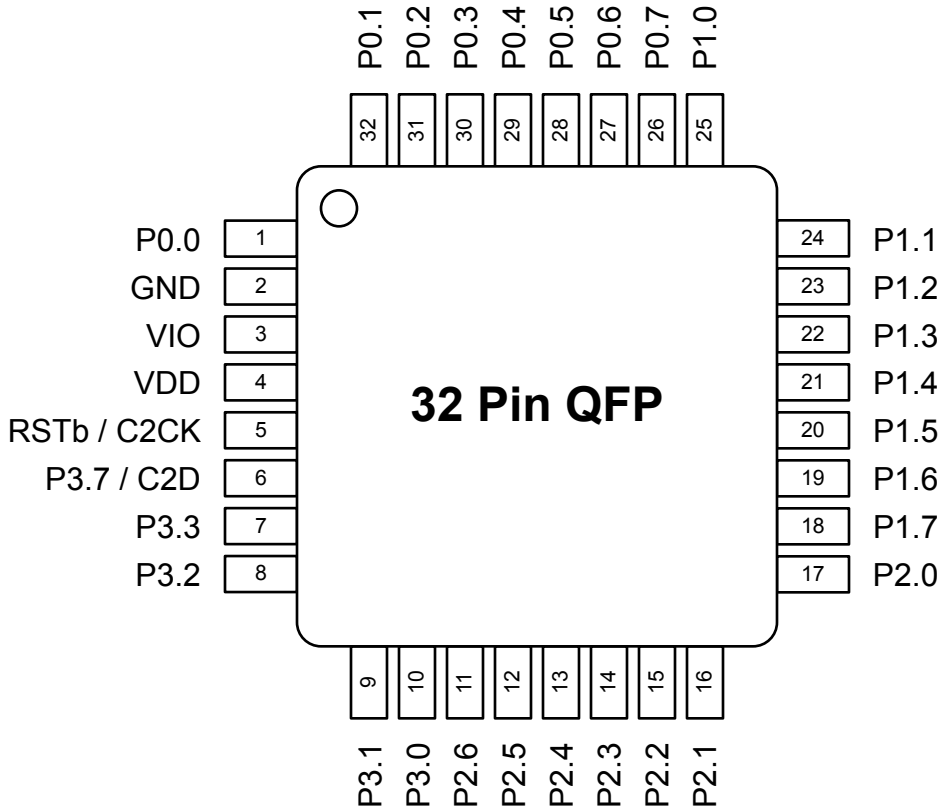

Figure 6.2. EFM8LB1x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8LB1x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
11	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
12	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
13	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.12 CMP1P.6 CMP1N.6
14	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5
15	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13	ADC0.10 CMP1P.4 CMP1N.4
16	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12	ADC0.9 CMP1P.3 CMP1N.3
17	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2

8. QFP32 Package Specifications

8.1 QFP32 Package Dimensions

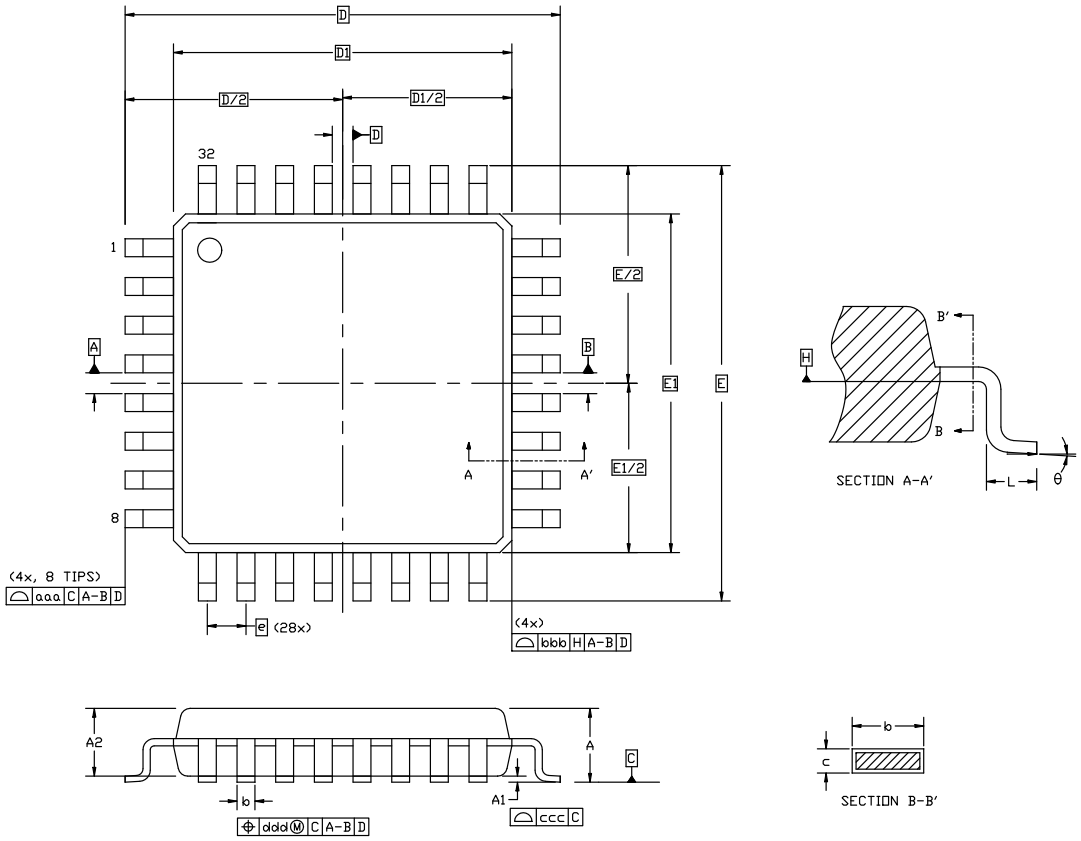

Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.50	0.60	0.70

Dimension	Min	Typ	Max
aaa		0.20	
bbb		0.20	
ccc		0.10	
ddd		0.20	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFP32 PCB Land Pattern

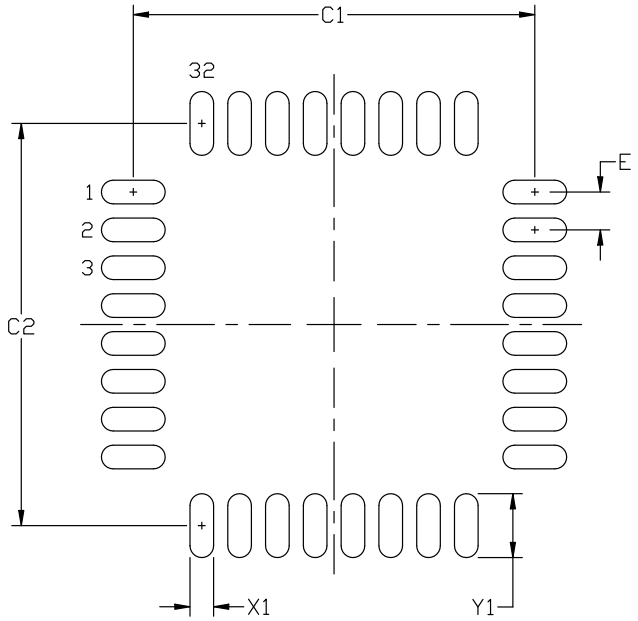

Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.55	
Y1	1.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8.3 QFP32 Package Marking

Figure 8.3. QFP32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions

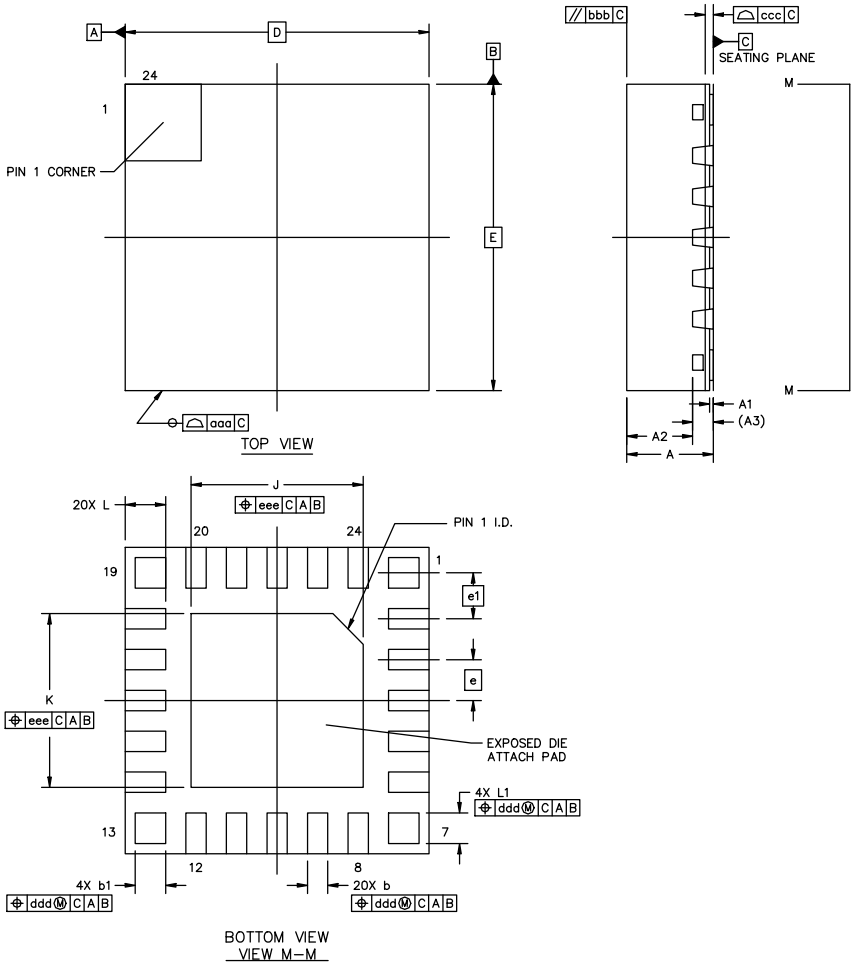

Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D		3.00 BSC	
E		3.00 BSC	

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-782 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 2 x 1 array of 0.7 mm x 1.6 mm openings on a 0.9 mm pitch should be used for the center pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 QFN24 Package Marking

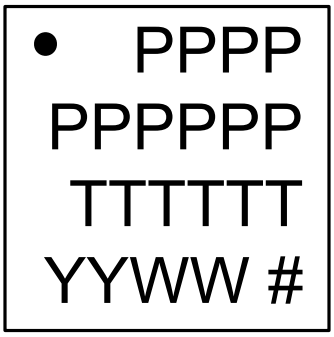

Figure 9.3. QFN24 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).