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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x14b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f64e-b-qfp32r

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	<ul style="list-style-type: none"> Core halted All peripherals clocked and fully operational Code resumes execution on wake event 	Set IDLE bit in PCON0	Any interrupt
Suspend	<ul style="list-style-type: none"> Core and peripheral clocks halted HFOSC0 and HFOSC1 oscillators stopped Regulator in normal bias mode for fast wake Timer 3 and 4 may clock from LFOSC0 Code resumes execution on wake event 	<ol style="list-style-type: none"> Switch SYSCLK to HFOSC0 Set SUSPEND bit in PCON1 	<ul style="list-style-type: none"> Timer 4 Event SPI0 Activity I2C0 Slave Activity Port Match Event Comparator 0 Falling Edge CLUn Interrupt-Enabled Event
Stop	<ul style="list-style-type: none"> All internal power nets shut down Pins retain state Exit on any reset source 	<ol style="list-style-type: none"> Clear STOPCF bit in REG0CN Set STOP bit in PCON0 	Any reset source
Snooze	<ul style="list-style-type: none"> Core and peripheral clocks halted HFOSC0 and HFOSC1 oscillators stopped Regulator in low bias current mode for energy savings Timer 3 and 4 may clock from LFOSC0 Code resumes execution on wake event 	<ol style="list-style-type: none"> Switch SYSCLK to HFOSC0 Set SNOOZE bit in PCON1 	<ul style="list-style-type: none"> Timer 4 Event SPI0 Activity I2C0 Slave Activity Port Match Event Comparator 0 Falling Edge CLUn Interrupt-Enabled Event
Shutdown	<ul style="list-style-type: none"> All internal power nets shut down Pins retain state Exit on pin or power-on reset 	<ol style="list-style-type: none"> Set STOPCF bit in REG0CN Set STOP bit in PCON0 	<ul style="list-style-type: none"> RSTb pin reset Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to $\pm 2\%$ over supply and temperature corners.
- 72 MHz internal oscillator (HFOSC1), accurate to $\pm 2\%$ over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
 - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
 - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0 or comparator 1

Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to $\text{SYSCLK}/2$ (transmit) or $\text{SYSCLK}/8$ (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions
- Dedicated baud rate generator supports baud rates up to $\text{SYSCLK}/2$ (transmit) or $\text{SYSCLK}/8$ (receive)
- 5, 6, 7, 8, or 9 bit data
- Automatic start and stop generation
- Automatic parity generation and checking
- Single-byte buffer on transmit and receive
- Auto-baud detection
- LIN break and sync field detection
- CTS / RTS hardware flow control

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes
- Supports external clock frequencies up to 12 Mbps in master or slave mode
- Support for all clock phase and polarity modes
- 8-bit programmable clock rate (master)
- Programmable receive timeout (slave)
- Two byte FIFO on transmit and receive
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte
- Support for multiple masters on the same data lines

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive FIFOs (one byte) to help increase throughput in faster applications

I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition
- Transmit and receive FIFOs (two byte) to help increase throughput in faster applications
- Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- Asynchronous output may be used to wake from low-power states

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 ⁴	I _{ADC}	High Speed Mode 1 Msps, 12-bit conversions Normal bias settings V _{DD} = 3.0 V	—	1275	1700	μA
		Low Power Mode 350 ksps, 12-bit conversions Low power bias settings V _{DD} = 3.0 V	—	390	530	μA
Internal ADC0 Reference ⁵	I _{VREFFS}	High Speed Mode	—	700	790	μA
		Low Power Mode	—	170	210	μA
On-chip Precision Reference	I _{VREFP}		—	75	—	μA
Temperature Sensor	I _{TSENSE}		—	68	120	μA
Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3) ⁶	I _{DAC}		—	125	—	μA
Comparators (CMP0, CMP1)	I _{CMP}	CPMD = 11	—	0.5	—	μA
		CPMD = 10	—	3	—	μA
		CPMD = 01	—	10	—	μA
		CPMD = 00	—	25	—	μA
Comparator Reference	I _{CPREF}		—	24	—	μA
Voltage Supply Monitor (VMON0)	I _{VMON}		—	15	20	μA

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in low power mode. Total ADC + Reference current will depend on sampling rate.
6. DAC supply current for each enabled DA and not including external load on pin.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCCLKs
Suspend Mode Wake-up Time	$t_{SUS-PENDWK}$	SYSCCLK = HFOSC0 CLKDIV = 0x00	—	170	—	ns
Snooze Mode Wake-up Time	$t_{SLEEPWK}$	SYSCCLK = HFOSC0 CLKDIV = 0x00	—	12	—	μ s

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	PSS_{HFOSC0}	$T_A = 25\text{ }^{\circ}\text{C}$	—	0.5	—	%/V
Temperature Sensitivity	TS_{HFOSC0}	$V_{DD} = 3.0\text{ V}$	—	40	—	ppm/ $^{\circ}\text{C}$
High Frequency Oscillator 1 (72 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	70.5	72	73.5	MHz
Power Supply Sensitivity	PSS_{HFOSC1}	$T_A = 25\text{ }^{\circ}\text{C}$	—	300	—	ppm/V
Temperature Sensitivity	TS_{HFOSC1}	$V_{DD} = 3.0\text{ V}$	—	103	—	ppm/ $^{\circ}\text{C}$
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	$T_A = 25\text{ }^{\circ}\text{C}$	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	$V_{DD} = 3.0\text{ V}$	—	65	—	ppm/ $^{\circ}\text{C}$

4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N _{bits}	14 Bit Mode	14			Bits
		12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f _S	14 Bit Mode	—	—	900	ksps
		12 Bit Mode	—	—	1	Msps
		10 Bit Mode	—	—	1.125	Msps
Throughput Rate (Low Power Mode)	f _S	14 Bit Mode	—	—	320	ksps
		12 Bit Mode	—	—	340	ksps
		10 Bit Mode	—	—	360	ksps
Tracking Time	t _{TRK}	High Speed Mode	217.8 ¹	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t _{PWR}		1.2	—	—	μs
SAR Clock Frequency	f _{SAR}	High Speed Mode	—	—	18.36	MHz
		Low Power Mode	—	—	12.25	MHz
Conversion Time ²	t _{CNV}	14-Bit Conversion, SAR Clock =18 MHz, System Clock = 72 MHz.	0.81			μs
		12-Bit Conversion, SAR Clock =18 MHz, System Clock = 72 MHz.	0.7			μs
		10-Bit Conversion, SAR Clock =18 MHz, System Clock = 72 MHz.	0.59			μs
Sample/Hold Capacitor	C _{SAR}	Gain = 1	—	5.2	—	pF
		Gain = 0.75	—	3.9	—	pF
		Gain = 0.5	—	2.6	—	pF
		Gain = 0.25	—	1.3	—	pF
Input Pin Capacitance	C _{IN}	High Quality Input	—	20	—	pF
		Normal Input	—	20	—	pF
Input Mux Impedance	R _{MUX}	High Quality Input	—	330	—	Ω
		Normal Input	—	550	—	Ω
Voltage Reference Range	V _{REF}		1	—	V _{IO}	V
Input Voltage Range ³	V _{IN}		0	—	V _{REF} / Gain	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Rejection Ratio	PSRR _{ADC}	At 1 kHz	—	66	—	dB
		At 1 MHz	—	43	—	dB
DC Performance						
Integral Nonlinearity	INL	14 Bit Mode	-3.5 ⁴	-1.2 / +5	8.5 ⁴	LSB
		12 Bit Mode	-1.9	-0.35 / +1	1.9	LSB
		10 Bit Mode	-0.6	±0.2	0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	14 Bit Mode	-1 ⁴	±1	2.5 ⁴	LSB
		12 Bit Mode	-0.9	±0.3	0.9	LSB
		10 Bit Mode	-0.5	±0.2	0.5	LSB
Offset Error ⁵	E _{OFF}	14 Bit Mode	-8 ⁴	-2.5	8 ⁴	LSB
		12 Bit Mode	-2	0	2	LSB
		10 Bit Mode	-1	0	1	LSB
Offset Temperature Coefficient	TC _{OFF}		—	0.011	—	LSB/°C
Slope Error	E _M	14 Bit Mode	-15 ⁴	—	15 ⁴	LSB
		12 Bit Mode	-2.6	—	2.6	LSB
		10 Bit Mode	-1.1	—	1.1	LSB
Dynamic Performance 10 kHz Sine Wave Input 1 dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	14 Bit Mode	66 ⁴	72	—	dB
		12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61	—	dB
Signal-to-Noise Plus Distortion	SNDR	14 Bit Mode	66 ⁴	72	—	dB
		12 Bit Mode	64	68	—	dB
		10 Bit Mode	59	61	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	14 Bit Mode	—	-74	—	dB
		12 Bit Mode	—	-72	—	dB
		10 Bit Mode	—	-69	—	dB
Spurious-Free Dynamic Range	SFDR	14 Bit Mode	—	74	—	dB
		12 Bit Mode	—	74	—	dB
		10 Bit Mode	—	71	—	dB

Note:

1. This time is equivalent to four periods of a clock running at 18 MHz + 2%.
2. Conversion Time does not include Tracking Time. Total Conversion Time is:

$$\text{Total Conversion Time} = [\text{RPT} \times (\text{ADTK} + \text{NUMBITS} + 1) \times \text{T}(\text{SARCLK})] + (\text{T}(\text{ADCCLK}) \times 4)$$

where RPT is the number of conversions represented by the ADRPT field and ADCCLK is the clock selected for the ADC.
3. Absolute input pin voltage is limited by the V_{IO} supply.
4. Measured with characterization data and not production tested.
5. The offset is determined using curve fitting since the specification is measured using linear search where the intercept is always positive.

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	μs
Power Supply Rejection	$PSRR_{\text{REFFS}}$		—	400	—	ppm/V
On-chip Precision Reference						
Valid Supply Range	V_{DD}	1.2 V Output	2.2	—	3.6	V
		2.4 V Output	2.7	—	3.6	V
Output Voltage	V_{REFP}	1.2 V Output, $V_{\text{DD}} = 3.3 \text{ V}$, $T = 25 \text{ °C}$	1.195	1.2	1.205	V
		1.2 V Output	1.18	1.2	1.22	V
		2.4 V Output, $V_{\text{DD}} = 3.3 \text{ V}$, $T = 25 \text{ °C}$	2.39	2.4	2.41	V
		2.4 V Output	2.36	2.4	2.44	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin	—	3	—	ms
		0.1 μF ceramic bypass on VREF pin	—	100	—	μs
Load Regulation	LR_{VREFP}	$V_{\text{REF}} = 2.4 \text{ V}$, Load = 0 to 200 μA to GND	—	8	—	μV/μA
		$V_{\text{REF}} = 1.2 \text{ V}$, Load = 0 to 200 μA to GND	—	5	—	μV/μA
Load Capacitor	C_{VREFP}	Load = 0 to 200 μA to GND	0.1	—	—	μF
Short-circuit current	ISC_{VREFP}		—	—	8	mA
Power Supply Rejection	$PSRR_{\text{VREFP}}$		—	75	—	dB
External Reference						
Input Current	I_{EXTREF}	ADC Sample Rate = 1 Msps; $V_{\text{REF}} = 3.0 \text{ V}$	—	5	—	μA

4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Uncalibrated Offset	V_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	751	—	mV
Uncalibrated Offset Error ¹	E_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	19	—	mV
Slope	M		—	2.82	—	mV/ $^{\circ}\text{C}$
Slope Error ¹	E_M		—	29	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity	LIN	$T = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$	—	-0.1 to 0.15	—	$^{\circ}\text{C}$
		$T = -20\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	—	-0.2 to 0.35	—	$^{\circ}\text{C}$
		$T = -40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$	—	-0.4 to 0.8	—	$^{\circ}\text{C}$
Turn-on Time	t_{ON}		—	3.5	—	μs
Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset ^{2, 3}	E_{TOT}	$T = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$	-2.6	—	1.8	$^{\circ}\text{C}$
		$T = -20\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	-2.9	—	2.7	$^{\circ}\text{C}$
		$T = -40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$	-3.2	—	4.2	$^{\circ}\text{C}$

Note:

1. Represents one standard deviation from the mean.
2. The factory-calibrated offset value is stored in the read-only area of flash in locations 0xFFD4 (low byte) and 0xFFD5 (high byte). The 14-bit result represents the output of the ADC when sampling the temp sensor using the 1.65 V internal voltage reference.
3. The temp sensor error includes the offset calibration error, slope error, and linearity error. The values are based upon characterization and are not tested across temperature in production. The values represent three standard deviations above and below the mean. Additional information on achieving high measurement accuracy is available in AN929: Accurate Temperature Sensing with the EFM8 Laser Bee MCU Family.

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 31 shows a typical connection diagram for the power pins of the device.

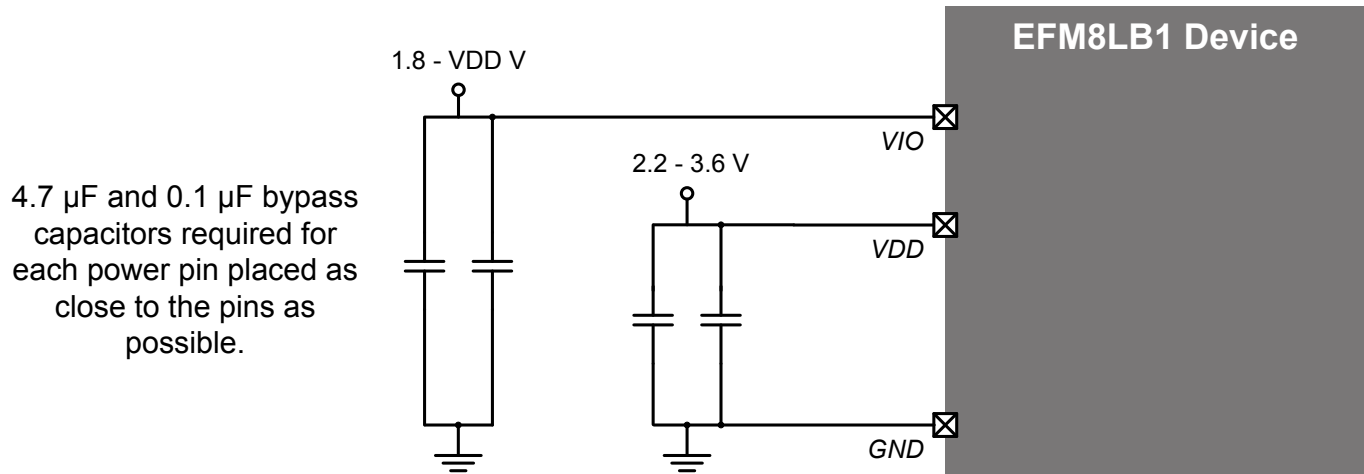


Figure 5.1. Power Connection Diagram

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7

6.3 EFM8LB1x-QFN24 Pin Definitions

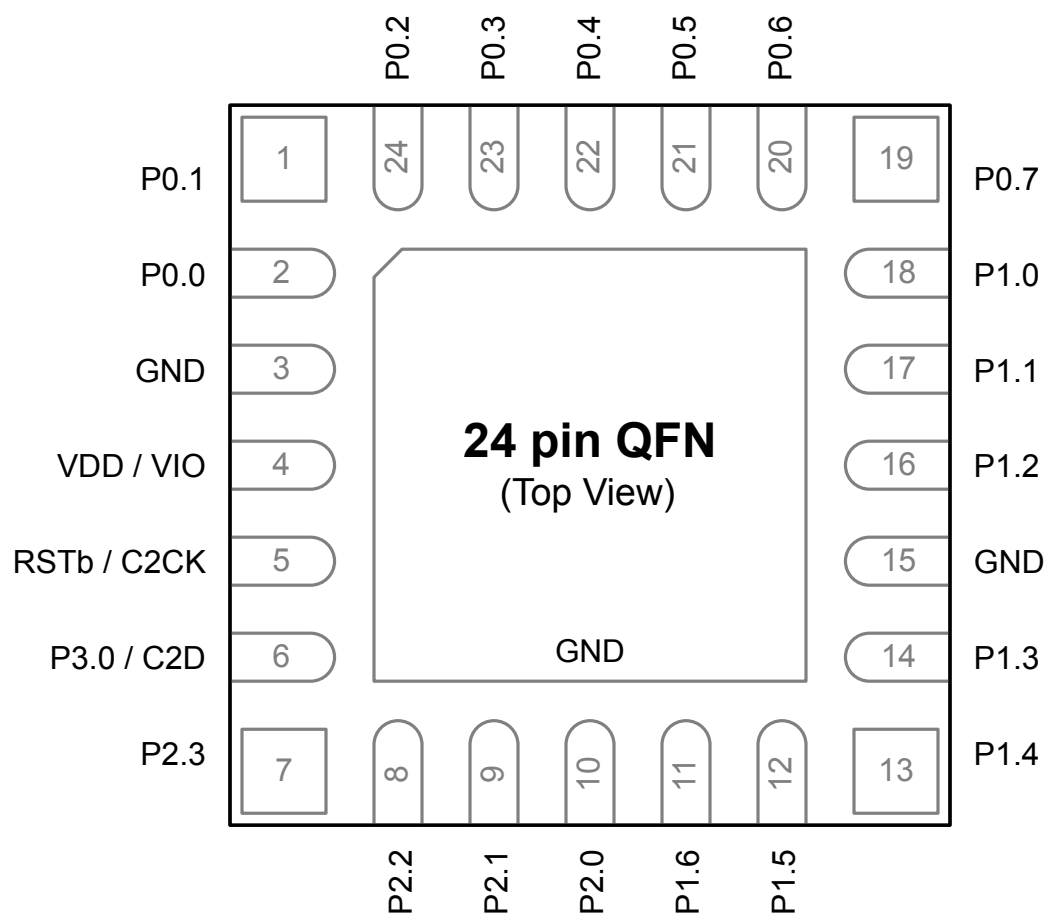


Figure 6.3. EFM8LB1x-QFN24 Pinout

Table 6.3. Pin Definitions for EFM8LB1x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Dimension	Min	Typ	Max
e	0.40 BSC		
e1	0.45 BSC		
J	1.60	1.70	1.80
K	1.60	1.70	1.80
L	0.35	0.40	0.45
L1	0.25	0.30	0.35
aaa	—	0.10	—
bbb	—	0.10	—
ccc	—	0.08	—
ddd	—	0.1	—
eee	—	0.1	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-248 but includes custom features which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Dimension	Min	Typ	Max
aaa		0.20	
bbb		0.18	
ccc		0.10	
ddd		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 QSOP24 PCB Land Pattern

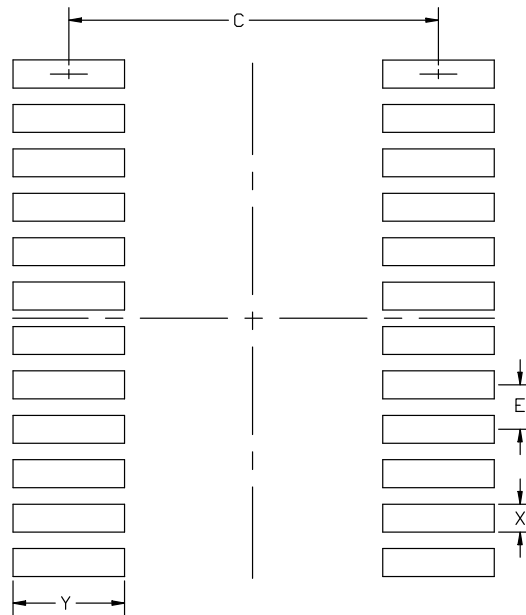


Figure 10.2. QSOP24 PCB Land Pattern Drawing

Table 10.2. QSOP24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.3 QSOP24 Package Marking



Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

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