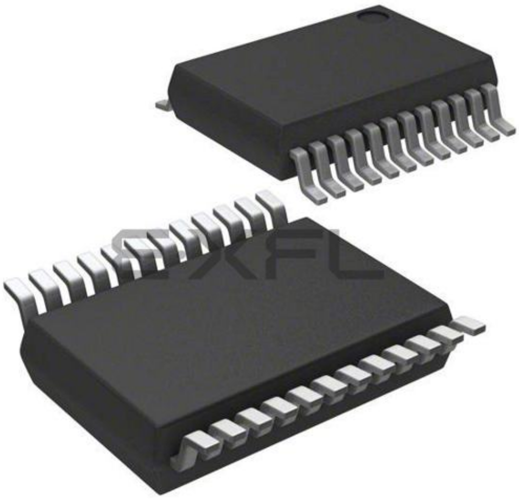

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 13x14b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f64e-b-qsop24

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	• Core and peripheral clocks halted • HFOSC0 and HFOSC1 oscillators stopped • Regulator in normal bias mode for fast wake • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SUSPEND bit in PCON1	• Timer 4 Event • SPI0 Activity • I2C0 Slave Activity • Port Match Event • Comparator 0 Falling Edge • CLUn Interrupt-Enabled Event
Stop	• All internal power nets shut down • Pins retain state • Exit on any reset source	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Snooze	• Core and peripheral clocks halted • HFOSC0 and HFOSC1 oscillators stopped • Regulator in low bias current mode for energy savings • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SNOOZE bit in PCON1	• Timer 4 Event • SPI0 Activity • I2C0 Slave Activity • Port Match Event • Comparator 0 Falling Edge • CLUn Interrupt-Enabled Event
Shutdown	• All internal power nets shut down • Pins retain state • Exit on pin or power-on reset	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	• RSTb pin reset • Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 14, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.2	—	3.6	V
Operating Supply Voltage on VIO[2, 3]	V_{IO}		2.2	—	V_{DD}	V
System Clock Frequency	f_{SYSCLK}		0	—	73.5	MHz
Operating Ambient Temperature	T_A		-40	—	105	°C

Note:
1. All voltages with respect to GND
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.
3. GPIO levels are undefined whenever VIO is less than 1 V.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		1.95	2.05	2.15	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to V_{DD} > 2.2 V	10	—	—	µs
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	50	—	µs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} >1 MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1,2]	t_{WRITE}	One Byte, F_{SYSCLK} = 24.5 MHz	19	20	21	µs
Erase Time[1,2]	t_{ERASE}	One Page, F_{SYSCLK} = 24.5 MHz	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming[3]	V_{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
CRC Calculation Time	t_{CRC}	One 256-Byte Block SYSCLK = 48 MHz	—	5.5	—	µs

Note:
1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

4.1.8 Crystal Oscillator

Table 4.8. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		0.02	—	25	MHz
Crystal Drive Current	I_{XTAL}	XFCN = 0	—	0.5	—	μA
		XFCN = 1	—	1.5	—	μA
		XFCN = 2	—	4.8	—	μA
		XFCN = 3	—	14	—	μA
		XFCN = 4	—	40	—	μA
		XFCN = 5	—	120	—	μA
		XFCN = 6	—	550	—	μA
		XFCN = 7	—	2.6	—	mA

4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	14 Bit Mode		14		Bits
		12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate (High Speed Mode)	f_S	14 Bit Mode	—	—	900	ksps
		12 Bit Mode	—	—	1	Msps
		10 Bit Mode	—	—	1.125	Msps
Throughput Rate (Low Power Mode)	f_S	14 Bit Mode	—	—	320	ksps
		12 Bit Mode	—	—	340	ksps
		10 Bit Mode	—	—	360	ksps
Tracking Time	t_{TRK}	High Speed Mode	217.8[1]	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t_{PWR}		1.2	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	18.36	MHz
		Low Power Mode	—	—	12.25	MHz
Conversion Time[2]	t_{CNV}	14-Bit Conversion, SAR Clock =18 MHz, System Clock = 72 MHz.		0.81		µs
		12-Bit Conversion, SAR Clock =18 MHz, System Clock = 72 MHz.		0.7		µs
		10-Bit Conversion, SAR Clock =18 MHz, System Clock = 72 MHz.		0.59		µs
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5.2	—	pF
		Gain = 0.75	—	3.9	—	pF
		Gain = 0.5	—	2.6	—	pF
		Gain = 0.25	—	1.3	—	pF
Input Pin Capacitance	C_{IN}	High Quality Input	—	20	—	pF
		Normal Input	—	20	—	pF
Input Mux Impedance	R_{MUX}	High Quality Input	—	330	—	Ω
		Normal Input	—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{IO}	V
Input Voltage Range[3]	V_{IN}		0	—	V_{REF} / Gain	V

4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Uncalibrated Offset	V_{OFF}	T_A = 0 °C	—	751	—	mV
Uncalibrated Offset Error[1]	E_{OFF}	T_A = 0 °C	—	19	—	mV
Slope	M		—	2.82	—	mV/°C
Slope Error[1]	E_M		—	29	—	µV/°C
Linearity	LIN	T = 0 °C to 70 °C	—	-0.1 to 0.15	—	°C
		T = -20 °C to 85 °C	—	-0.2 to 0.35	—	°C
		T = -40 °C to 105 °C	—	-0.4 to 0.8	—	°C
Turn-on Time	t_{ON}		—	3.5	—	µs
Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset[2, 3]	E_{TOT}	T = 0 °C to 70 °C	-2.6	—	1.8	°C
		T = -20 °C to 85 °C	-2.9	—	2.7	°C
		T = -40 °C to 105 °C	-3.2	—	4.2	°C

Note:

1. Represents one standard deviation from the mean.
2. The factory-calibrated offset value is stored in the read-only area of flash in locations 0xFFD4 (low byte) and 0xFFD5 (high byte). The 14-bit result represents the output of the ADC when sampling the temp sensor using the 1.65 V internal voltage reference.
3. The temp sensor error includes the offset calibration error, slope error, and linearity error. The values are based upon characterization and are not tested across temperature in production. The values represent three standard deviations above and below the mean. Additional information on achieving high measurement accuracy is available in AN929: Accurate Temperature Sensing with the EFM8 Laser Bee MCU Family.

4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	I_{OH} = -7 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -3.3 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (High Drive)	V_{OL}	I_{OL} = 13.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 7 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 3.6 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Output High Voltage (Low Drive)	V_{OH}	I_{OH} = -4.75 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -2.25 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OH} = -1.2 mA, 1.71 V ≤ V_{IO} < 2.2 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	I_{OL} = 6.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 3.5 mA, 2.2 V ≤ V_{IO} < 3.0 V I_{OL} = 1.8 mA, 1.71 V ≤ V_{IO} < 2.2 V	—	—	V_{IO} x 0.2	V
Input High Voltage	V_{IH}		0.7 x V_{IO}	—	—	V
Input Low Voltage	V_{IL}		—	—	0.3 x V_{IO}	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	-30	-20	-10	μA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{IO}	-1.1	—	4	μA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	V_{IO} < V_{IN} < V_{IO}+2.5 V Any pin except P3.0, P3.1, P3.2, or P3.3	0	5	150	μA

4.1.16 SMBus

Table 4.16. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	70[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	µs
Data Hold Time	$t_{HD:DAT}$		0	—	—	µs
Data Setup Time	$t_{SU:DAT}$		4.7	—	—	µs
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	µs
Clock High Period	t_{HIGH}		9.4	—	50[3]	µs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	256[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	256[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	µs
Data Hold Time	$t_{HD:DAT}$		0	—	—	µs
Data Setup Time	$t_{SU:DAT}$		1.3	—	—	µs
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	µs
Clock High Period	t_{HIGH}		2.6	—	50[3]	µs

Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
3. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.

Table 4.17. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	f_{CSO} / 3
Bus Free Time Between STOP and START Conditions	t_{BUF}	2 / f_{CSO}
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	1 / f_{CSO}
Repeated START Condition Setup Time	$t_{SU:STA}$	2 / f_{CSO}
STOP Condition Setup Time	$t_{SU:STO}$	2 / f_{CSO}
Clock Low Period	t_{LOW}	1 / f_{CSO}
Clock High Period	t_{HIGH}	2 / f_{CSO}

Note:

1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

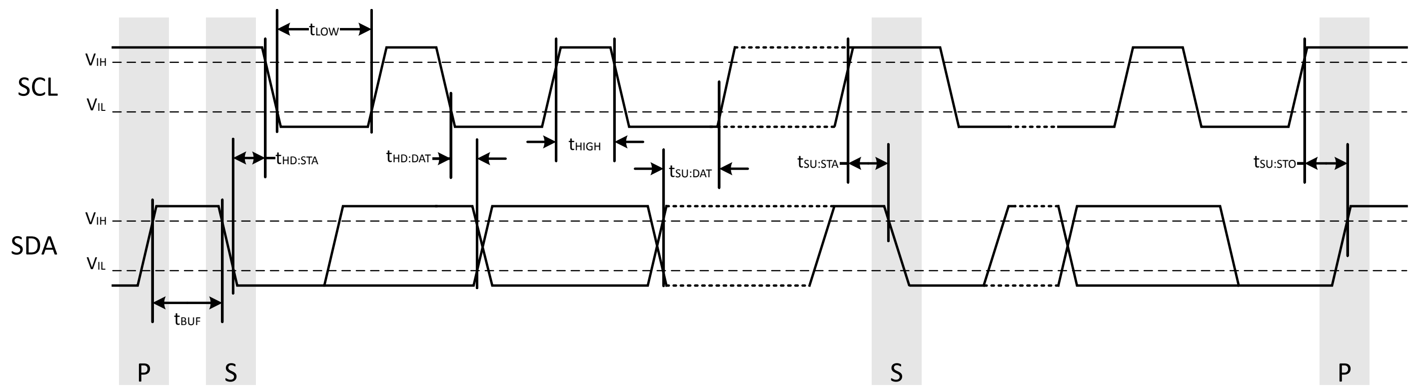

Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFN24 Packages	—	30	—	°C/W
		QFN32 Packages	—	26	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QSOP24 Packages	—	65	—	°C/W

Note:

1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

6. Pin Definitions

6.1 EFM8LB1x-QFN32 Pin Definitions

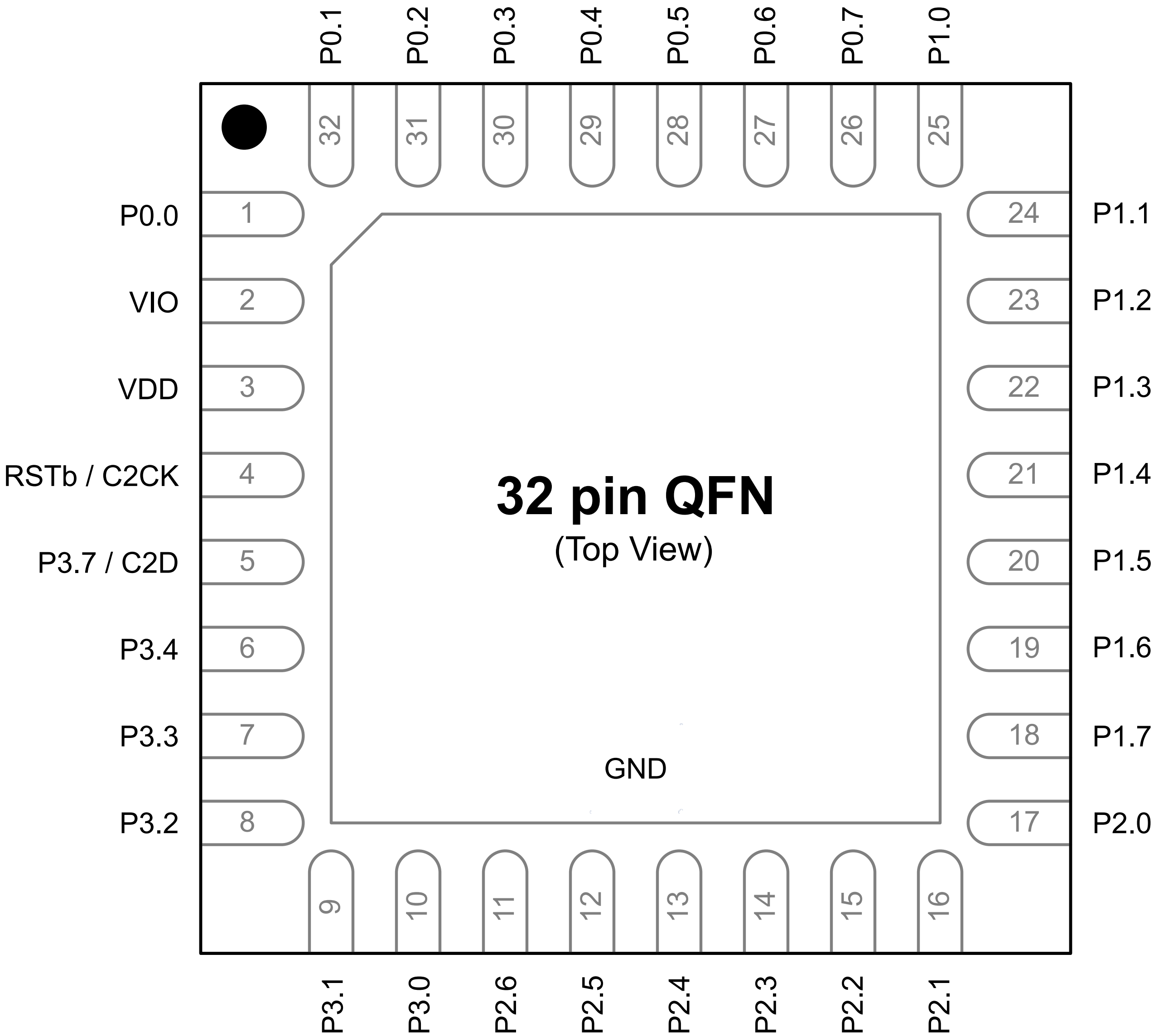

Figure 6.1. EFM8LB1x-QFN32 Pinout

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4
28	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART0_RX CLU0B.10 CLU1A.9 CLU3B.11	ADC0.3 CMP0P.3 CMP0N.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13	ADC0.10 CMP1P.4 CMP1N.4
13	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12	ADC0.9 CMP1P.3 CMP1N.3
14	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2
15	GND	Ground			
16	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8
17	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7
18	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0A.12 CLU1A.10 CLU2A.10 CLU3B.12	ADC0.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
Center	GND	Ground			

Dimension	Min	Typ	Max
aaa		0.20	
bbb		0.20	
ccc		0.10	
ddd		0.20	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions

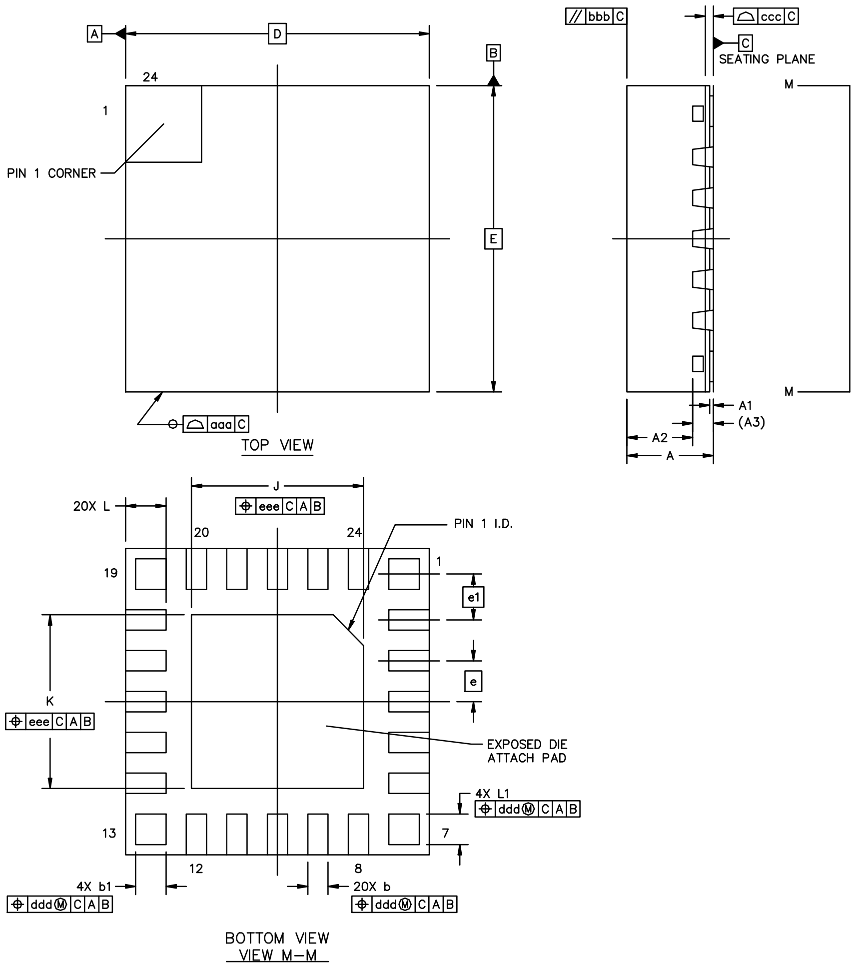

Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D		3.00 BSC	
E		3.00 BSC	

Dimension	Min	Max

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-782 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 2 x 1 array of 0.7 mm x 1.6 mm openings on a 0.9 mm pitch should be used for the center pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 QFN24 Package Marking

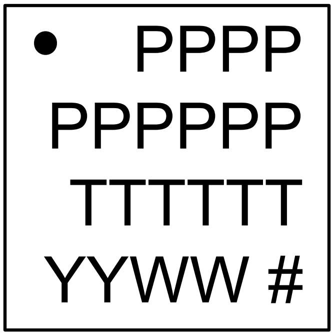

Figure 9.3. QFN24 Package Marking

The package marking consists of:
- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Dimension	Min	Typ	Max
aaa		0.20	
bbb		0.18	
ccc		0.10	
ddd		0.10	

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.3 QSOP24 Package Marking

Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

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