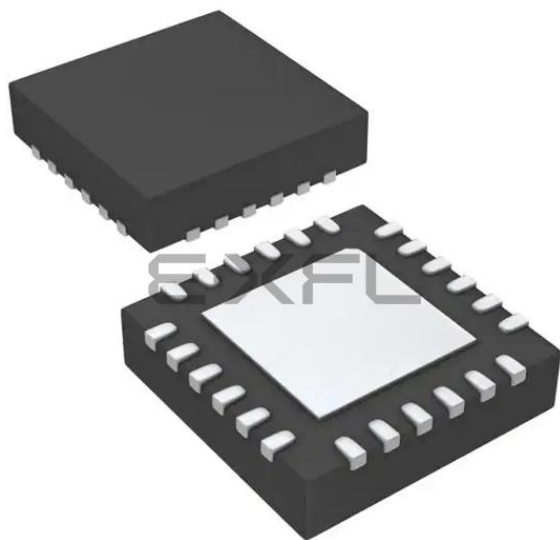




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Details

Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x14b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f64es0-b-qfn24

1. Feature List

The EFM8LB1 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 72 MHz maximum operating frequency
- Memory:
 - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
 - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
 - Internal LDO regulator for CPU core voltage
 - Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
 - Up to 25 pins 5 V tolerant under bias
 - Selectable state retention through reset events
 - Flexible peripheral crossbar for peripheral routing
 - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
 - Internal 72 MHz oscillator with accuracy of $\pm 2\%$
 - Internal 24.5 MHz oscillator with $\pm 2\%$ accuracy
 - Internal 80 kHz low-frequency oscillator
 - External CMOS clock option
 - External crystal/RC oscillator (up to 25 MHz)
- Analog:
 - 14/12/10-Bit Analog-to-Digital Converter (ADC)
 - Internal calibrated temperature sensor ($\pm 3^\circ\text{C}$)
 - 4 x 12-Bit Digital-to-Analog Converters (DAC)
 - 2 x Low-current analog comparators with adjustable reference
- Communications and Digital Peripherals:
 - 2 x UART, up to 3 Mbaud
 - SPI™ Master / Slave, up to 12 Mbps
 - SMBus™/I2C™ Master / Slave, up to 400 kbps
 - I2C High-Speed Slave, up to 3.4 Mbps
 - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
 - 4 Configurable Logic Units
- Timers/Counters and PWM:
 - 6-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes
 - 6 x 16-bit general-purpose timers
 - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
 - Full memory and register inspection
 - Four hardware breakpoints, single-stepping
- Pre-programmed UART or SMBus bootloader

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8LB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified (pending) and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

2. Ordering Information

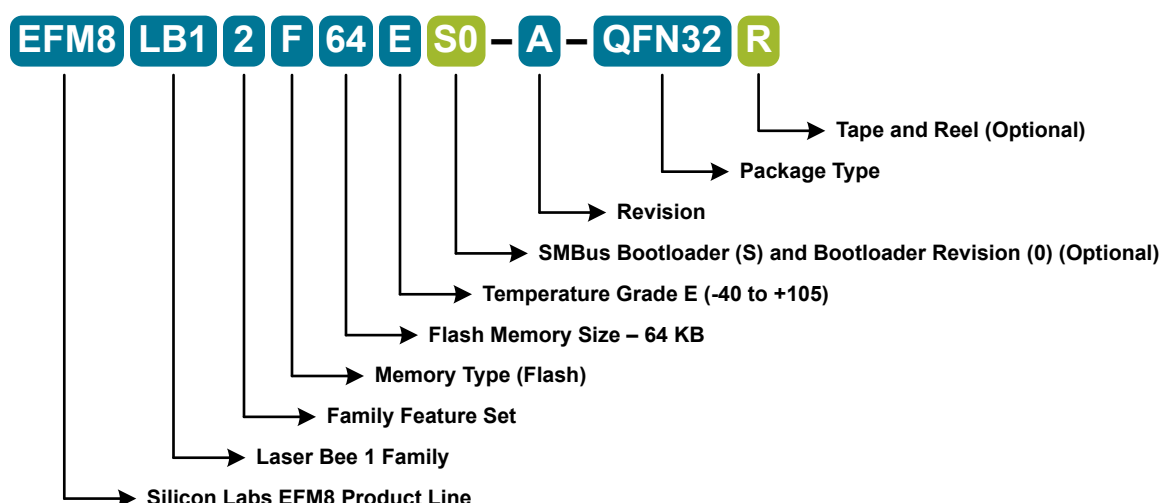


Figure 2.1. EFM8LB1 Part Numbering

All EFM8LB1 family members have the following features:

- CIP-51 Core running up to 72 MHz
- Three Internal Oscillators (72 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- Six 16-bit Timers
- Four Configurable Logic Units
- 14-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, temperature sensor, channel sequencer, and direct-to-VRAM data transfer
- Two Analog Comparators
- 16-bit CRC Unit
- AEC-Q100 qualified (pending)

In addition to these features, each part number in the EFM8LB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Voltage DACs	Comparator 0 Inputs	Comparator 1 Inputs	Bootloader Type	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8LB12F64E-B-QFN32	64	4352	29	20	4	10	9	UART	Yes	-40 to +105 °C	QFN32
EFM8LB12F64E-B-QFP32	64	4352	28	20	4	10	9	UART	Yes	-40 to +105 °C	QFP32
EFM8LB12F64E-B-QFN24	64	4352	20	12	4	6	6	UART	Yes	-40 to +105 °C	QFN24

3. System Overview

3.1 Introduction

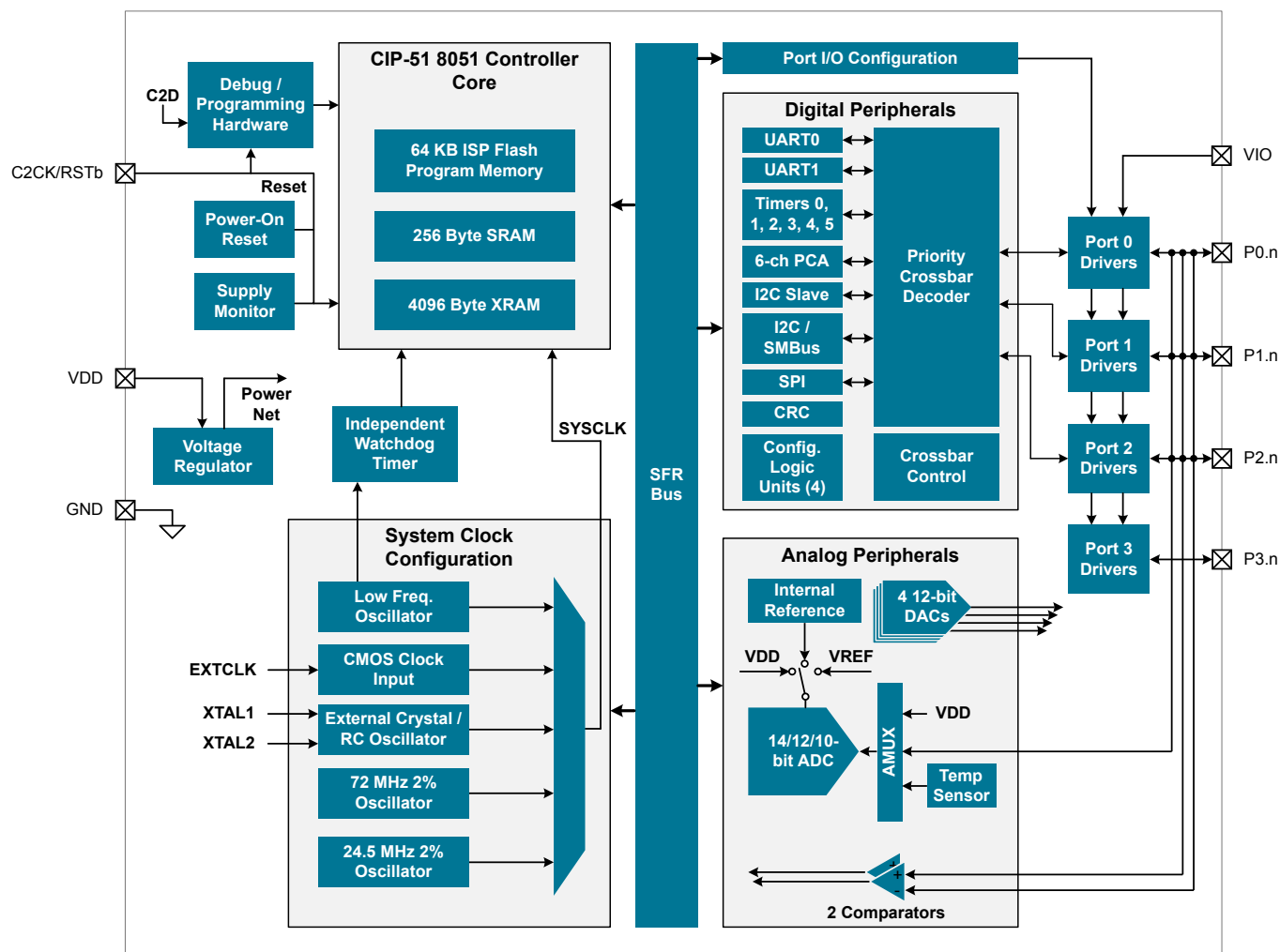


Figure 3.1. Detailed EFM8LB1 Block Diagram

Bootloader	Pins for Bootload Communication
Note: 1. The STK uses these pins for another purpose, so there is a special SMBus bootloader build for the STK only included in <i>AN945: EFM8 Factory Bootloader User Guide</i> that uses P1.2 (SDA) and P1.3 (SCL).	

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QFN32	P3.7 / C2D
QFP32	P3.7 / C2D
QFN24	P3.0 / C2D
QSOP24	P3.0 / C2D

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

4.1.8 Crystal Oscillator

Table 4.8. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		0.02	—	25	MHz
Crystal Drive Current	I_{XTAL}	XFCN = 0	—	0.5	—	μA
		XFCN = 1	—	1.5	—	μA
		XFCN = 2	—	4.8	—	μA
		XFCN = 3	—	14	—	μA
		XFCN = 4	—	40	—	μA
		XFCN = 5	—	120	—	μA
		XFCN = 6	—	550	—	μA
		XFCN = 7	—	2.6	—	mA

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	μs
Power Supply Rejection	$PSRR_{\text{REFFS}}$		—	400	—	ppm/V
On-chip Precision Reference						
Valid Supply Range	V_{DD}	1.2 V Output	2.2	—	3.6	V
		2.4 V Output	2.7	—	3.6	V
Output Voltage	V_{REFP}	1.2 V Output, $V_{\text{DD}} = 3.3 \text{ V}$, $T = 25 \text{ °C}$	1.195	1.2	1.205	V
		1.2 V Output	1.18	1.2	1.22	V
		2.4 V Output, $V_{\text{DD}} = 3.3 \text{ V}$, $T = 25 \text{ °C}$	2.39	2.4	2.41	V
		2.4 V Output	2.36	2.4	2.44	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin	—	3	—	ms
		0.1 μF ceramic bypass on VREF pin	—	100	—	μs
Load Regulation	LR_{VREFP}	$V_{\text{REF}} = 2.4 \text{ V}$, Load = 0 to 200 μA to GND	—	8	—	μV/μA
		$V_{\text{REF}} = 1.2 \text{ V}$, Load = 0 to 200 μA to GND	—	5	—	μV/μA
Load Capacitor	C_{VREFP}	Load = 0 to 200 μA to GND	0.1	—	—	μF
Short-circuit current	ISC_{VREFP}		—	—	8	mA
Power Supply Rejection	$PSRR_{\text{VREFP}}$		—	75	—	dB
External Reference						
Input Current	I_{EXTREF}	ADC Sample Rate = 1 Msps; $V_{\text{REF}} = 3.0 \text{ V}$	—	5	—	μA

4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Uncalibrated Offset	V_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	751	—	mV
Uncalibrated Offset Error ¹	E_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	19	—	mV
Slope	M		—	2.82	—	mV/ $^{\circ}\text{C}$
Slope Error ¹	E_M		—	29	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity	LIN	$T = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$	—	-0.1 to 0.15	—	$^{\circ}\text{C}$
		$T = -20\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	—	-0.2 to 0.35	—	$^{\circ}\text{C}$
		$T = -40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$	—	-0.4 to 0.8	—	$^{\circ}\text{C}$
Turn-on Time	t_{ON}		—	3.5	—	μs
Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset ^{2, 3}	E_{TOT}	$T = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$	-2.6	—	1.8	$^{\circ}\text{C}$
		$T = -20\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	-2.9	—	2.7	$^{\circ}\text{C}$
		$T = -40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$	-3.2	—	4.2	$^{\circ}\text{C}$

Note:

1. Represents one standard deviation from the mean.
2. The factory-calibrated offset value is stored in the read-only area of flash in locations 0xFFD4 (low byte) and 0xFFD5 (high byte). The 14-bit result represents the output of the ADC when sampling the temp sensor using the 1.65 V internal voltage reference.
3. The temp sensor error includes the offset calibration error, slope error, and linearity error. The values are based upon characterization and are not tested across temperature in production. The values represent three standard deviations above and below the mean. Additional information on achieving high measurement accuracy is available in AN929: Accurate Temperature Sensing with the EFM8 Laser Bee MCU Family.

4.1.12 DACs

Table 4.12. DACs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}		12			Bits
Throughput Rate	f_S		—	—	200	ksps
Integral Nonlinearity	INL	DAC0 and DAC2	-10	-1.77 / 1.56	10	LSB
		DAC1 and DAC3	-11.5	-2.73 / 1.11	11.5	LSB
Differential Nonlinearity	DNL		-1	—	1	LSB
Output Noise	$V_{\text{REF}} = 2.4 \text{ V}$ $f_S = 0.1 \text{ Hz to } 300 \text{ kHz}$		—	110	—	μV_{RMS}
Slew Rate	SLEW		—	± 1	—	V/ μs
Output Settling Time to 1% Full-scale	t_{SETTLE}	V_{OUT} change between 25% and 75% Full Scale	—	2.6	5	μs
Power-on Time	t_{PWR}		—	—	10	μs
Voltage Reference Range	V_{REF}		1.15	—	V_{DD}	V
Power Supply Rejection Ratio	PSRR	DC, $V_{\text{OUT}} = 50\%$ Full Scale	—	78	—	dB
Total Harmonic Distortion	THD	$V_{\text{OUT}} = 10 \text{ kHz}$ sine wave, 10% to 90%	54	—	—	dB
Offset Error	E_{OFF}	$V_{\text{REF}} = 2.4 \text{ V}$	-8	0	8	LSB
Full-Scale Error	E_{FS}	$V_{\text{REF}} = 2.4 \text{ V}$	-13	± 5	13	LSB
External Load Impedance	R_{LOAD}		2	—	—	k Ω
External Load Capacitance ¹	C_{LOAD}		—	—	100	pF
Load Regulation		$V_{\text{OUT}} = 50\%$ Full Scale $I_{\text{OUT}} = -2 \text{ to } 2 \text{ mA}$	—	100	1300	$\mu\text{V}/\text{mA}$

Note:

1. No minimum external load capacitance is required. However, under low loading conditions, it is possible for the DAC output to glitch during start-up. If smooth start-up is required, the minimum loading capacitance at the pin should be a minimum of 10 pF.

Table 4.17. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	$f_{\text{CSO}} / 3$
Bus Free Time Between STOP and START Conditions	t_{BUF}	$2 / f_{\text{CSO}}$
Hold Time After (Repeated) START Condition	$t_{\text{HD:STA}}$	$1 / f_{\text{CSO}}$
Repeated START Condition Setup Time	$t_{\text{SU:STA}}$	$2 / f_{\text{CSO}}$
STOP Condition Setup Time	$t_{\text{SU:STO}}$	$2 / f_{\text{CSO}}$
Clock Low Period	t_{LOW}	$1 / f_{\text{CSO}}$
Clock High Period	t_{HIGH}	$2 / f_{\text{CSO}}$

Note:
1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

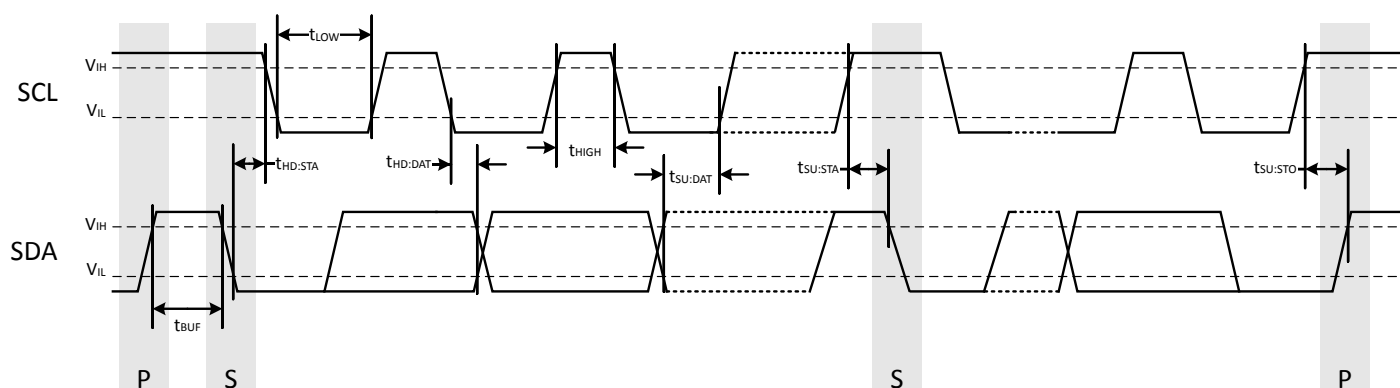


Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFN24 Packages	—	30	—	°C/W
		QFN32 Packages	—	26	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QSOP24 Packages	—	65	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.19 Absolute Maximum Ratings on page 30](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		-55	125	°C
Storage Temperature	T_{STG}		-65	150	°C
Voltage on VDD	V_{DD}		GND-0.3	4.2	V
Voltage on VIO ²	V_{IO}		GND-0.3	$V_{DD}+0.3$	V
Voltage on I/O pins or RSTb, excluding P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	V_{IN}	$V_{IO} > 3.3\text{ V}$	GND-0.3	5.8	V
		$V_{IO} < 3.3\text{ V}$	GND-0.3	$V_{IO}+2.5$	V
Voltage on P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	V_{IN}		GND-0.3	$V_{DD}+0.3$	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I_{IO}		-100	100	mA
Operating Junction Temperature	T_J	$T_A = -40\text{ °C to }105\text{ °C}$	-40	130	°C

Note:

1. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 31 shows a typical connection diagram for the power pins of the device.

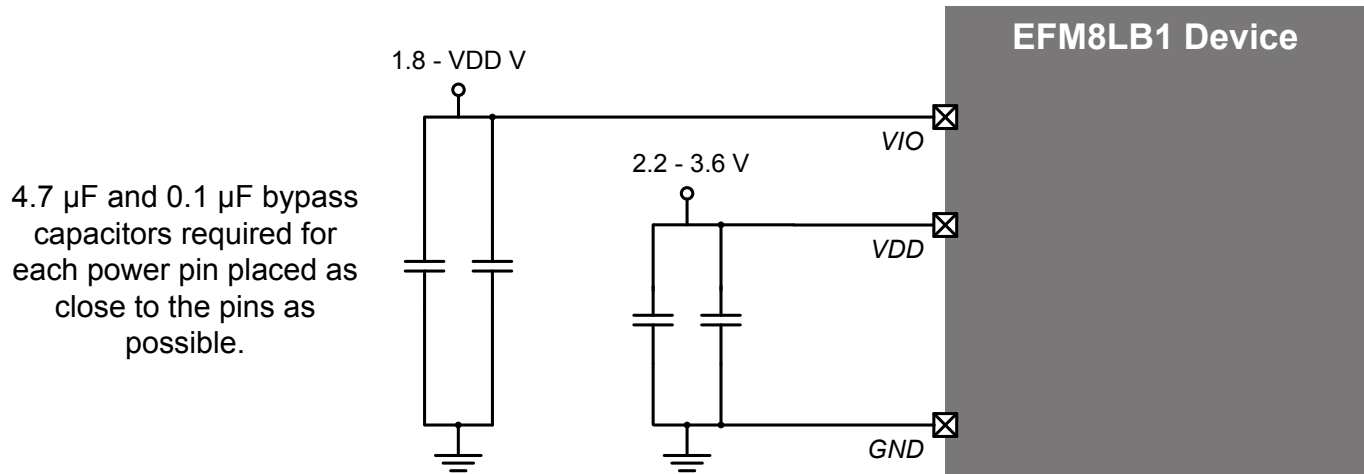


Figure 5.1. Power Connection Diagram

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (<http://www.silabs.com/8bit-appnotes>) or in Simplicity Studio.

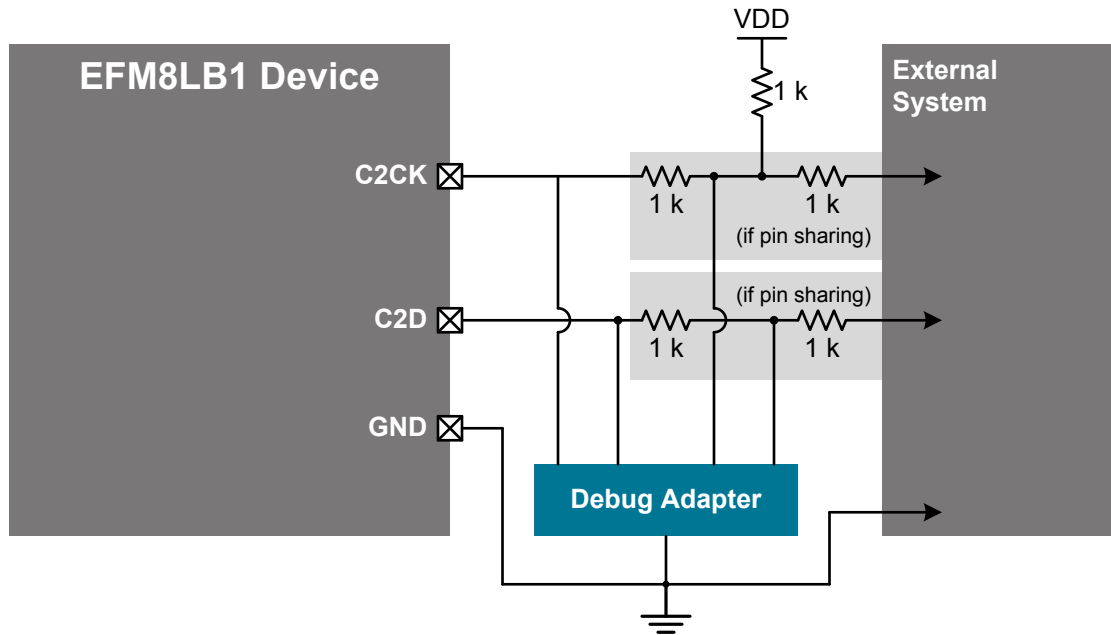


Figure 5.2. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.13	ADC0.7 CMP0P.7 CMP0N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.9 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
8	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2
9	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
10	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
11	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
5	GND	Ground			
6	VDD / VIO	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
10	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions

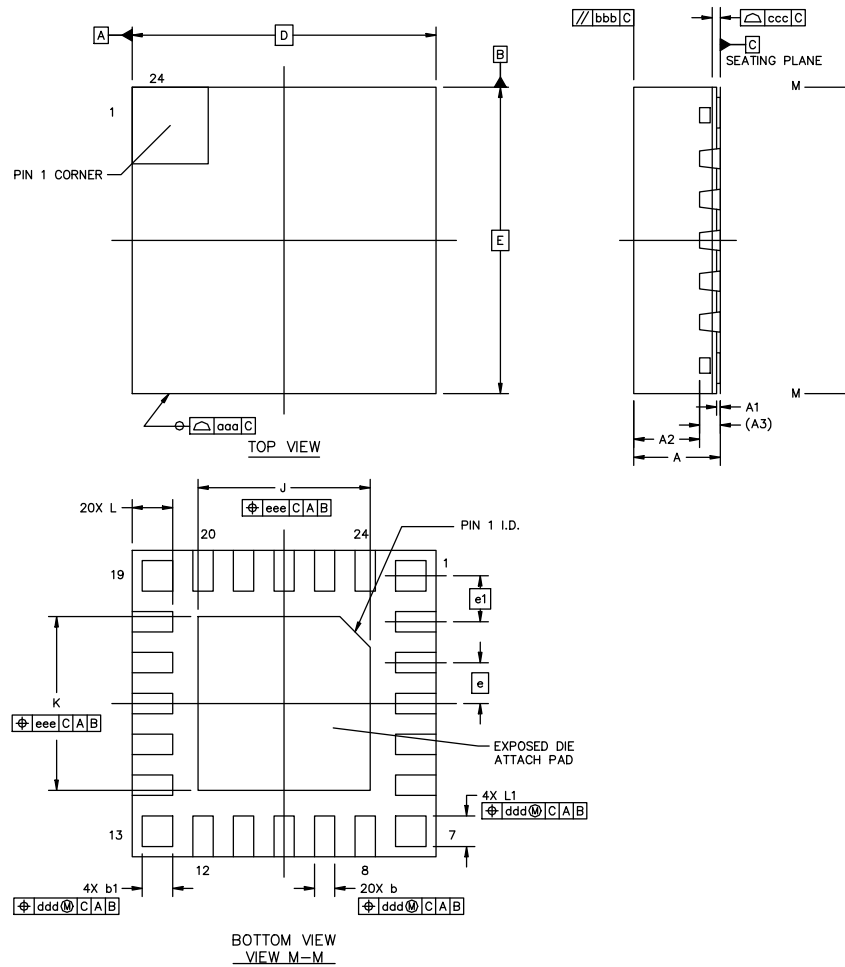


Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3	0.203 REF		
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D	3.00 BSC		
E	3.00 BSC		

11. Revision History

11.1 Revision 1.01

October 21st, 2016

Updated QFN24 center pad stencil description.

11.2 Revision 1.0

September 6th, 2016

Updated part numbers to revision B.

Updated many specifications with full characterization data.

Added a note regarding which DACs are available to [Table 2.1 Product Selection Guide on page 2](#).

Added specifications for [4.1.16 SMBus](#).

Added bootloader pinout information to [3.10 Bootloader](#).

Added CRC Calculation Time to [4.1.4 Flash Memory](#).

11.3 Revision 0.5

February 10th, 2016

Updated [Figure 5.2 Debug Connection Diagram on page 32](#) to move the pull-up resistor on C2D / RSTb to after the series resistor instead of before.

Added S0 devices and information about the SMBus bootloader in [3.10 Bootloader](#).

Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in [3.10 Bootloader](#).

Added mention of the pre-programmed bootloaders in [1. Feature List](#).

Updated all part numbers to revision B.

Added the C oscillator, which is now available on revision B.

Adjusted C1, C2, X2, Y2, and Y1 maximums for [7.2 QFN32 PCB Land Pattern](#).

Adjusted package markings for QFN32 and QSOP24 packages.

Filled in TBD minimum and maximum values for DAC Differential Nonlinearity in [Table 4.12 DACs on page 24](#).

11.4 Revision 0.4

Updated specification tables based on current device characterization status and production test limits.

Added bootloader section.

Added typical connection diagrams.

Corrected CLU connections in pin function tables.

11.5 Revision 0.3

Added information on the bootloader to [3.10 Bootloader](#).

Updated some characterization TBD values.

11.6 Revision 0.1

Initial release.

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