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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	122
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bfd18spmc-gk7e1

1. Product Lineup

Memory Size

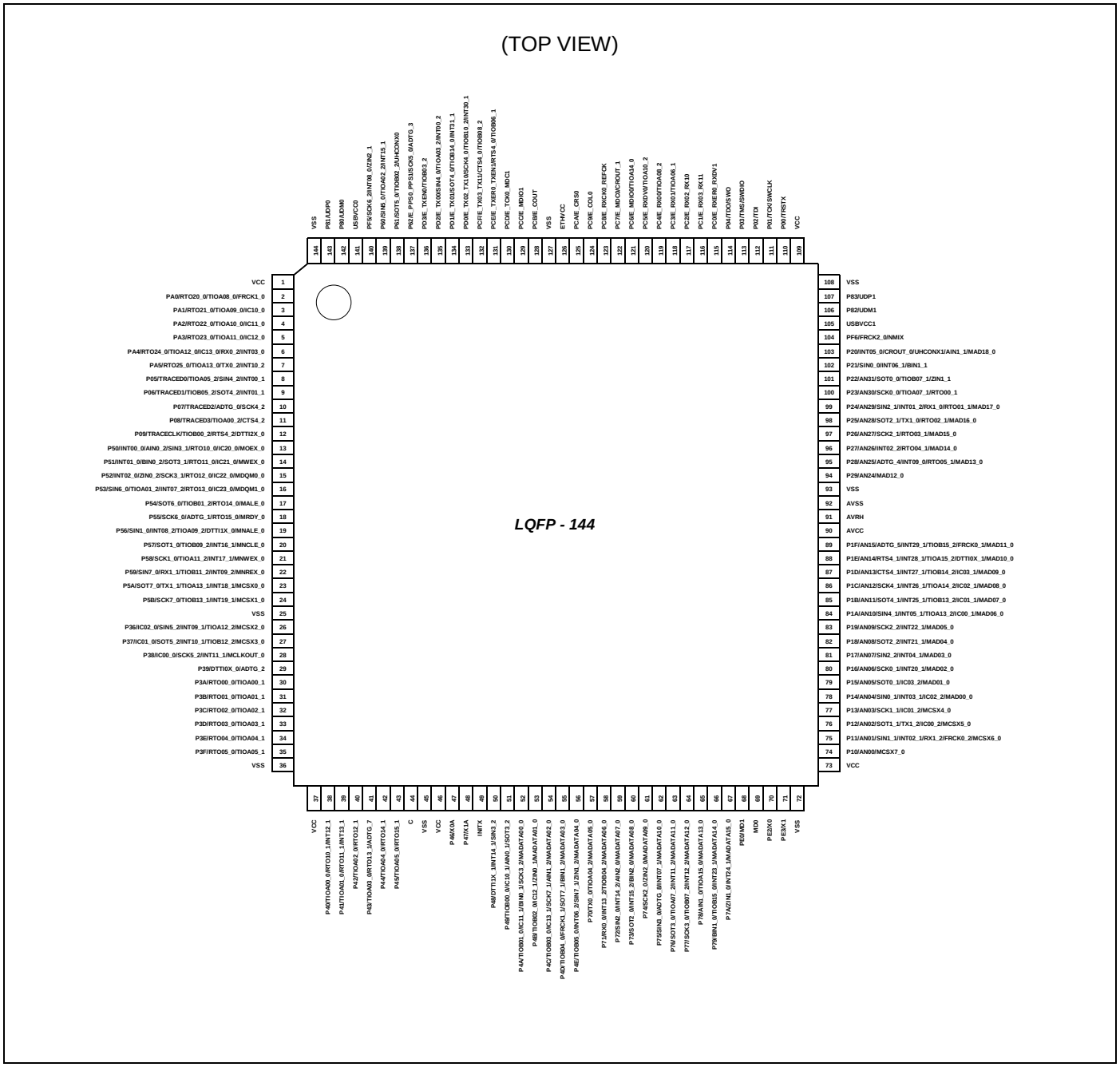
Product name	MB9BFD16S MB9BFD16T	MB9BFD17S MB9BFD17T	MB9BFD18S MB9BFD18T
On-chip Flash memory	512 KB	768 KB	1 MB
On-chip RAM	64 KB	96 KB	128 KB

Function

Product name			MB9BFD16S MB9BFD17S MB9BFD18S	MB9BFD16T MB9BFD17T MB9BFD18T
Pin count			144	176/192
CPU			Cortex-M3	
	Freq.		144 MHz	
Power supply voltage range			VCC: 2.7 V to 5.5 V (USBVCC0: 3.0 V to 3.6 V) (USBVCC1: 3.0 V to 3.6 V) (ETHVCC: 3.0 V to 5.5 V)	
USB2.0 (Function/Host)			2ch. (Max)	
CAN			2ch. (Max)	
Ethernet-MAC			2ch. (Max) MII: 1ch. / RMII: 2ch.(Max)	
DMAC			8ch.	
External Bus Interface			Addr: 19-bit (Max) R/Wdata: 8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR & NAND Flash	Addr: 25-bit (Max) R/Wdata :8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR & NAND Flash
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			8ch. (Max) ch.4 to ch.7: FIFO (16 steps × 9-bit) ch.0 to ch.3: No FIFO	
Base Timer (PWC/ Reload timer/PWM/PPG)			16ch. (Max)	
MF-Timer	A/D activation compare	3ch.	3 units (Max)	
	Input capture	4ch.		
	Free-run timer	3ch.		
	Output compare	6ch.		
	Waveform generator	3ch.		
	PPG	3ch.		
QPRC			3ch. (Max)	
Dual Timer			1 unit	
Watch Counter			1 unit	
CRC Accelerator			Yes	
Watchdog timer			1ch. (SW) + 1ch. (HW)	
External Interrupts			32 pins (Max)+ NMI × 1	
I/O ports			122 pins (Max)	154 pins (Max)
12-bit A/D converter			24ch. (3 units)	32ch. (3 units)
CSV (Clock Super Visor)			Yes	
LVD (Low-Voltage Detector)			2ch.	
Built-in CR	High-speed		4 MHz	
	Low-speed		100 kHz	
Debug Function			SWJ-DP/ETM	

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use.
See “12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Internal CR Oscillation Characteristics” for accuracy of built-in CR.

FPT-144P-M08



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

TIOA09_0 and TIOA09_2 cannot be used as the external startup trigger input (TGIN signal) at I/O mode 1 (timer full mode) of the Base Timer. See "Base Timer" in "7. Handling Devices" for details.

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
35	27	J2	P37 IC01_0 SOT5_2 INT10_1 TIOB12_2 MCSX3_0	E	H
36	28	K1	P38 IC00_0 SCK5_2 INT11_1 MCLKOUT_0	E	H
37	29	K2	P39 DTTI0X_0 ADTG_2	E	I
38	30	K3	P3A RTO00_0 TIOA00_1	G	I
39	31	K4	P3B RTO01_0 TIOA01_1	G	I
40	32	L1	P3C RTO02_0 TIOA02_1	G	I
41	33	L2	P3D RTO03_0 TIOA03_1	G	I
42	34	L3	P3E RTO04_0 TIOA04_1	G	I
43	35	M2	P3F RTO05_0 TIOA05_1	G	I
44	36	M1	VSS	-	
45	37	N1	VCC	-	
46	38	N2	P40 TIOA00_0 RTO10_1 INT12_1	G	H
47	39	N3	P41 TIOA01_0 RTO11_1 INT13_1	G	H

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
94	78	L11	P14 AN04 SIN0_1 INT03_1 IC02_2 MAD00_0	F	L
95	79	K13	P15 AN05 SOT0_1 IC03_2 MAD01_0	F	K
96	80	K12	P16 AN06 SCK0_1 INT20_1 MAD02_0	F	L
97	81	K14	P17 AN07 SIN2_2 INT04_1 MAD03_0	F	L
-	-	P7	VSS	-	
-	-	P11	VSS	-	
-	-	L14	VSS	-	
98	82	K11	P18 AN08 SOT2_2 INT21_1 MAD04_0	F	L
99	83	J13	P19 AN09 SCK2_2 INT22_1 MAD05_0	F	L
100	84	J12	P1A AN10 SIN4_1 INT05_1 TIOA13_2 IC00_1 MAD06_0	F	L

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
101	85	J11	P1B AN11 SOT4_1 INT25_1 TIOB13_2 IC01_1 MAD07_0	F	L
102	86	J10	P1C AN12 SCK4_1 INT26_1 TIOA14_2 IC02_1 MAD08_0	F	L
103	87	J9	P1D AN13 CTS4_1 INT27_1 TIOB14_2 IC03_1 MAD09_0	F	L
104	88	H10	P1E AN14 RTS4_1 INT28_1 TIOA15_2 DTTI0X_1 MAD10_0	F	L
105	89	H9	P1F AN15 ADTG_5 INT29_1 TIOB15_2 FRCK0_1 MAD11_0	F	L
106	90	J14	AVCC	-	
107	91	H14	AVRH	-	
108	92	G14	AVSS	-	
109	93	F14	VSS	-	
110	-	H13	PB0 AN16 TIOA09_1 SIN7_2 INT16_0	F	L

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
111	-	H12	PB1 AN17 TIOB09_1 SOT7_2 INT17_0	F	L
112	-	H11	PB2 AN18 TIOA10_1 SCK7_2 INT18_0	F	L
113	-	G13	PB3 AN19 TIOB10_1 INT19_0	F	L
114	-	G12	PB4 AN20 TIOA11_1 SIN0_2 INT20_0	F	L
115	-	G11	PB5 AN21 TIOB11_1 SOT0_2 INT21_0 AIN2_2	F	L
-	-	G7	VSS	-	
-	-	J7	VSS	-	
116	-	G10	PB6 AN22 TIOA12_1 SCK0_2 INT22_0 BIN2_2	F	L
117	-	G9	PB7 AN23 TIOB12_1 INT23_0 ZIN2_2	F	L
118	94	F10	P29 AN24 MAD12_0	F	K

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
165	135	C6	PD2 E_TX00 SIN4_0 TIOA03_2 INT00_2	L	R
166	136	D6	PD3 E_TXEN0 TIOB03_2	L	Q
167	137	E6	P62 E_PPS0_PPS1 SCK5_0 ADTG_3	E	Q
168	138	B5	P61 SOT5_0 TIOB02_2 UHCONX0	E	I
169	139	C5	P60 SIN5_0 TIOA02_2 INT15_1	E	H
170	-	B4	PF3 TIOA06_0 SIN6_2 INT06_0 AIN2_1	I[1]	H
171	-	C4	PF4 TIOB06_0 SOT6_2 INT07_0 BIN2_1	I[1]	H
172	140	B3	PF5 SCK6_2 INT08_0 ZIN2_1	I[1]	H
173	141	A4	USBVCC0	-	
174	142	A3	P80 UDM0	H	O
175	143	A2	P81 UDP0	H	O
176	144	B1	VSS	-	
-	-	M7	VSS	-	

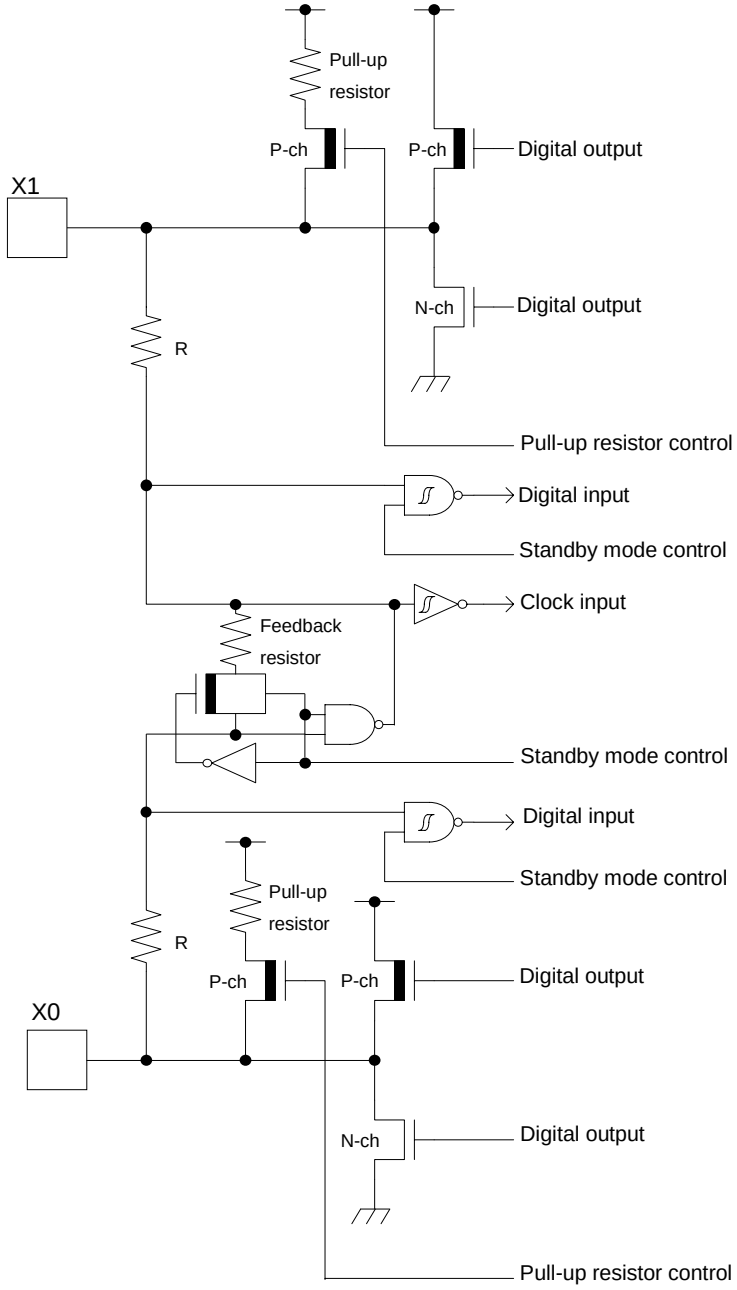
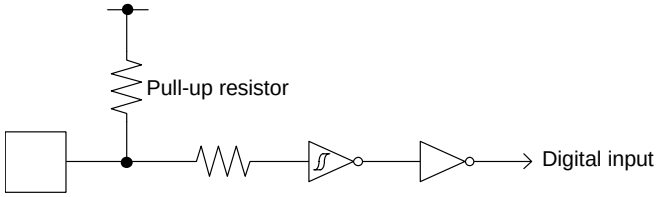
[1]: 5 V tolerant I/O

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
GPIO	P00	General-purpose I/O port 0	134	110	B13
	P01		135	111	A12
	P02		136	112	C12
	P03		137	113	B12
	P04		138	114	B11
	P05		8	8	D3
	P06		9	9	D4
	P07		10	10	E2
	P08		11	11	E3
	P09		12	12	E4
	P10	General-purpose I/O port 1	90	74	M13
	P11		91	75	M12
	P12		92	76	L13
	P13		93	77	L12
	P14		94	78	L11
	P15		95	79	K13
	P16		96	80	K12
	P17		97	81	K14
	P18		98	82	K11
	P19		99	83	J13
	P1A		100	84	J12
	P1B		101	85	J11
	P1C		102	86	J10
	P1D		103	87	J9
	P1E		104	88	H10
	P1F		105	89	H9
	P20	General-purpose I/O port 2	127	103	D13
	P21		126	102	D12
	P22		125	101	E13
	P23		124	100	E12
	P24		123	99	E11
	P25		122	98	E10
	P26		121	97	F13
	P27		120	96	F12
	P28		119	95	F11
	P29		118	94	F10

Module	Pin name	Function	Pin No.		
			LQFP-176	LQFP-144	BGA-192
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	126	102	D12
	SIN0_1		94	78	L11
	SIN0_2		114	-	G12
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	125	101	E13
	SOT0_1 (SDA0_1)		95	79	K13
	SOT0_2 (SDA0_2)		115	-	G11
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I^2C (operation mode 4).	124	100	E12
	SCK0_1 (SCL0_1)		96	80	K12
	SCK0_2 (SCL0_2)		116	-	G10
Multi-function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	19	19	F6
	SIN1_1		91	75	M12
	SIN1_2		81	-	M10
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	20	20	G2
	SOT1_1 (SDA1_1)		92	76	L13
	SOT1_2 (SDA1_2)		82	-	N11
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I^2C (operation mode 4).	21	21	G3
	SCK1_1 (SCL1_1)		93	77	L12
	SCK1_2 (SCL1_2)		83	-	M11

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	165	135	C6
	SIN4_1		100	84	J12
	SIN4_2		8	8	D3
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	164	134	B6
	SOT4_1 (SDA4_1)		101	85	J11
	SOT4_2 (SDA4_2)		9	9	D4
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I^2C (operation mode 4).	163	133	F7
	SCK4_1 (SCL4_1)		102	86	J10
	SCK4_2 (SCL4_2)		10	10	E2
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	161	131	D7
	RTS4_1		104	88	H10
	RTS4_2		12	12	E4
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	162	132	E7
	CTS4_1		103	87	J9
	CTS4_2		11	11	E3
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	169	139	C5
	SIN5_1		141	-	B10
	SIN5_2		34	26	J3
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	168	138	B5
	SOT5_1 (SDA5_1)		142	-	C10
	SOT5_2 (SDA5_2)		35	27	J2
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I^2C (operation mode 4).	167	137	E6
	SCK5_1 (SCL5_1)		143	-	D10
	SCK5_2 (SCL5_2)		36	28	K1

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. ■Oscillation feedback resistor : Approximately 1MΩ ■With Standby mode control When the GPIO is selected. ■CMOS level output. ■CMOS level hysteresis input ■With pull-up resistor control ■With standby mode control ■Pull-up resistor : Approximately 50 kΩ ■I_{OH} = -4 mA, I_{OL} = 4 mA
B		■CMOS level hysteresis input ■Pull-up resistor : Approximately 50 kΩ

(Vcc = AVcc = USBVcc0 = USBVcc1 = ETHVcc = 2.7 V to 5.5 V, Vss = AVss = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*2	Max*2		
TIMER mode current	I_{CCT}	VCC	Main TIMER mode	Ta = + 25°C, When LVD is off	4	10	mA	[1], [3]
				Ta = + 85°C, When LVD is off	-	55	mA	[1], [3]
			Sub TIMER mode	Ta = + 25°C, When LVD is off	1.1	5	mA	[1], [4]
				Ta = + 85°C, When LVD is off	-	50	mA	[1], [4]
STOP mode current	I_{CCH}		STOP mode	Ta = + 25°C, When LVD is off	1	5	mA	[1]
				Ta = + 85°C, When LVD is off	-	50	mA	[1]

[1]: When all ports are fixed.

[2]: V_{CC} = 5.5 V

[3]: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

[4]: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

Low-Voltage Detection Current

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for interrupt	4	7	µA	At not detect

Flash Memory Current

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	12	14	mA	

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = AVRL = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1 unit operation	0.57	0.72	mA	
			At stop	0.06	35	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5 V	1.1	1.96	mA	
			At stop	0.06	4	µA	

CSIO (SPI = 1, SCINV = 1)

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see “8. Block Diagram” in this datasheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance = 30 pF.

12.4.13 I^2C Timing

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})[1]	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCLclock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCLclock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45[2]	0	0.9[3]	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	8 MHz ≤ t_{CYCP} ≤ 40 MHz	2 t_{CYCP}[4]	-	2 t_{CYCP}[4]	-	ns	[5]
		40 MHz < t_{CYCP} ≤ 60 MHz	3 t_{CYCP}[4]	-	3 t_{CYCP}[4]	-	ns	[5]
		60 MHz < t_{CYCP} ≤ 72 MHz	4 t_{CYCP}[4]	-	4 t_{CYCP}[4]	-	ns	[5]

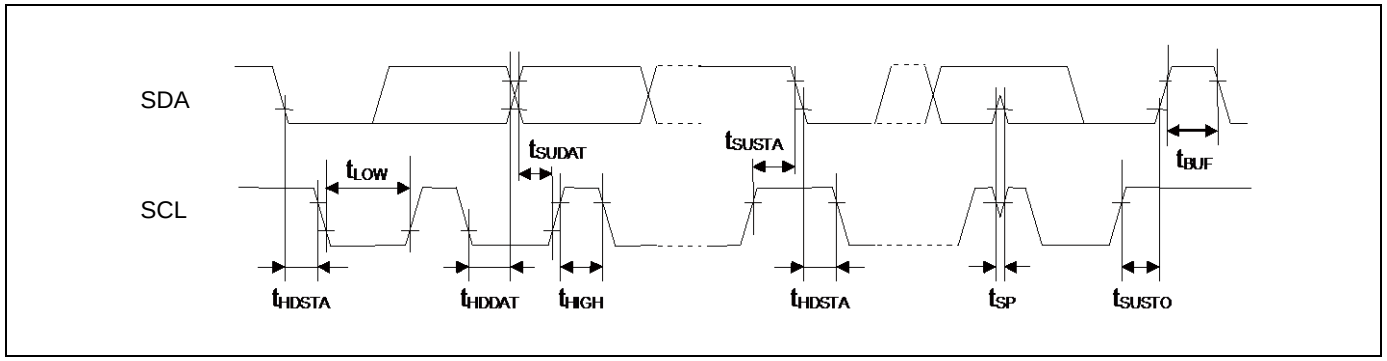
[1]: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.
Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

[2]: The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

[3]: A Fast-mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns"

[4]: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number which I^2C is connected to, see "8. Block Diagram" in this datasheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.

[5]: The number of steps of the noise filter can be changed with register settings.
Change the number of the noise filter steps according to APB2 bus clock frequency.

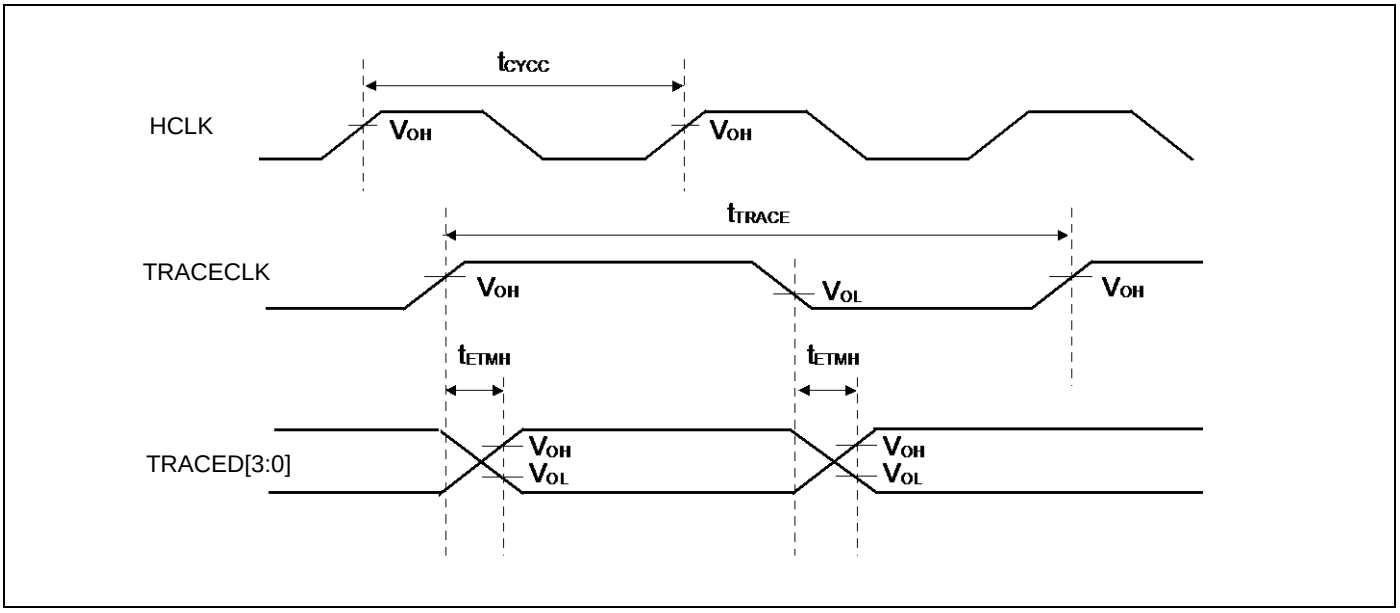


12.4.14 ETM Timing

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[3:0]	Vcc ≥ 4.5 V	2	9	ns	
			Vcc < 4.5 V	2	15		
TRACECLK frequency	1/ t_{TRACE}	TRACECLK	Vcc ≥ 4.5 V	-	50	MHz	
			Vcc < 4.5 V	-	32	MHz	
TRACECLK cycle time	t_{TRACE}		Vcc ≥ 4.5 V	20	-	ns	
			Vcc < 4.5 V	31.25	-	ns	

Note: When the external load capacitance = 30 pF.



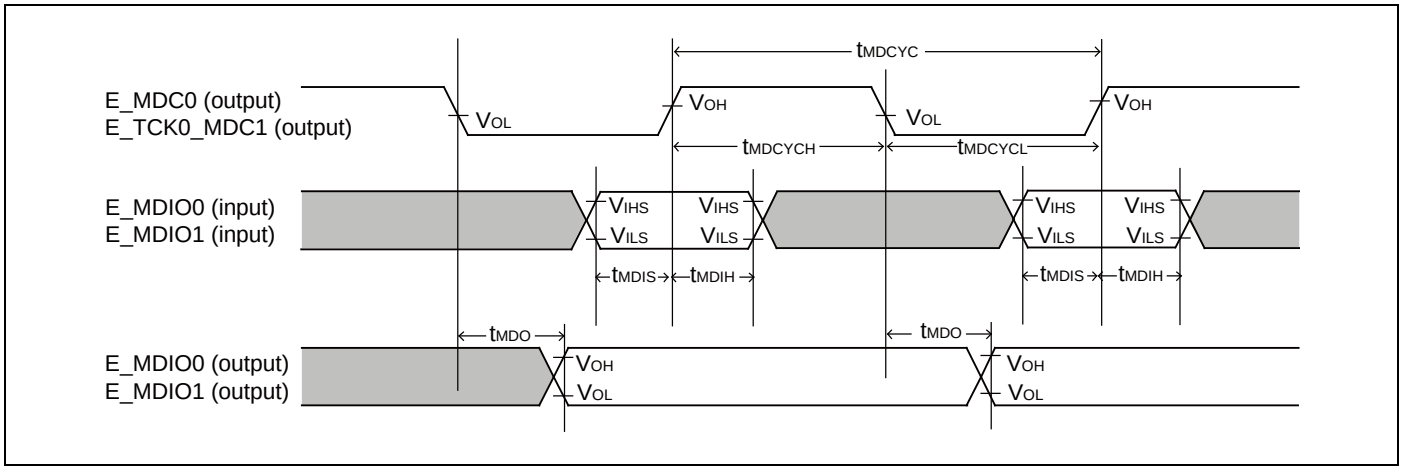
Management interface

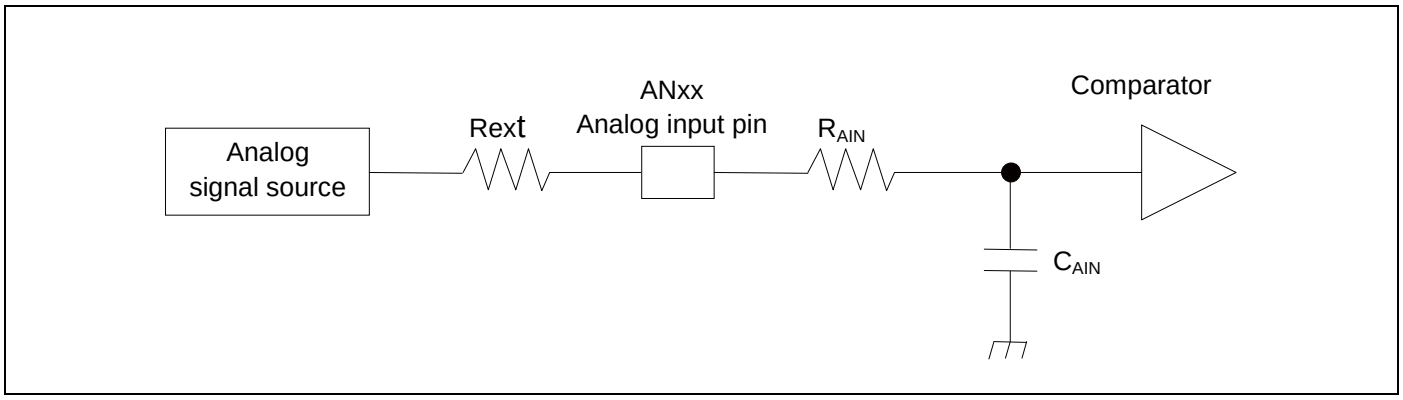
(ETHVcc = 3.0 V to 3.6 V, 4.5 V to 5.5 V)

(Vss = 0 V, Ta = - 40°C to + 85°C, C_L=25 pF)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Management Clock Cycle time[1] (ch.0)	t_{MDCYC}	E_MDC0	-	400	-	ns
Management Clock Cycle time[1] (ch.1)		E_TCK0_MDC1				
Management Clock High pulse width duty (ch.0)	t_{MDCYCH}	E_MDC0	t_{MDCYCH} / t_{MDCYC}	45	55	%
Management Clock High pulse width duty (ch.1)		E_TCK0_MDC1				
Management Clock Low pulse width duty (ch.0)	t_{MDCYCL}	E_MDC0	t_{MDCYCL} / t_{MDCYC}	45	55	%
Management Clock Low pulse width duty (ch.1)		E_TCK0_MDC1				
MDC ↓ → MDIO Delay time (ch.0)	t_{MDO}	E_MDIO0	-	-	60	ns
MDC ↓ → MDIO Delay time (ch.1)		E_MDIO1				
MDIO → MDC ↑ Setup time (ch.0)	t_{MDIS}	E_MDIO0	-	20	-	ns
MDIO → MDC ↑ Setup time (ch.1)		E_MDIO1				
MDC ↑ → MDIO Hold time (ch.0)	t_{MDIH}	E_MDIO0	-	0	-	ns
MDC ↑ → MDIO Hold time (ch.1)		E_MDIO1				

[1]: The clock time should be set to a value greater than the minimum value by setting the Ether-MAC setting register.





(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts : Sampling time

R_{AIN} : input resistance of A/D = 2 kΩ at $4.5 \leq AV_{CC} \leq 5.5$

input resistance of A/D = 3.8 kΩ at $2.7 \leq AV_{CC} < 4.5$

C_{AIN} : input capacity of A/D = 12.9 pF at $2.7 \leq AV_{CC} \leq 5.5$

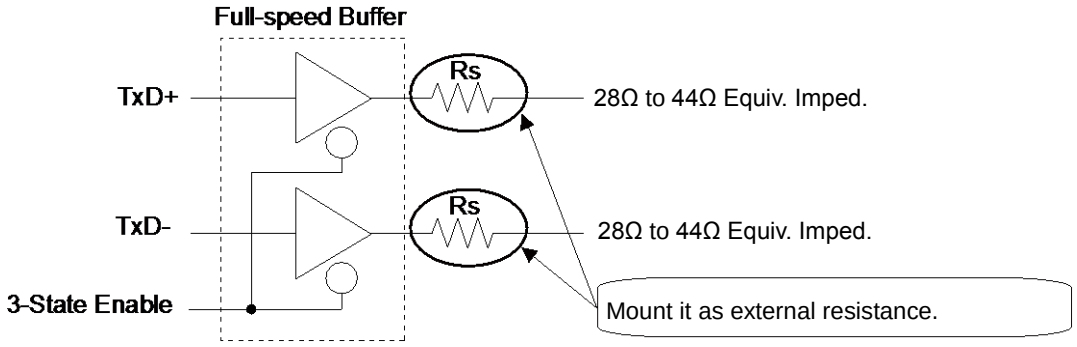
Rext : Output impedance of external circuit

(Equation 2) $Tc = Tcck \times 14$

Tc : Compare time

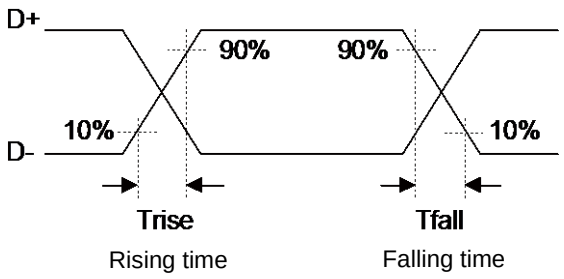
Tcck : Compare clock cycle

[6]: USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15% characteristic impedance (Differential Mode). USB standard defines that output impedance of USB driver must be in range from 28 Ω to 44 Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommendation value 27 Ω) series resistor Rs.



Rs series resistor 25 Ω to 30 Ω
Series resistor of 27 Ω (recommendation value) must be added.
And, use "resistance with an uncertainty of 5% by E24 sequence".

[7]: They indicate rise time (Trise) and fall time (Tfall) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.



See Figure "Low-speed load (compliance load)" for conditions of external load.

12.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

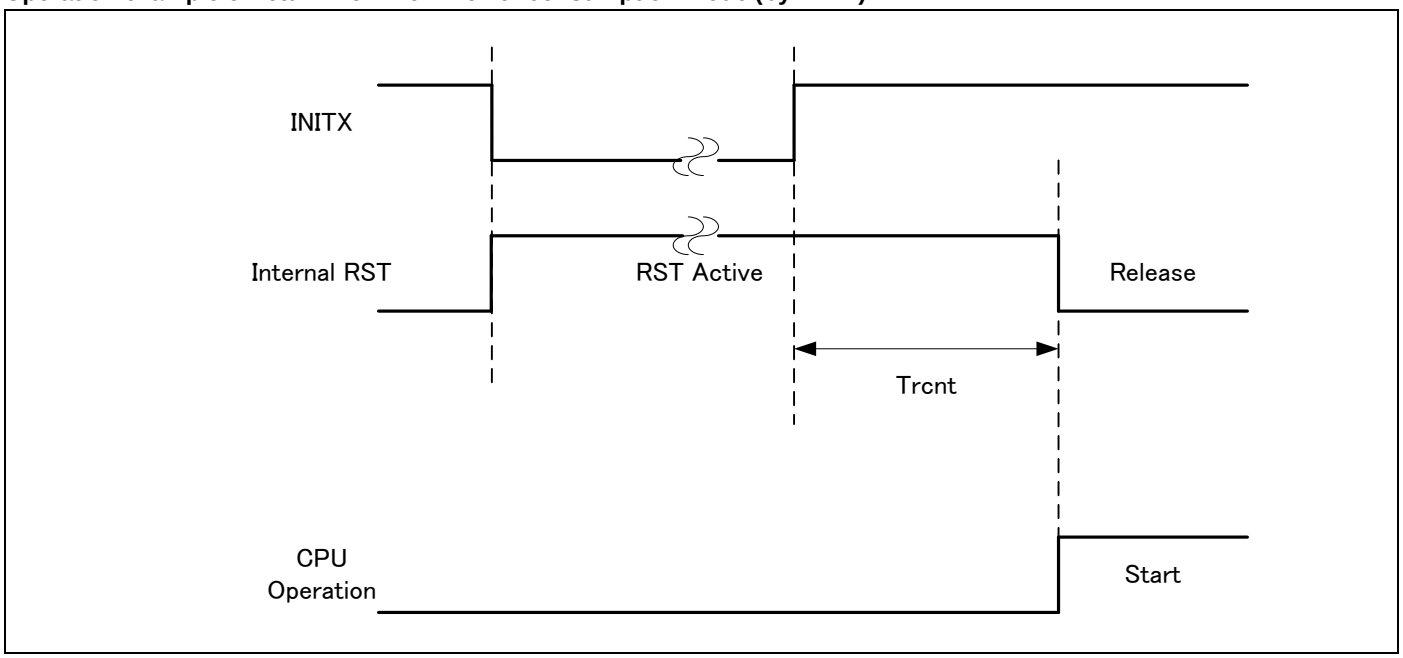
Return count time

(V_{CC} = 2.7 V to 5.5 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max[1]		
SLEEP mode	Trcnt	321	461	µs	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		321	461	µs	
Low-speed CR TIMER mode		441	701	µs	
Sub TIMER mode		441	701	µs	
STOP mode		441	701	µs	

[1]: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



13. Ordering Information

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9BFD16SPMC-GE1	512 KB	64 KB	Plastic · LQFP 144-pin (0.5 mm pitch), (FPT-144P-M08)	Tray
MB9BFD17SPMC-GE1	768 KB	96 KB		
MB9BFD18SPMC-GE1	1 MB	128 KB		
MB9BFD16TPMC-GE1	512 KB	64 KB	Plastic · LQFP 176-pin (0.5 mm pitch), (FPT-176P-M07)	
MB9BFD17TPMC-GE1	768 KB	96 KB		
MB9BFD18TPMC-GE1	1 MB	128 KB		
MB9BFD16TBGL-GE1	512 KB	64 KB	Plastic · PFBGA 192-pin (0.8 mm pitch), (BGA-192P-M06)	
MB9BFD17TBGL-GE1	768 KB	96 KB		
MB9BFD18TBGL-GE1	1 MB	128 KB		