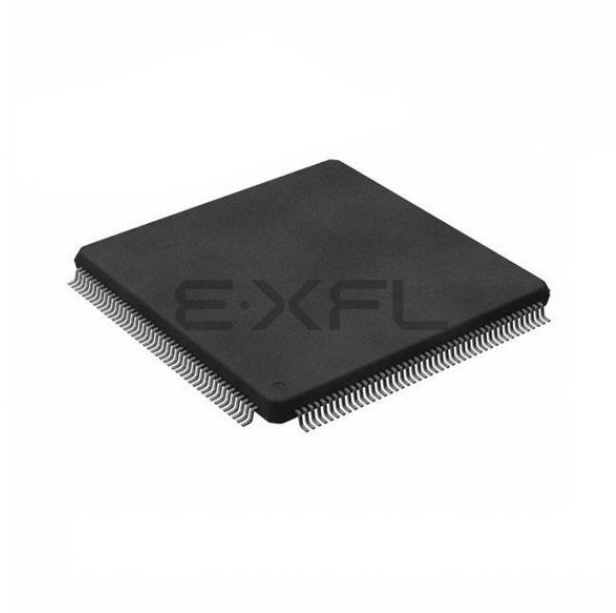
Infineon Technologies - MB9BFD18TPMC-GK7E1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, CSIO, EBI/EMI, Ethernet, I²C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	154
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bfd18tpmc-gk7e1

Contents

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
External Interrupt	INT00_0	External interrupt request 00 input pin	13	13	E5
	INT00_1		8	8	D3
	INT00_2		165	135	C6
	INT01_0	External interrupt request 01 input pin	14	14	F1
	INT01_1		9	9	D4
	INT01_2		123	99	E11
	INT02_0	External interrupt request 02 input pin	15	15	F2
	INT02_1		91	75	M12
	INT02_2		120	96	F12
	INT03_0	External interrupt request 03 input pin	6	6	D2
	INT03_1		94	78	L11
	INT03_2		28	-	H3
	INT04_0	External interrupt request 04 input pin	31	-	H6
	INT04_1		97	81	K14
	INT04_2		29	-	H4
	INT05_0	External interrupt request 05 input pin	127	103	D13
	INT05_1		100	84	J12
	INT05_2		30	-	H5
	INT06_0	External interrupt request 06 input pin	170	-	B4
	INT06_1		126	102	D12
	INT06_2		64	56	K6
	INT07_0	External interrupt request 07 input pin	171	-	C4
	INT07_1		70	62	P8
	INT07_2		16	16	F3
	INT08_0	External interrupt request 08 input pin	172	140	B3
	INT08_1		33	-	J4
	INT08_2		19	19	F6
	INT09_0	External interrupt request 09 input pin	119	95	F11
	INT09_1		34	26	J3
	INT09_2		22	22	G4
	INT10_0	External interrupt request 10 input pin	76	-	K9
	INT10_1		35	27	J2
	INT10_2		7	7	D1
	INT11_0	External interrupt request 11 input pin	77	-	P10
	INT11_1		36	28	K1
	INT11_2		71	63	J8
	INT12_0	External interrupt request 12 input pin	78	-	N10
	INT12_1		46	38	N2
	INT12_2		72	64	P9
	INT13_0	External interrupt request 13 input pin	81	-	M10
	INT13_1		47	39	N3
	INT13_2		66	58	N8
	INT14_0	External interrupt request 14 input pin	82	-	N11
	INT14_1		58	50	M5
	INT14_2		67	59	M8

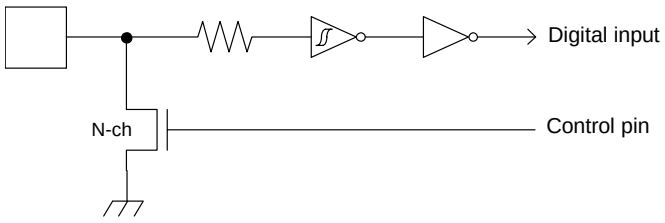
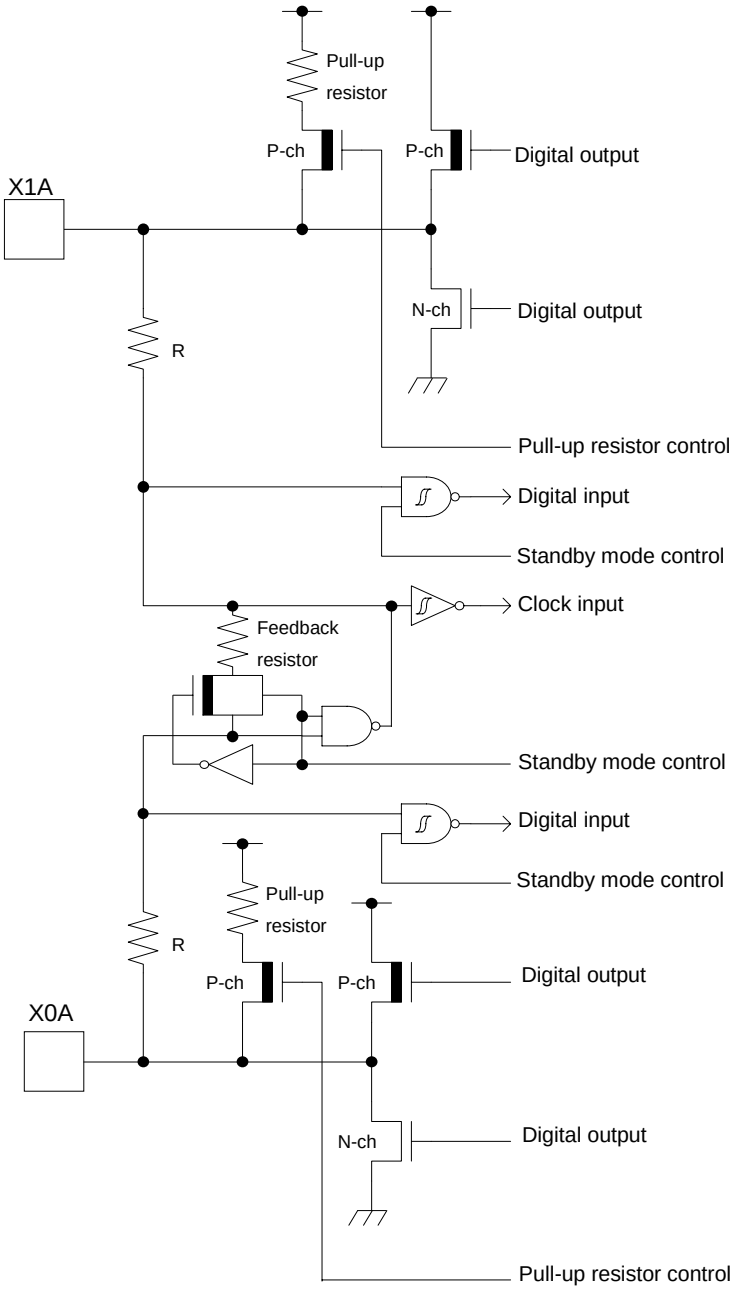
Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
GPIO	P60	General-purpose I/O port 6	169	139	C5
	P61		168	138	B5
	P62		167	137	E6
	P70	General-purpose I/O port 7	65	57	J6
	P71		66	58	N8
	P72		67	59	M8
	P73		68	60	L8
	P74		69	61	K8
	P75		70	62	P8
	P76		71	63	J8
	P77		72	64	P9
	P78		73	65	N9
	P79		74	66	M9
	P7A		75	67	L9
	P7B		76	-	K9
	P7C		77	-	P10
	P7D		78	-	N10
	P7E		79	-	L10
	P7F		80	-	K10
	P80	General-purpose I/O port 8	174	142	A3
	P81		175	143	A2
	P82		130	106	D14
	P83		131	107	C14
	P90	General-purpose I/O port 9	139	-	C11
	P91		140	-	D11
	P92		141	-	B10
	P93		142	-	C10
	P94		143	-	D10
	P95		144	-	B9
	PA0	General-purpose I/O port A	2	2	B2
	PA1		3	3	C2
	PA2		4	4	C3
	PA3		5	5	D5
	PA4		6	6	D2
	PA5		7	7	D1
	PB0	General-purpose I/O port B	110	-	H13
	PB1		111	-	H12
	PB2		112	-	H11
	PB3		113	-	G13
	PB4		114	-	G12
	PB5		115	-	G11
	PB6		116	-	G10
	PB7		117	-	G9

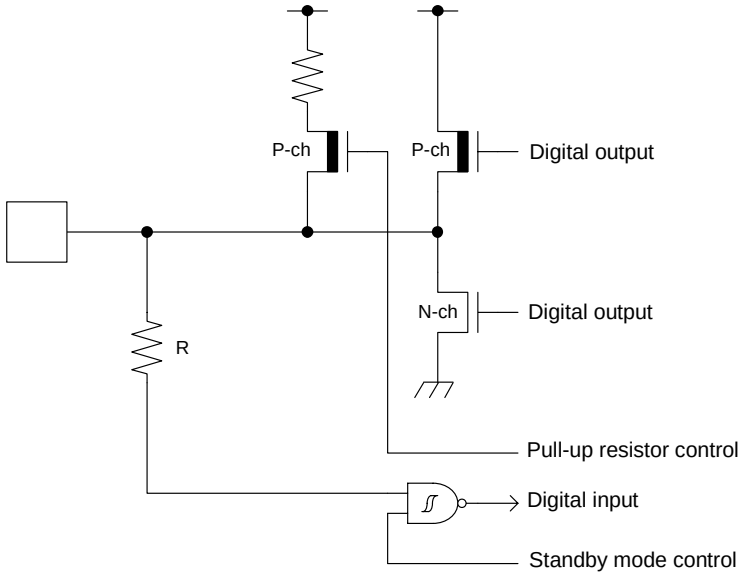
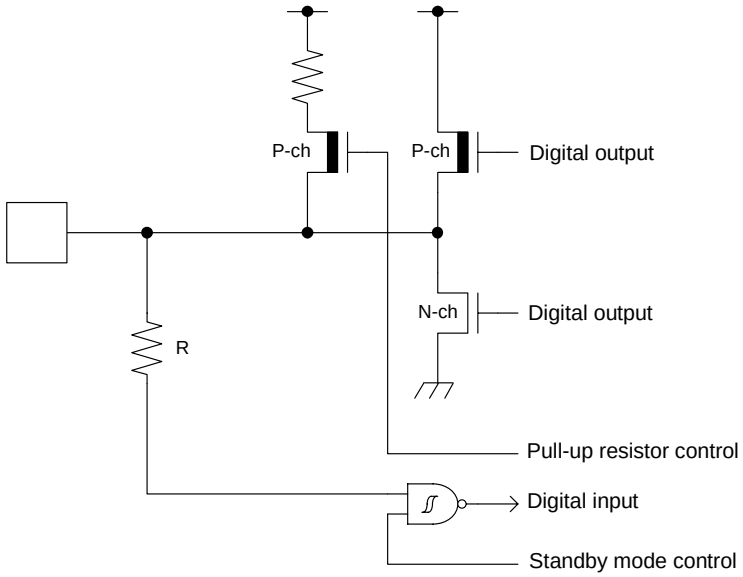
Module	Pin name	Function	Pin no		
			LQFP-176	LQFP-144	BGA-192
GPIO	PC0	General-purpose I/O port C	145	115	C9
	PC1		146	116	B8
	PC2		147	117	D9
	PC3		148	118	E9
	PC4		149	119	F9
	PC5		150	120	C8
	PC6		151	121	D8
	PC7		152	122	E8
	PC8		153	123	A10
	PC9		154	124	F8
	PCA		155	125	B7
	PCB		158	128	A7
	PCC		159	129	C7
	PCD		160	130	A6
	PCE		161	131	D7
	PCF		162	132	E7
	PD0	General-purpose I/O port D	163	133	F7
	PD1		164	134	B6
	PD2		165	135	C6
	PD3		166	136	D6
	PE0	General-purpose I/O port E	84	68	N13
	PE2		86	70	P12
	PE3		87	71	P13
	PF0	General-purpose I/O port F[1]	81	-	M10
	PF1		82	-	N11
	PF2		83	-	M11
	PF3		170	-	B4
	PF4		171	-	C4
	PF5		172	140	B3
	PF6		128	104	C13

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	16	16	F3
	SIN6_1		31	-	H6
	SIN6_2		170	-	B4
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	17	17	F4
	SOT6_1 (SDA6_1)		30	-	H5
	SOT6_2 (SDA6_2)		171	-	C4
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I^2C (operation mode 4).	18	18	F5
	SCK6_1 (SCL6_1)		29	-	H4
	SCK6_2 (SCL6_2)		172	140	B3
Multi-function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	22	22	G4
	SIN7_1		64	56	K6
	SIN7_2		110	-	H13
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	23	23	G5
	SOT7_1 (SDA7_1)		63	55	L6
	SOT7_2 (SDA7_2)		111	-	H12
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I^2C (operation mode 4).	24	24	G6
	SCK7_1 (SCL7_1)		62	54	M6
	SCK7_2 (SCL7_2)		112	-	H11

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi-function Timer 1	DTTI1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of multi-function timer 1.	19	19	F6
	DTTI1X_1		58	50	M5
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	2	2	B2
	FRCK1_1		63	55	L6
	IC10_0	16-bit input capture ch.1 input pin of multi-function timer 1. (ICxx describes channel number)	3	3	C2
	IC10_1		59	51	L5
	IC11_0		4	4	C3
	IC11_1		60	52	K5
	IC12_0		5	5	D5
	IC12_1		61	53	N6
	IC13_0		6	6	D2
	IC13_1		62	54	M6
	RTO10_0 (PPG10_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	13	13	E5
	RTO10_1 (PPG10_1)		46	38	N2
	RTO11_0 (PPG10_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	14	14	F1
	RTO11_1 (PPG10_1)		47	39	N3
	RTO12_0 (PPG12_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	15	15	F2
	RTO12_1 (PPG12_1)		48	40	M3
	RTO13_0 (PPG12_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	16	16	F3
	RTO13_1 (PPG12_1)		49	41	L4
	RTO14_0 (PPG14_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	17	17	F4
	RTO14_1 (PPG14_1)		50	42	M4
	RTO15_0 (PPG14_0)	Wave form generator output pin of multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	18	18	F5
	RTO15_1 (PPG14_1)		51	43	N4

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	28	-	H3
	AIN0_1		59	51	L5
	AIN0_2		13	13	E5
	BIN0_0	QPRC ch.0 BIN input pin	29	-	H4
	BIN0_1		60	52	K5
	BIN0_2		14	14	F1
	ZIN0_0	QPRC ch.0 ZIN input pin	30	-	H5
	ZIN0_1		61	53	N6
	ZIN0_2		15	15	F2
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch.1 AIN input pin	73	65	N9
	AIN1_1		127	103	D13
	AIN1_2		62	54	M6
	BIN1_0	QPRC ch.1 BIN input pin	74	66	M9
	BIN1_1		126	102	D12
	BIN1_2		63	55	L6
	ZIN1_0	QPRC ch.1 ZIN input pin	75	67	L9
	ZIN1_1		125	101	E13
	ZIN1_2		64	56	K6
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch.2 AIN input pin	67	59	M8
	AIN2_1		170	-	B4
	AIN2_2		115	-	G11
	BIN2_0	QPRC ch.2 BIN input pin	68	60	L8
	BIN2_1		171	-	C4
	BIN2_2		116	-	G10
	ZIN2_0	QPRC ch.2 ZIN input pin	69	61	K8
	ZIN2_1		172	140	B3
	ZIN2_2		117	-	G9
USB0	UDM0	USB ch.0 function/host D – pin	174	142	A3
	UDP0	USB ch.0 function/host D + pin	175	143	A2
	UHCONX0	USB ch.0. USB external pull-up control pin	168	138	B5
USB1	UDM1	USB ch.1 function/host D – pin	130	106	D14
	UDP1	USB ch.1 function/host D + pin	131	107	C14
	UHCONX1	USB ch.1. USB external pull-up control pin	127	103	D13

Type	Circuit	Remarks
C		■Open drain output ■CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. ■Oscillation feedback resistor : Approximately 5 MΩ ■With Standby mode control When the GPIO is selected. ■CMOS level output. ■CMOS level hysteresis input ■With pull-up resistor control ■With standby mode control ■Pull-up resistor : Approximately 50 kΩ ■I_{OH} = -4 mA, I_{OL} = 4 mA

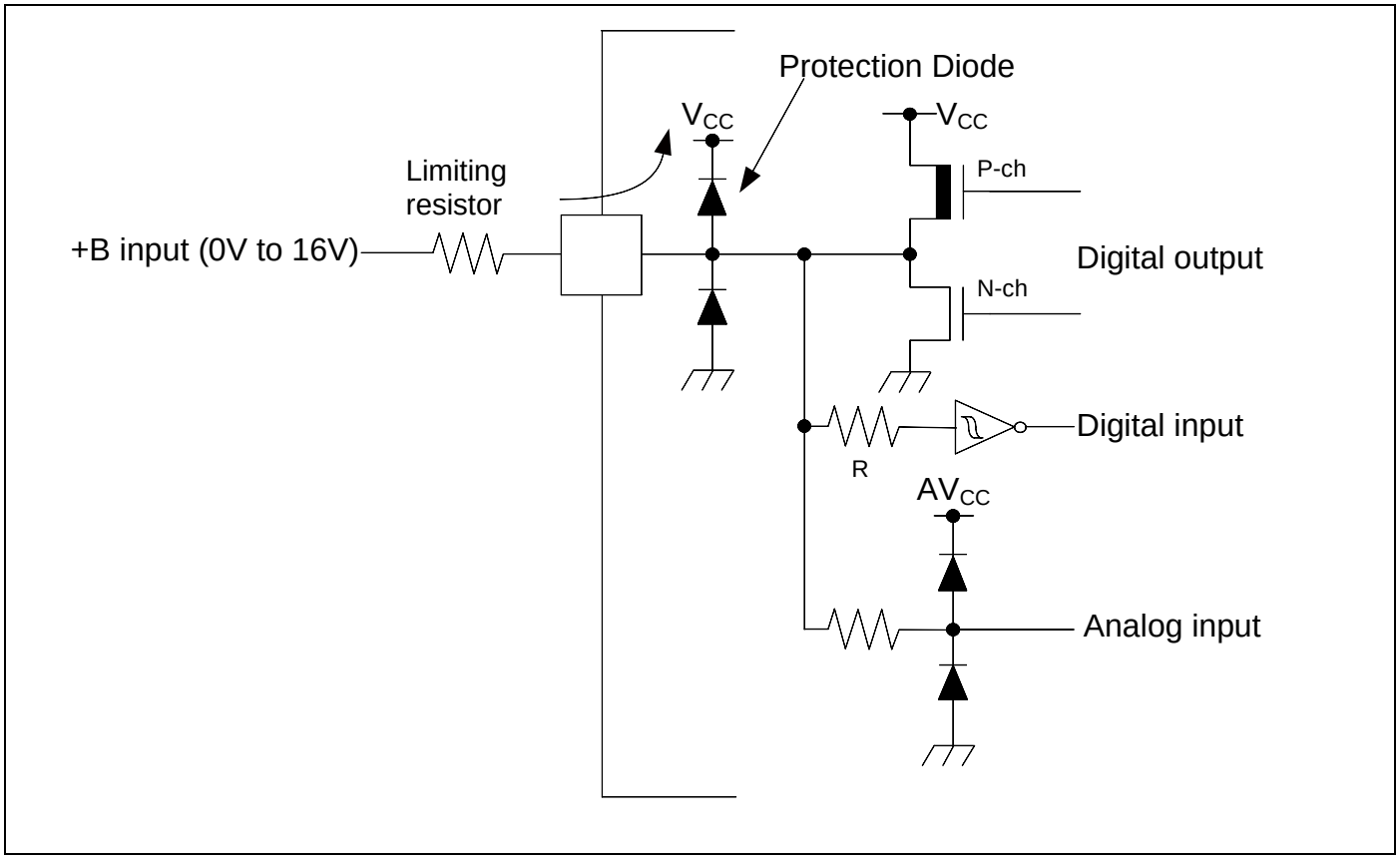
Type	Circuit	Remarks
K		■CMOS level output ■TTL level hysteresis input ■With pull-up resistor control ■With standby mode control ■Pull-up resistor : Approximately 50 kΩ ■I_{OH} = -4 mA, I_{OL} = 4 mA
L		■CMOS level output ■CMOS level hysteresis input ■With pull-up resistor control ■With standby mode control ■Pull-up resistor : Approximately 50 kΩ ■I_{OH} = -8 mA, I_{OL} = 8 mA ■When this pin is used as an I^2C pin, the digital output P-ch transistor is always off ■+B input is available

[7]: The average output is the average current for a single pin over a period of 100 ms.

[8]: The total average output current is the average current for all pins over a period of 100 ms.

[9]:

- See "4. List of Pin Functions" and "5. I/O Circuit Type" about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



WARNING:

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

12.4.8 External Bus Timing

External bus clock output characteristics

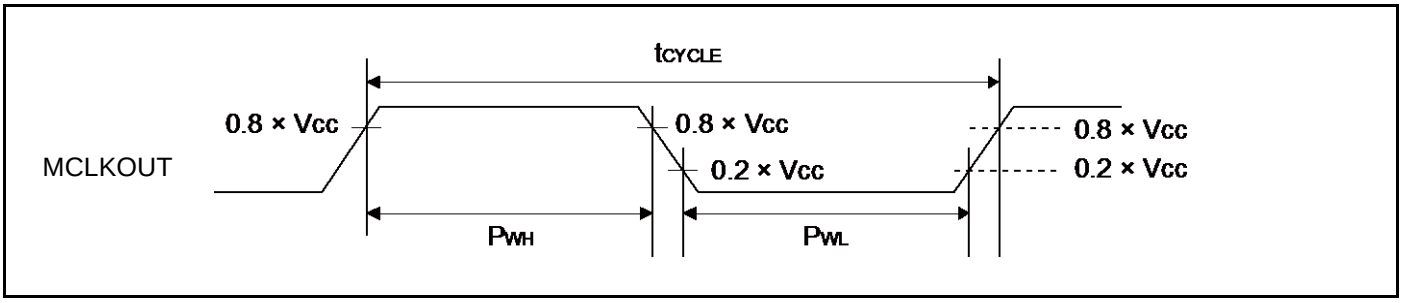
(Vcc = 2.7 V to 5.5V, Vss = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT[1]	Vcc ≥ 4.5 V	-	50[2]	MHz
			Vcc < 4.5 V	-	32[3]	MHz

[1]: External bus clock (MCLKOUT) is divided clock of HCLK.
For more information about setting of clock divider, see "Chapter 12: External Bus Interface" in "FM3 Family Peripheral Manual".
When external bus clock is not output, this characteristic does not give any effect on external bus operation.

[2]: When AHB bus clock frequency is more than 100 MHz, the divider setting for MCLKOUT must be more than 4.

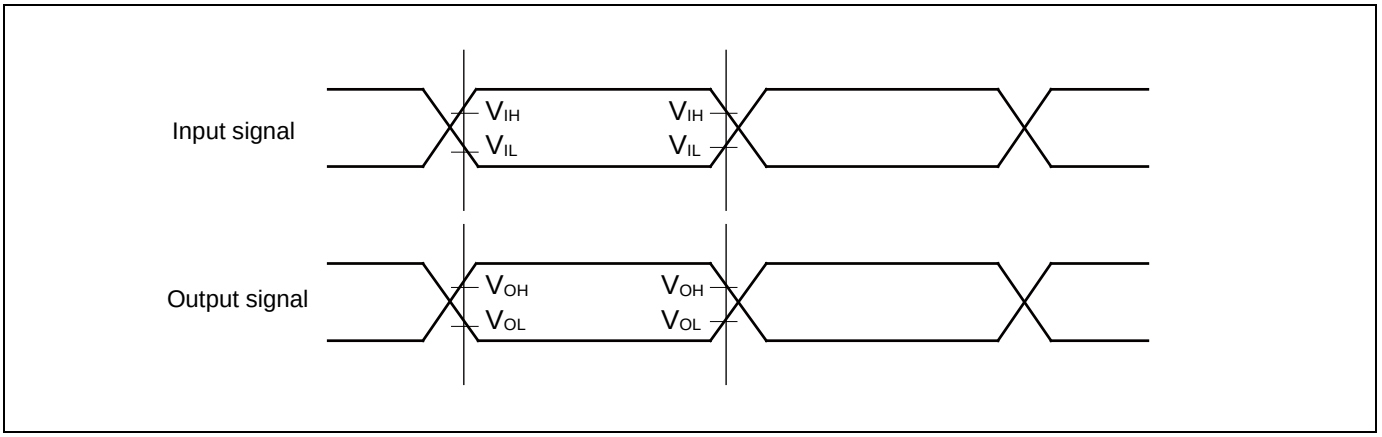
[3]: When AHB bus clock frequency is more than 64 MHz, the divider setting for MCLKOUT must be more than 4.



External bus signal input/output characteristics

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



Separate bus access asynchronous SRAM mode

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MOEX Min pulse width	t_{OEW}	MOEX	Vcc ≥ 4.5 V	MCLK×n-3	-	ns
			Vcc < 4.5 V			
MCSX ↓ → Address output delay time	t_{CSL-AV}	MCSX[7:0], MAD[24:0]	Vcc ≥ 4.5 V	-9	+9	ns
			Vcc < 4.5 V	-12	+12	
MOEX ↑ → Address hold time	t_{OEH-AX}	MOEX, MAD[24:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL-OEL}$	MOEX, MCSX[7:0]	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
MOEX ↑ → MCSX ↑ time	$t_{OEH-CSH}$		Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-RDQML}$	MCSX, MDQM[1:0]	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
Data set up → MOEX ↑ time	t_{DS-OE}	MOEX, MADATA[15:0]	Vcc ≥ 4.5 V	20	-	ns
			Vcc < 4.5 V	38	-	
MOEX ↑ → Data hold time	t_{DH-OE}	MOEX, MADATA[15:0]	Vcc ≥ 4.5 V	0	-	ns
			Vcc < 4.5 V			
MWEX Min pulse width	t_{WEW}	MWEX	Vcc ≥ 4.5 V	MCLK×n-3	-	ns
			Vcc < 4.5 V			
MWEX ↑ → Address output delay time	t_{WEH-AX}	MWEX, MAD[24:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL-WEL}$	MWEX, MCSX[7:0]	Vcc ≥ 4.5 V	MCLK×n-9	MCLK×n+9	ns
			Vcc < 4.5 V	MCLK×n-12	MCLK×n+12	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH-CSH}$		Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	Vcc ≥ 4.5 V	MCLK×n-9	MCLK×n+9	ns
			Vcc < 4.5 V	MCLK×n-12	MCLK×n+12	
MCSX ↓ → Data output time	t_{CSL-DV}	MCSX, MADATA[15:0]	Vcc ≥ 4.5 V	MCLK-9	MCLK+9	ns
			Vcc < 4.5 V	MCLK-12	MCLK+12	
MWEX ↑ → Data hold time	t_{WEH-DX}	MWEX, MADATA[15:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	

Note: When the external load capacitance = 30 pF. (m = 0 to 15, n = 1 to 16)

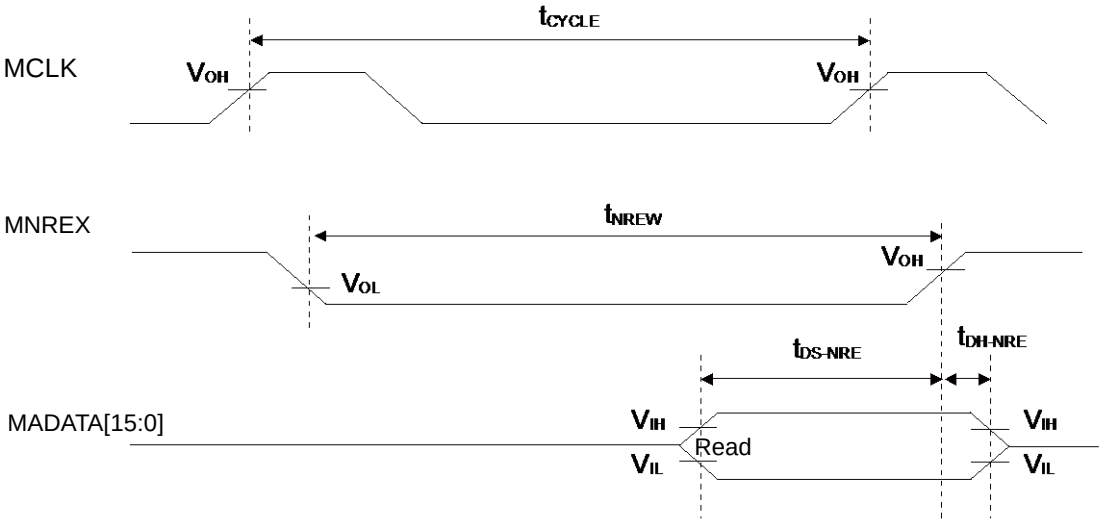
NAND flash mode

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MNREX Min pulse width	t_{NREW}	MNREX	Vcc ≥ 4.5 V Vcc < 4.5 V	MCLK×n-3	-	ns
Data setup → MNREX↑time	t_{DS-NRE}	MNREX, MADATA[15:0]	Vcc ≥ 4.5 V Vcc < 4.5 V	20 38	- -	ns
MNREX↑→ Data hold time	t_{DH-NRE}	MNREX, MADATA[15:0]	Vcc ≥ 4.5 V Vcc < 4.5 V	0	-	ns
MNALE↑→ MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	Vcc ≥ 4.5 V Vcc < 4.5 V	MCLK×m-9 MCLK×m-12	MCLK×m+9 MCLK×m+12	ns
MNALE↓→ MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	Vcc ≥ 4.5 V Vcc < 4.5 V	MCLK×m-9 MCLK×m-12	MCLK×m+9 MCLK×m+12	ns
MNCLE↑→ MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	Vcc ≥ 4.5 V Vcc < 4.5 V	MCLK×m-9 MCLK×m-12	MCLK×m+9 MCLK×m+12	ns
MNWEX↑→ MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	Vcc ≥ 4.5 V Vcc < 4.5 V	0	MCLK×m+9 MCLK×m+12	ns
MNWEX Min pulse width	t_{NWEW}	MNWEX	Vcc ≥ 4.5 V Vcc < 4.5 V	MCLK×n-3	-	ns
MNWEX↓→ Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[15:0]	Vcc ≥ 4.5 V Vcc < 4.5 V	-9 -12	+9 +12	ns
MNWEX↑→ Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[15:0]	Vcc ≥ 4.5 V Vcc < 4.5 V	0	MCLK×m+9 MCLK×m+12	ns

Note: When the external load capacitance = 30 pF. (m=0 to 15, n=1 to 16)

NAND Flash Read



CSIO (SPI = 1, SCINV = 0)

(Vcc = 2.7 V to 5.5 V, Vss = 0 V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function Serial is connected to, see “8. Block Diagram” in this datasheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance = 30 pF.

12.4.16 Ethernet-MAC Timing

RMII transmission (100 Mbps/10 Mbps)

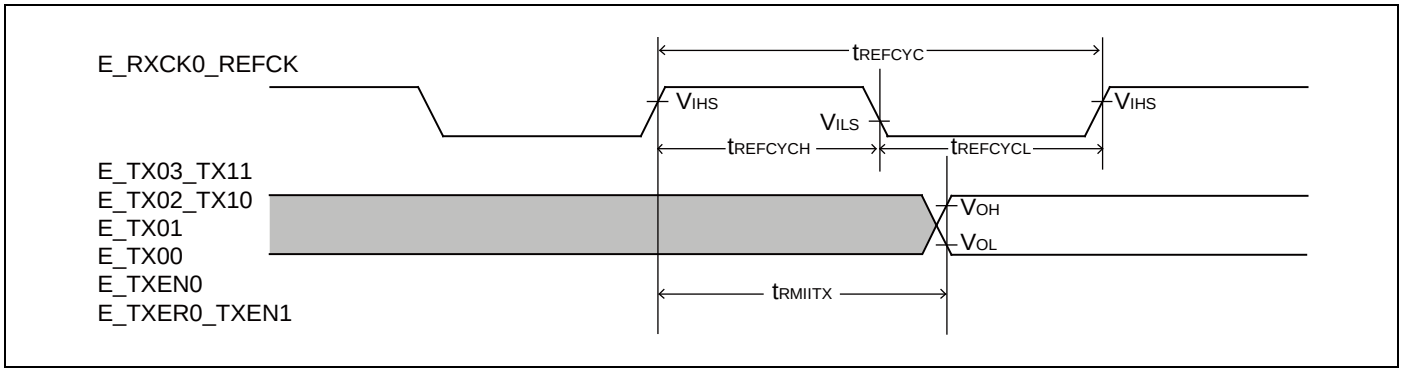
(ETHVcc = 3.0 V to 3.6 V, 4.5 V to 5.5 V[1])

(Vss = 0 V, Ta = - 40°C to + 85°C, C_L=25 pF)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Reference Clock Cycle time[2]	t_{REFCYC}	E_RXCK0_REFCK	20 ns (typical)	-	-	ns
Reference Clock High pulse width duty	$t_{REFCYCH}$	E_RXCK0_REFCK	$t_{REFCYCH}$ / t_{REFCYC}	35	65	%
Reference Clock Low pulse width duty	$t_{REFCYCL}$	E_RXCK0_REFCK	$t_{REFCYCL}$ / t_{REFCYC}	35	65	%
REFCK ↑ → Transmitted data Delay time (ch.0)	t_{RMIITX}	E_TX01, E_TX00, E_TXEN0	-	-	12	ns
REFCK ↑ → Transmitted data Delay time (ch.1)		E_TX03_TX11, E_TX02_TX10, E_TXER0_TXEN1				

[1]: When ETHV = 4.5 V to 5.5 V, it is recommended to add a series resistor at the output pin to suppress the output current.

[2]: The reference clock is fixed to 50 MHz in the RMII specifications. The clock accuracy should meet the PHY-device specifications.

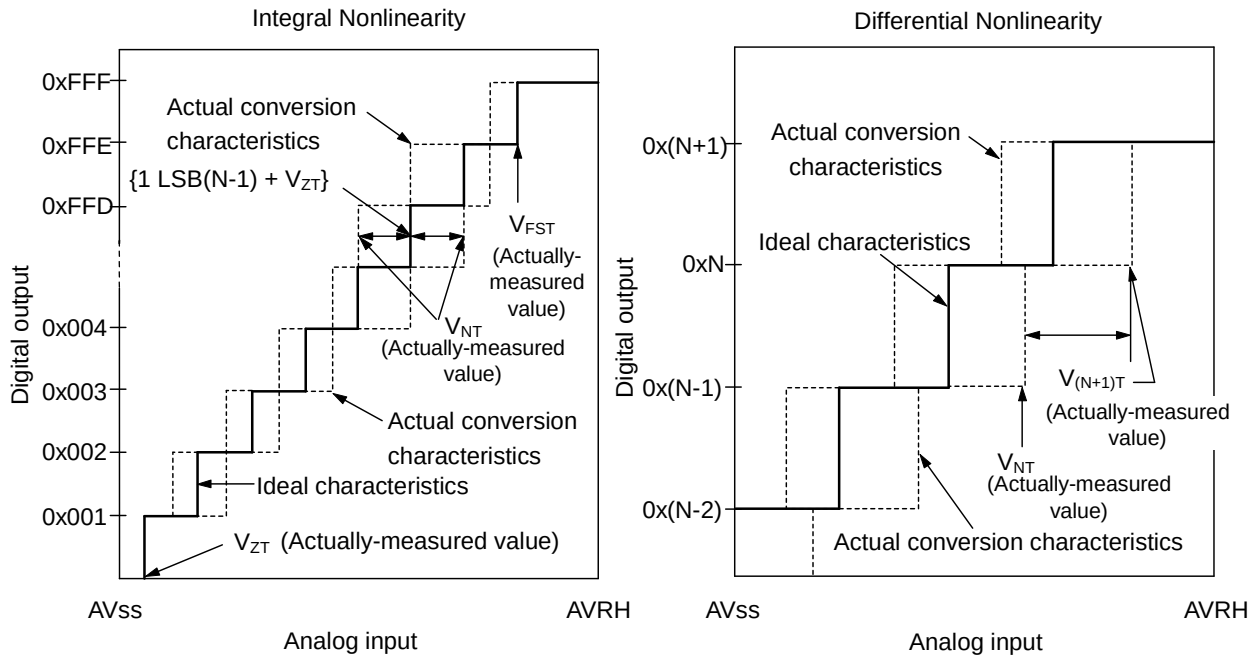


Definition of 12-bit A/D converter terms

■Resolution : Analog variation that is recognized by an A/D converter.

■Integral Nonlinearity : Deviation of the line between the zero-transition point (0b000000000000⟷0b000000000001) and the full-scale transition point (0b111111111110⟷0b111111111111) from the actual conversion characteristics.

■Differential Nonlinearity : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



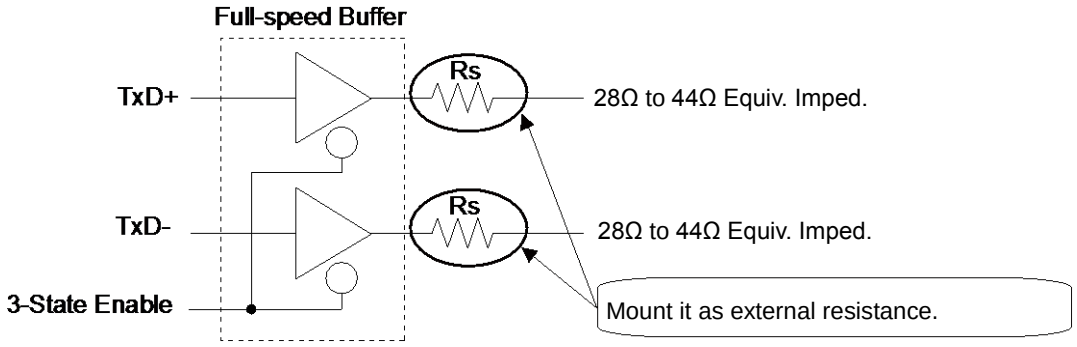
$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

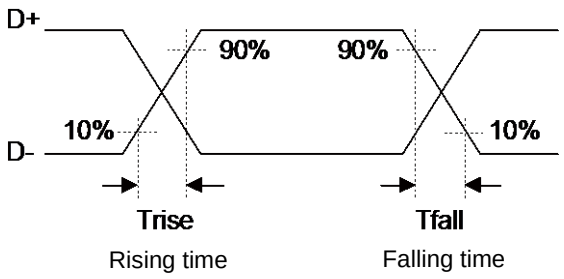
N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

[6]: USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15% characteristic impedance (Differential Mode). USB standard defines that output impedance of USB driver must be in range from 28 Ω to 44 Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommendation value 27 Ω) series resistor Rs.



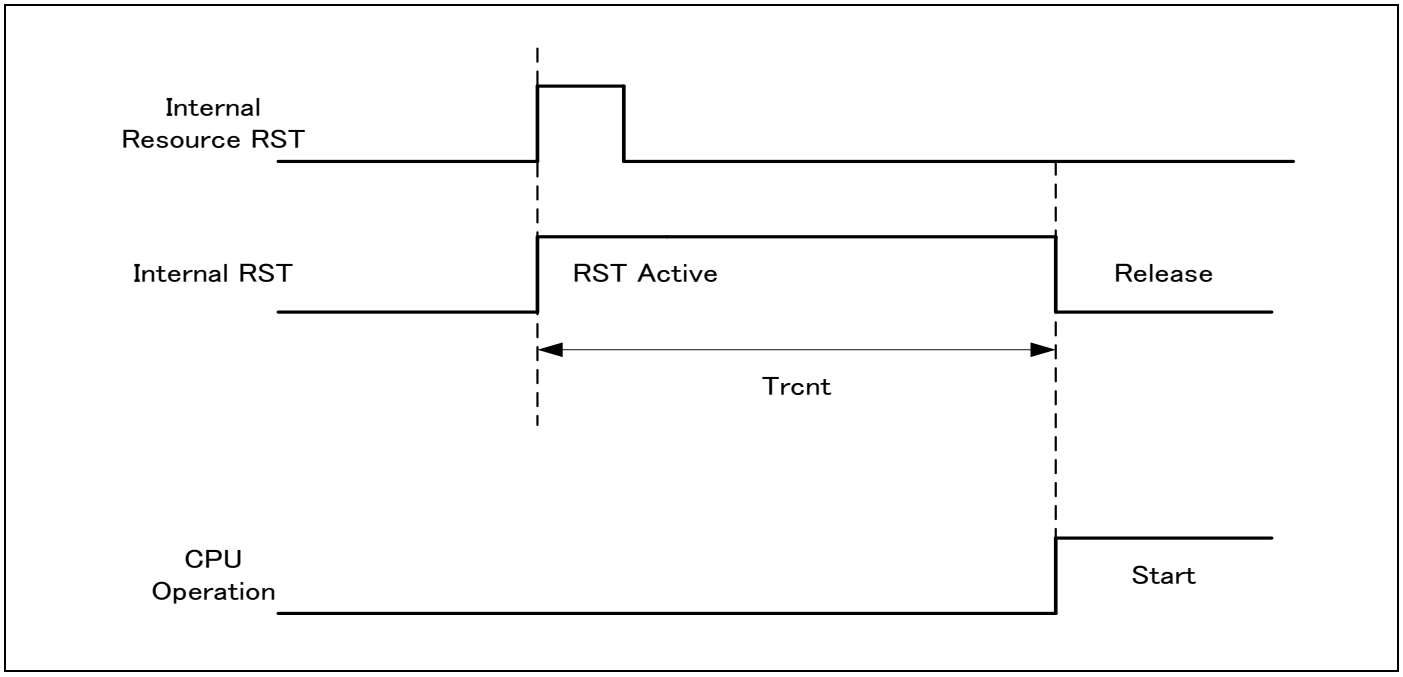
Rs series resistor 25 Ω to 30 Ω
Series resistor of 27 Ω (recommendation value) must be added.
And, use "resistance with an uncertainty of 5% by E24 sequence".

[7]: They indicate rise time (Trise) and fall time (Tfall) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.



See Figure "Low-speed load (compliance load)" for conditions of external load.

Operation example of return from low power consumption mode (by internal resource reset[1])



[1]: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- The return factor is different in each Low-Power consumption modes.
  See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual.
- When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual"
- The time during the power-on reset/low-voltage detection reset is excluded. See "12.4.7. Power-on Reset Timing in 12.4. AC Characteristics 12. Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset
- When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time
- The internal resource reset means the watchdog reset and the CSV reset.

13. Ordering Information

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9BFD16SPMC-GE1	512 KB	64 KB	Plastic · LQFP 144-pin (0.5 mm pitch), (FPT-144P-M08)	Tray
MB9BFD17SPMC-GE1	768 KB	96 KB		
MB9BFD18SPMC-GE1	1 MB	128 KB		
MB9BFD16TPMC-GE1	512 KB	64 KB	Plastic · LQFP 176-pin (0.5 mm pitch), (FPT-176P-M07)	
MB9BFD17TPMC-GE1	768 KB	96 KB		
MB9BFD18TPMC-GE1	1 MB	128 KB		
MB9BFD16TBGL-GE1	512 KB	64 KB	Plastic · PFBGA 192-pin (0.8 mm pitch), (BGA-192P-M06)	
MB9BFD17TBGL-GE1	768 KB	96 KB		
MB9BFD18TBGL-GE1	1 MB	128 KB		

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