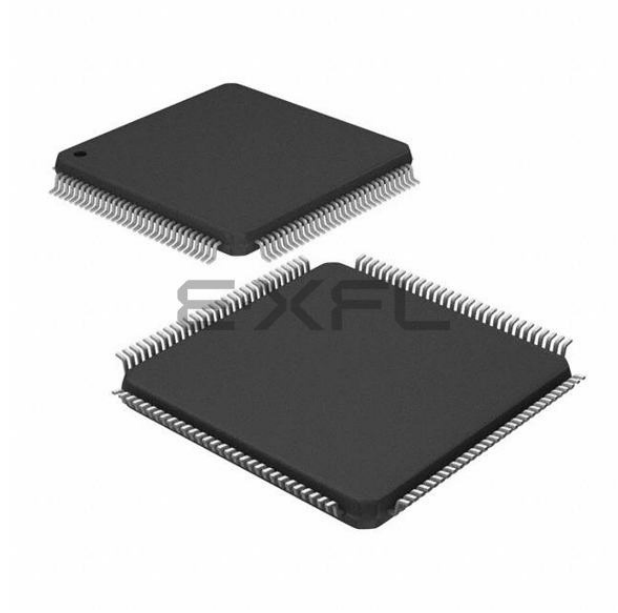

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	90
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2dh5gjamv20000

1. Product Lineup

Memory Size

Product Name		S6E2DH5G0A S6E2DH5J0A	S6E2DH5GJA
On-chip Flash memory		384 Kbytes	
On-chip SRAM	SRAM	36 Kbytes	
	SRAM0	32 Kbytes	
	SRAM2	4 Kbytes	
VRAM for GDC		512 Kbytes	
VFLASH for GDC		-	2 Mbytes

Function

Product Name			S6E2DH5G0A	S6E2DH5J0A	S6E2DH5GJA
Pin count			120/161	176	120
CPU			Cortex-M4F, MPU, NVIC 128ch.		
		Freq.	160 MHz		
Power supply voltage range			2.7 V to 3.6 V		
USB2.0 (Device/Host)			1ch.		
CAN-FD (non-ISO CAN FD)			1ch.		
DMAC			8ch.		
DSTC			128ch.		
GDC unit	Graphics・Display controller		1 unit		
	High-Speed Quad SPI		1ch.		(VFLASH only)
	Hyper Bus Interface		1 unit		-
	SDRAM-IF		-	1ch.	-
External Bus Interface			Addr:25-bit (Max), Data: 8-/16-bit, CS:2 (Max) SRAM, NOR Flash, NAND Flash, SDRAM		
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			8ch. (Max)		
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)		
MF Timer	A/D activation compare	6ch.	1 unit		
	Input capture	4ch.			
	Free-run timer	3ch.			
	Output compare	6ch.			
	Waveform generator	3ch.			
	PPG	3ch.			
SD Card Interface			1 unit		
I^{2}S			2 units		
QPRC			1ch.		
Dual Timer			1 unit		
Real-Time Clock			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes(Fixed, Programmable)		
Watchdog Timer			1ch. (SW) + 1ch. (HW)		
External Interrupts			16 pins (Max)+ NMI × 1		
I/O ports			98 pins (Max)	154 pins (Max)	90 pins (Max)
12-bit A/D converter			24ch. (2 units)		
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2ch.		
Built-in CR		High-speed	4 MHz		
		Low-speed	100 kHz		
Debug Function			SWJ-DP/ETM		
Unique ID			Yes		

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DH5GJA)	FBGA161			
113	—	—	—	PC7	K	I
				GE_SDBA0		
114	—	—	—	PC8	K	I
				GE_SDA11		
115	—	—	—	PC9	K	I
				GE_SDA10		
116	78	78	F12	P1C	F	M
				AN12		
				SCS60_1		
				TIOA6_0		
				INT14_0		
				RTO03_1 (PPG02_1)		
				MADATA12_0		
117	79	79	F13	P1D	F	M
				AN13		
				SIN6_1		
				TIOB6_0		
				INT15_0		
				RTO04_1 (PPG04_1)		
				MADATA13_0		
118	80	80	E10	P1E	F	L
				AN14		
				SOT6_1 (SDA6_1)		
				TIOA7_0		
				RTO05_1 (PPG04_1)		
				MADATA14_0		
119	81	81	E11	P1F	F	L
				AN15		
				SCK6_1 (SCL6_1)		
				TIOB7_0		
				MADATA15_0		

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DH5GJA)	FBGA161			
141	94	94	C11	P02 TDI MAD24_0	E	H
142	95	95	B11	P03 TMS SWDIO	E	G
143	96	96	B10	P04 TDO SWO	E	G
144	–	–	–	PD5 GE_SDA0	K	I
145	–	–	–	PD6 GE_SDDQM3	K	I
146	–	–	–	PD7 GE_SDDQM2	K	I
147	–	–	–	PD8 GE_SDDQM1	K	I
148	–	–	–	PD9 GE_SDDQM0	K	I
149	97	97	C10	P05 RX2_2 INT10_1 PNL_PD15 MAD18_0	E	K
150	98	98	D9	P06 TX2_2 PNL_PD14 MAD17_0	E	I
151	99	99	C9	P07 SIN2_1 INT11_1 PNL_PD13 MAD16_0	E	K
152	100	100	B9	P08 SOT2_1 (SDA2_1) PNL_PD12 MAD15_0	E	I
153	101	101	A9	P09 SCK2_1 (SCL2_1) PNL_PD11 MAD14_0	E	I

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DH5GJA)	FBGA161			
–	–	–	A1, A5, A10, A13, D5, D6, D7, D8, E5, E6, E7, E8, E9, F5, F6, F9, G4, G5, G9, H4, H5, H9, J4, J5, J6, J7, J8, J9, J10, K4, K6, K10, L6, M6, M7, M10, N1, N6, N8, N10, N13	VSS	–	–

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DH5GJA)	FBGA161
GPIO	PB0	General-purpose I/O port B	47	–	–	–
	PB1		48	–	–	–
	PB2		49	–	–	–
	PB3		50	–	–	–
	PB4		56	–	–	–
	PB5		57	–	–	–
	PB6		58	–	–	–
	PB7		59	–	–	–
	PB8		72	–	–	–
	PB9		73	–	–	–
	PBA		74	–	–	–
	PBB		75	–	–	–
	PBC		76	–	–	–
	PBD		77	–	–	–
	PC0	General-purpose I/O port C	94	–	–	–
	PC1		95	–	–	–
	PC2		96	–	–	–
	PC3		97	–	–	–
	PC4		98	–	–	–
	PC5		99	–	–	–
	PC6		112	–	–	–
	PC7		113	–	–	–
	PC8		114	–	–	–
	PC9		115	–	–	–
	PCA		126	–	–	–
	PCB		127	–	–	–
	PCC		128	–	–	–
	PCD		129	–	–	–
	PD0	General-purpose I/O port D	134	–	–	–
	PD1		135	–	–	–
	PD2		136	–	–	–
	PD3		137	–	–	–
	PD4		138	–	–	–
	PD5		144	–	–	–
	PD6		145	–	–	–
	PD7		146	–	–	–
	PD8		147	–	–	–
	PD9		148	–	–	–
	PDA		166	–	–	–
	PDB		167	–	–	–
	PDC		168	–	–	–
	PDD		169	–	–	–

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DH5GJA)	FBGA161
I²S 0	I2SMCLK0_0	I²S ch.0 external clock pin	6	2	2	C3
	I2SDO0_0	I²S ch.0 serial transition data output pin	7	3	3	C2
	I2SWS0_0	I²S ch.0 frame synchronization signal pin	8	4	4	D3
	I2SDI0_0	I²S ch.0 serial received data input pin	9	5	5	D2
	I2SCK0_0	I²S ch.0 bit clock pin	10	6	6	D1
I²S 1	I2SMCLK1_0	I²S ch.1 external clock pin	51	33	33	M3
	I2SDO1_0	I²S ch.1 serial transition data output pin	52	34	34	L4
	I2SWS1_0	I²S ch.1 frame synchronization signal pin	53	35	35	M4
	I2SDI1_0	I²S ch.1 serial received data input pin	54	36	36	K5
	I2SCK1_0	I²S ch.1 bit clock pin	55	37	37	L5
GDC High-Speed Quad SPI	GE_SPCK	SPI clock output pin	34	20	-	J1
	GE_SPDQ0	SPI data input / output pin	35	21	-	K1
	GE_SPDQ1		38	24	-	J2
	GE_SPDQ2		39	25	-	J3
	GE_SPDQ3		36	22	-	H2
	GE_SPCSX0	SPI chip select output pin	37	23	-	H3
GDC HyperBus I/F	GE_HBCK	HBI clock output pin	34	20	-	J1
	GE_HBDQ0	HBI data input / output pin	36	22	-	H2
	GE_HBDQ1		37	23	-	H3
	GE_HBDQ2		38	24	-	J2
	GE_HBDQ3		39	25	-	J3
	GE_HBDQ4		40	26	-	K2
	GE_HBDQ5		41	27	-	K3
	GE_HBDQ6		42	28	-	L2
	GE_HBDQ7		43	29	-	L3
	GE_HBCSX0	HBI chip select output pin	35	21	-	K1
	GE_HBCSX1		12	8	-	E4
	GE_HBRWDS	HBI RWDS input / output pin	33	19	-	G2
	GE_HBRESETX	HBI hardware reset output pin	25	15	-	F3
	GE_HBINTX	HBI interrupt input pin	26	16	-	F2
	GE_HBRSTOX	HBI reset input pin	27	17	-	F1
	GE_HBWPX	HBI write protect output pin	28	18	-	G3

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									

Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7,*8 (PLL)	*5	160 MHz	185	285	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					144 MHz	179	276	mA	
					120 MHz	169	261	mA	
					100 MHz	161	250	mA	
					80 MHz	154	239	mA	
					60 MHz	146	227	mA	
					40 MHz	138	215	mA	
					20 MHz	130	204	mA	
					8 MHz	125	196	mA	
					4 MHz	124	195	mA	
			Normal operation *6,*7,*8 (PLL)	*5	160 MHz	45	122	mA	*3 When all peripheral clocks are OFF
					144 MHz	41	117	mA	
					120 MHz	36	111	mA	
					100 MHz	31	105	mA	
					80 MHz	26	99	mA	
					60 MHz	22	94	mA	
					40 MHz	17	89	mA	
					20 MHz	12	83	mA	
					8 MHz	10	80	mA	
					4 MHz	9	79	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK2=HCLK/2, PCLK1=HCLK

*5: When not operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

*6: With data access to a main flash memory.

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*8: Data access is nothing to VFLASH memory

Table 12-6 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4 (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep *5,*6 operation (PLL)	160 MHz	103	181	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
				144 MHz	98	175	mA	
				120 MHz	91	168	mA	
				100 MHz	86	162	mA	
				80 MHz	80	155	mA	
				60 MHz	74	149	mA	
				40 MHz	69	143	mA	
				20 MHz	63	137	mA	
				8 MHz	59	132	mA	
				4 MHz	58	131	mA	
			Sleep *5,*6 operation (PLL)	160 MHz	24	91	mA	*3 When all peripheral clocks are OFF
				144 MHz	22	89	mA	
				120 MHz	19	86	mA	
				100 MHz	16	83	mA	
				80 MHz	14	81	mA	
				60 MHz	11	78	mA	
				40 MHz	9	76	mA	
				20 MHz	6	73	mA	
				8 MHz	5	72	mA	
				4 MHz	4	71	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*6: Data access is nothing to VFLASH memory

12.4.8 Power-on Reset Timing

(V_{SS} = 0V)

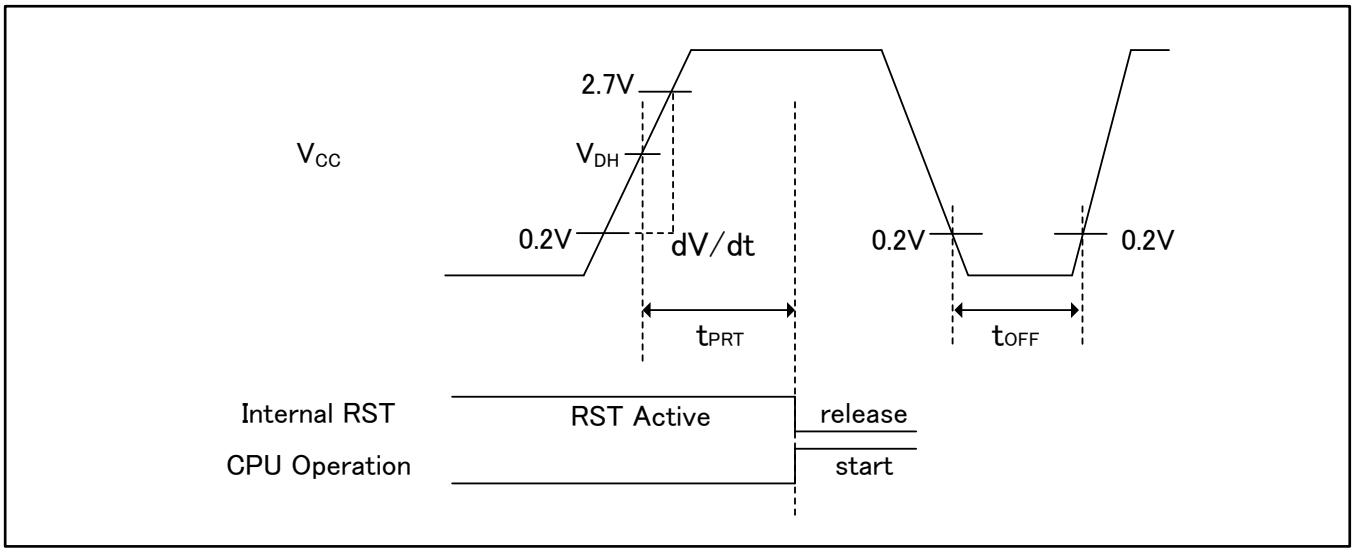
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	V_{CC}	-	1	-	-	ms	*1
Power ramp rate	dV/dt		VCC: 0.2V to 2.70V	0.6	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	0.33	-	0.60	ms	

*1: V_{CC} must be held below 0.2V for a minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (tOFF>1ms).

Note:

− *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 7.*



Glossary

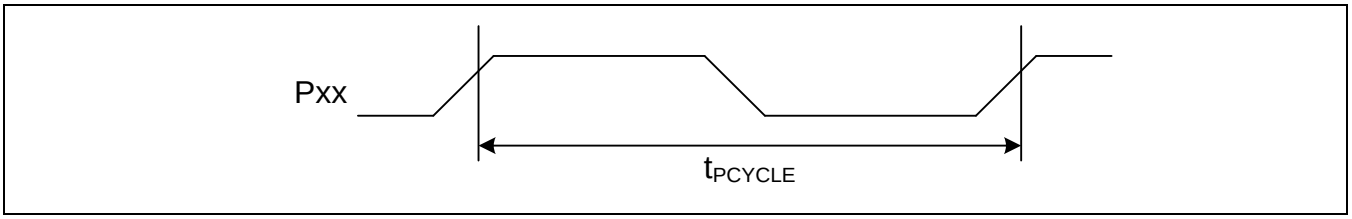
□ VDH: detection voltage of Low Voltage detection reset. See “12.7.Low-Voltage Detection Characteristics”.

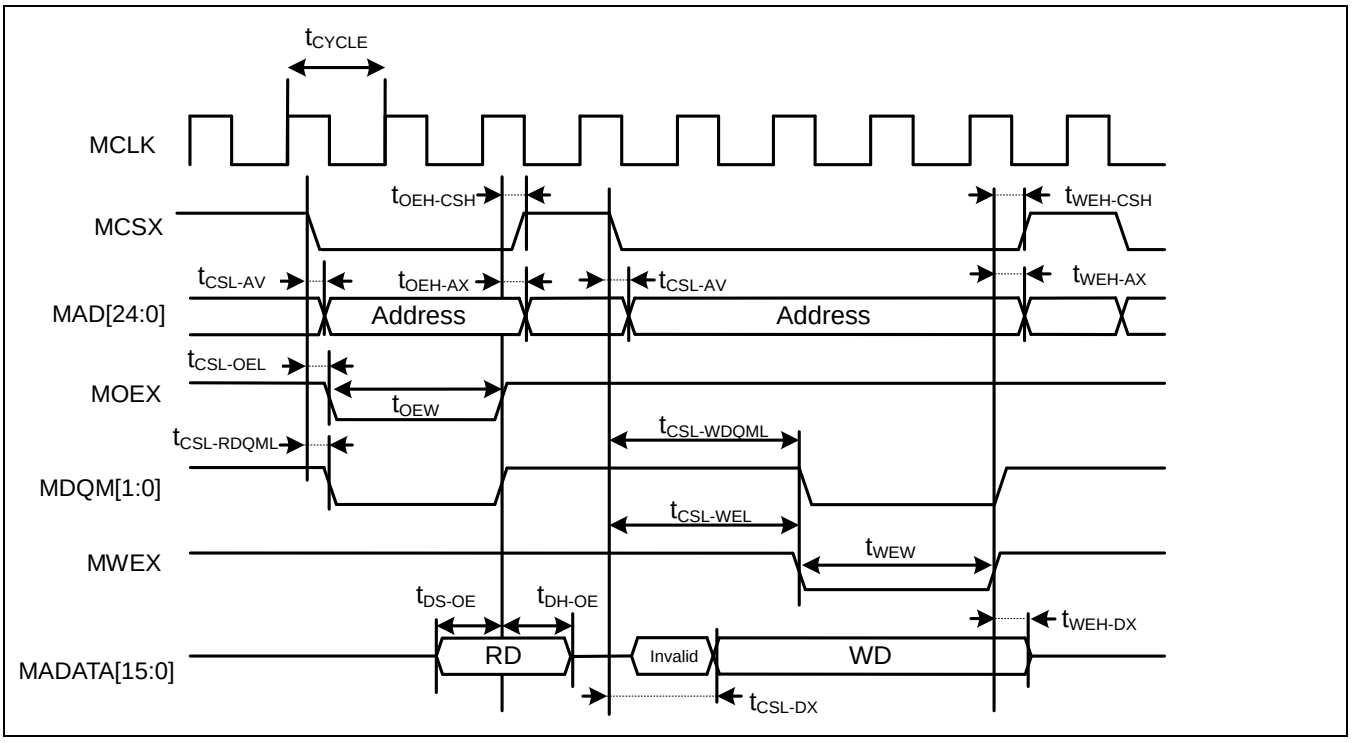
12.4.9 GPIO Output Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	t_{PCYCLE}	Pxx*	-	-	32	MHz	

*: GPIO is a target.



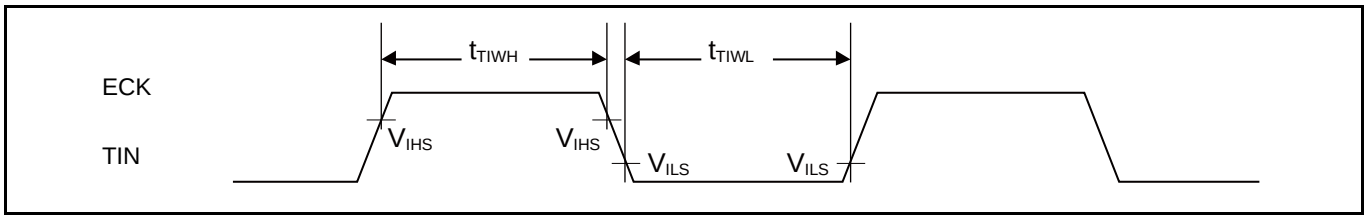

tCYCLE
MCLK
MCSX
tOEH-CSH
tWEH-CSH
MAD[24:0]
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
MOEX
tCSL-OEL
tOEW
MDQM[1:0]
tCSL-RDQML
tCSL-WDQML
tCSL-WEL
MWEX
tWEW
MADATA[15:0]
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DX

12.4.11 Base Timer Input Timing

Timer Input Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

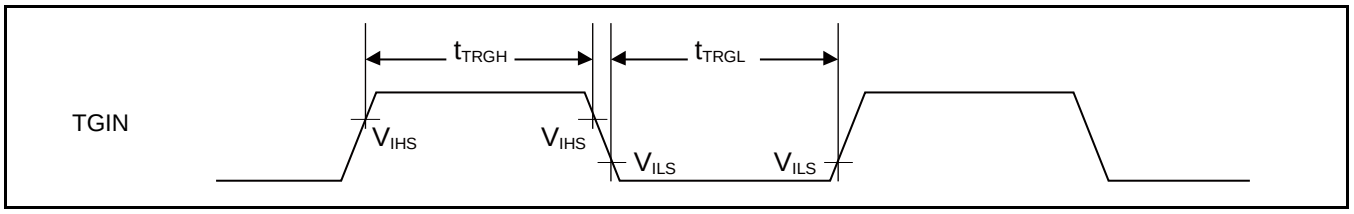
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger Input Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which the Base Timer is connected to, see 8. Block Diagram in this data sheet.

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL=1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50+5t_{CYCP}	(*3)+50+5t_{CYCP}	ns
SCS↓→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

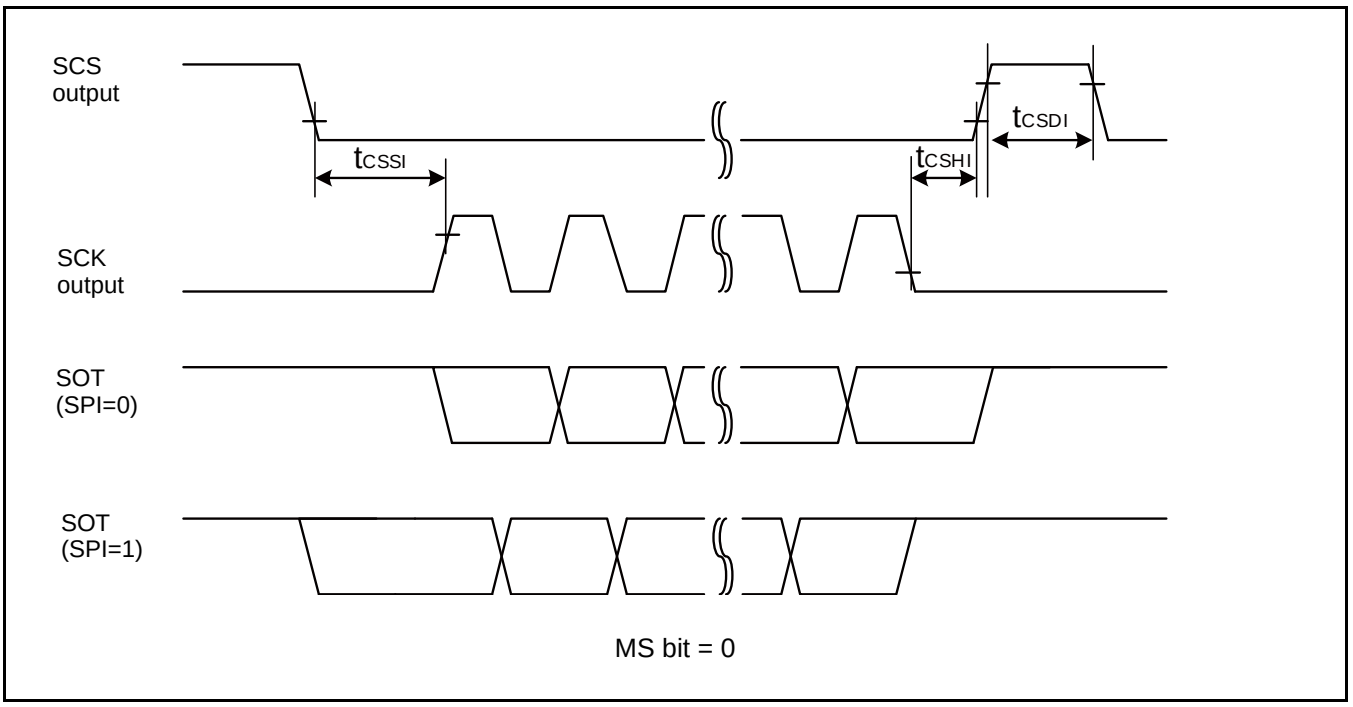
High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

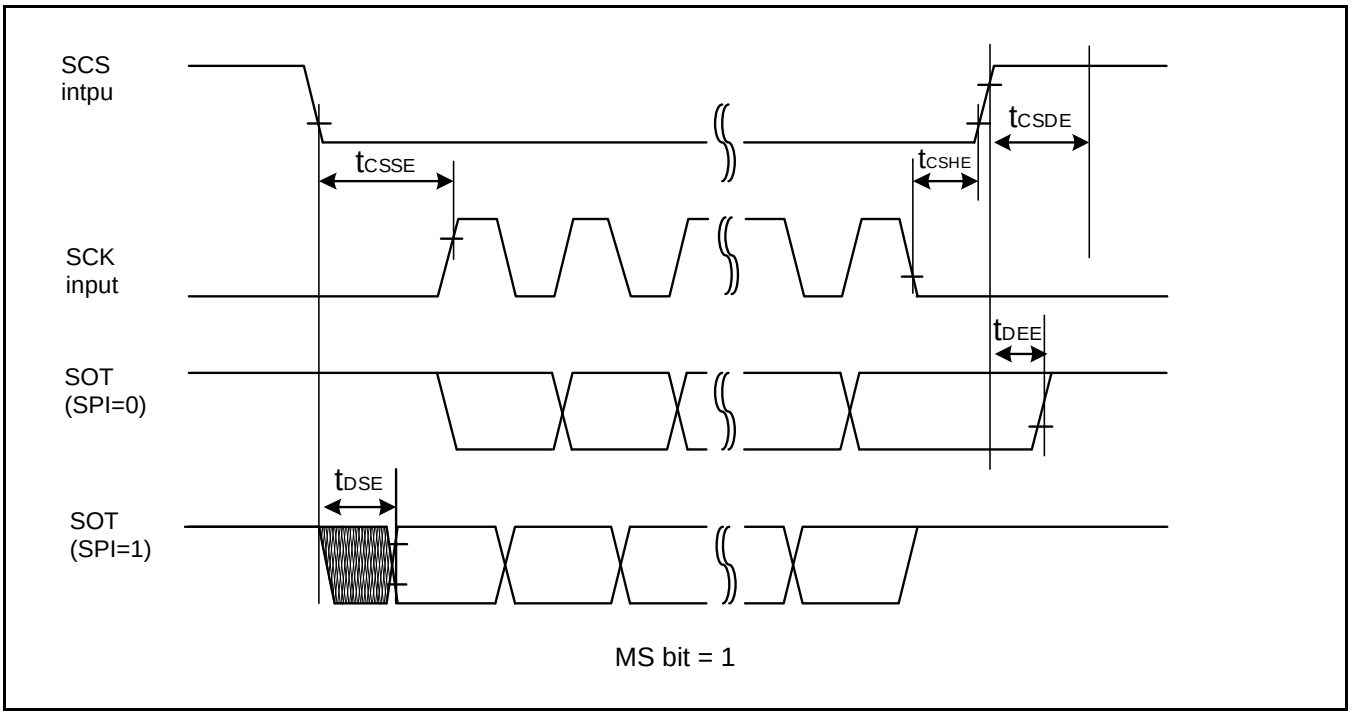
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 10	+ 10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  SIN6_0, SOT6_0, SCK6_0, SCS60_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL=0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

12.4.13 External Input Timing

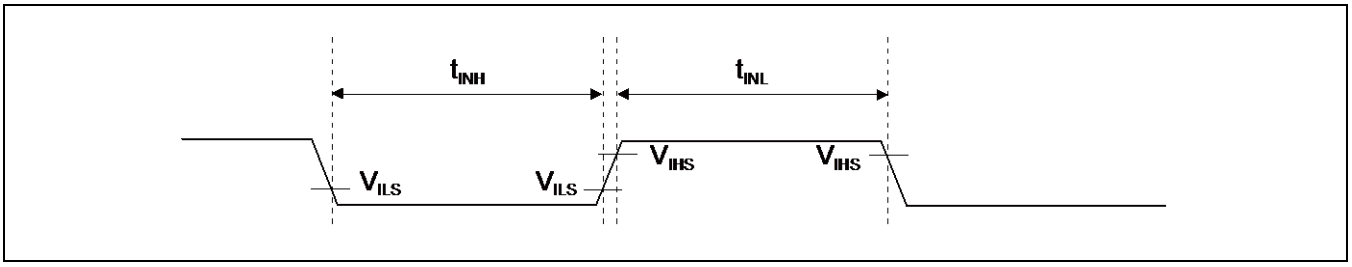
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

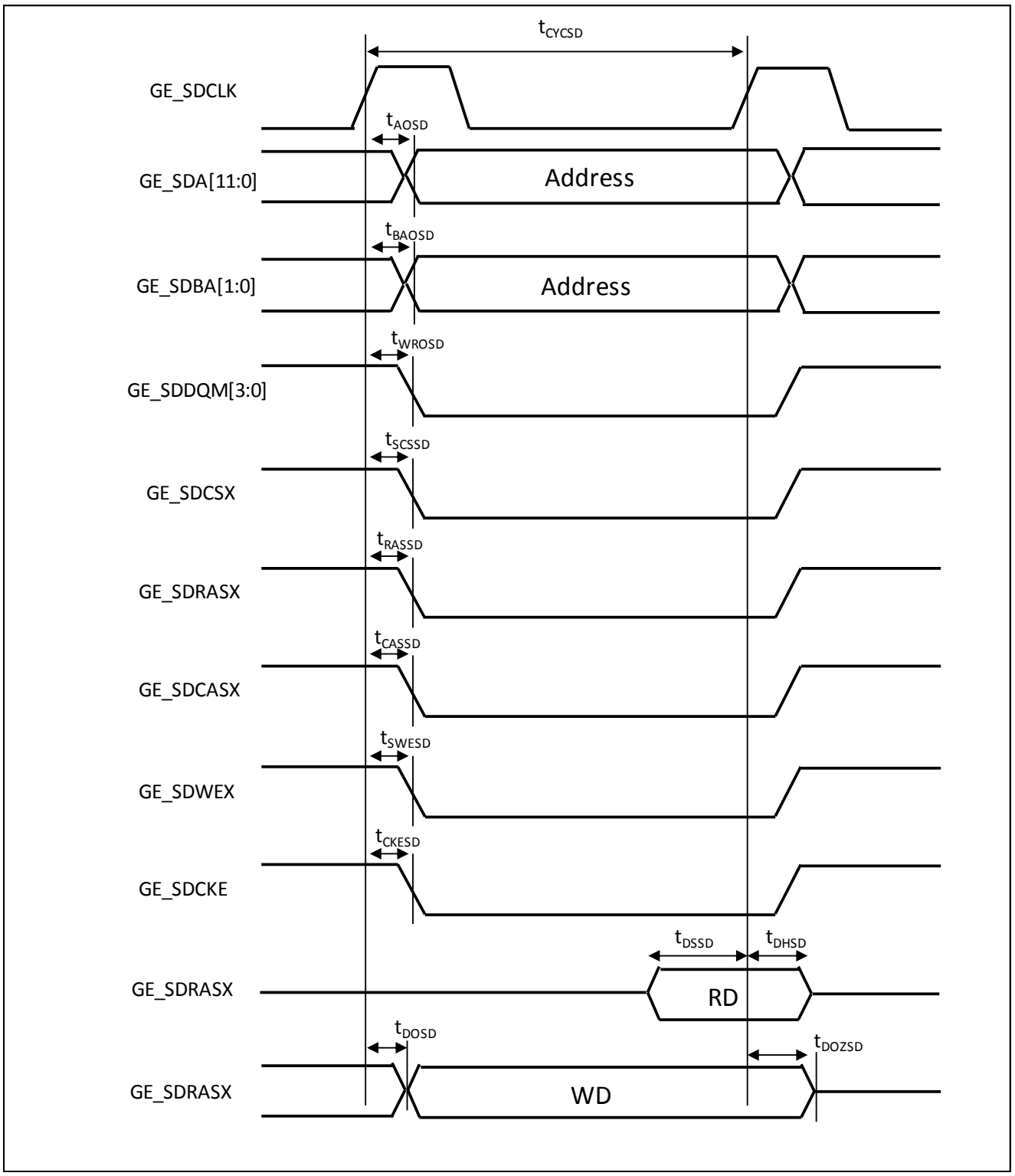
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCK0					Free-run timer input clock
		IC0x					Input capture
		DTTI0X	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INTxx, NMIX	-	$2t_{CYCP}$ + 100(*1)	-	ns	External interrupt, NMI
				500(*2)	-	ns	
		WKUPx	-	500(*3)	-	ns	Deep standby wake up

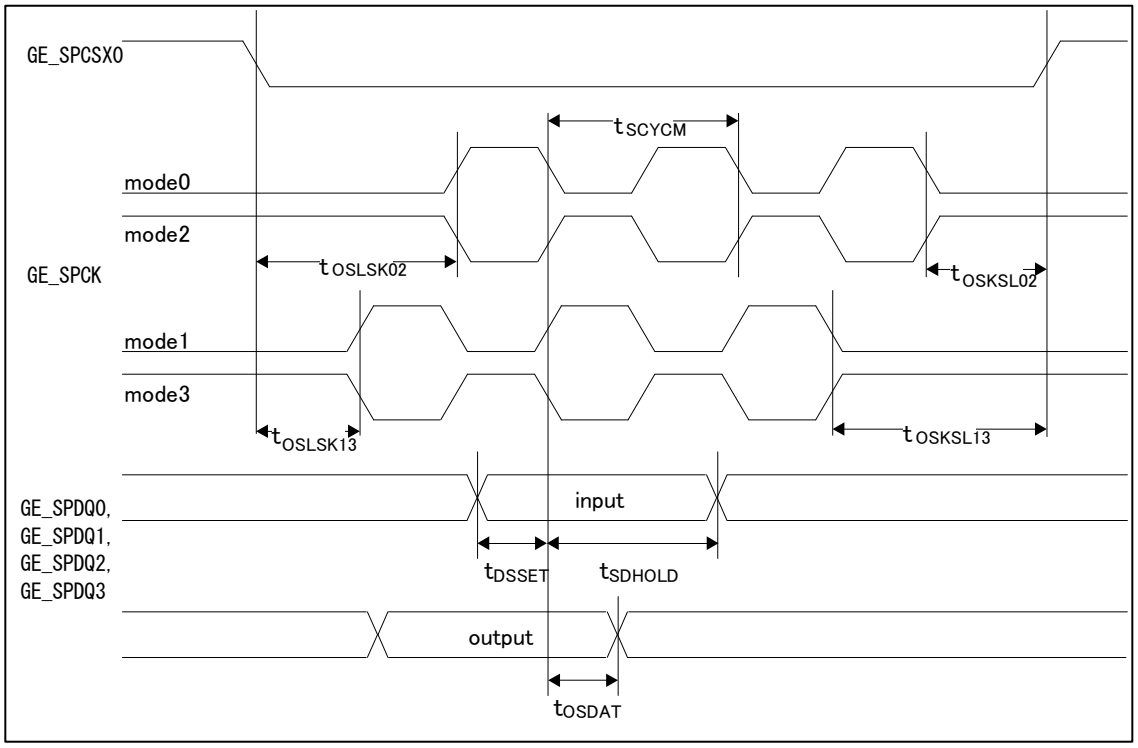
(*1): t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode. About the APB bus number which the Multi-function Timer and External interrupt are connected to, see 8. Block Diagram in this data sheet.

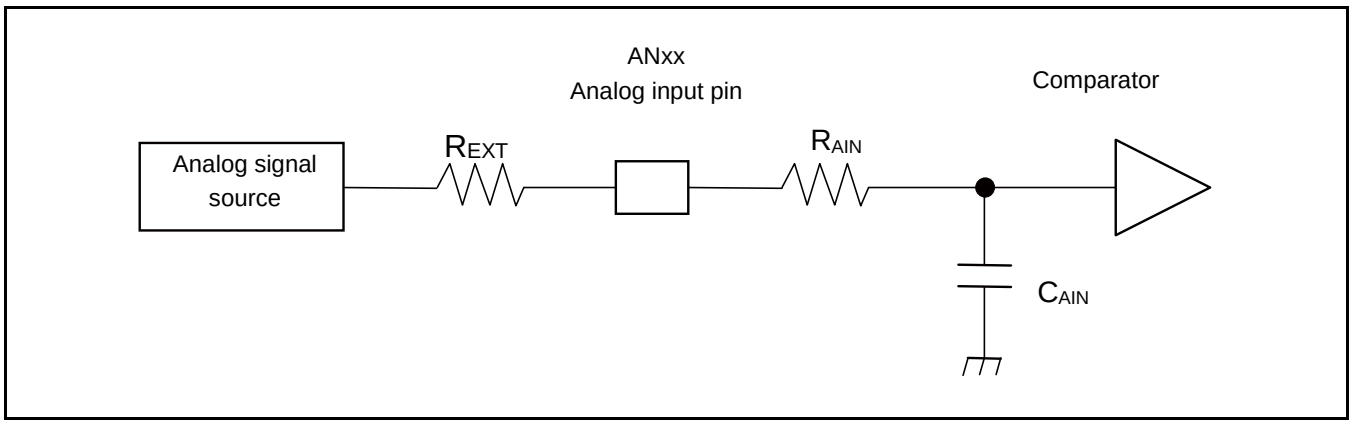
(*2): When in Stop mode, in timer mode.

(*3): When in deep standby RTC mode, in deep standby Stop mode.




tCYCSD
GE_SDCLK
tAOSD
GE_SDA[11:0]
Address
tBAOSD
GE_SDBA[1:0]
Address
tWROSD
GE_SDDQM[3:0]
tSCSSD
GE_SDCSX
tRASSD
GE_SDRASX
tCASSD
GE_SDCASX
tSWESD
GE_SDWEX
tCKESD
GE_SDCKE
tDSSD
tDHSD
GE_SDRASX
RD
tDOSD
tDOZSD
GE_SDRASX
WD


GE_SPCSX0
tSCYCM
mode0
mode2
GE_SPCK
tOSLSK02
tOSKSL02
mode1
mode3
tOSLSK13
tOSKSL13
GE_SPDQ0,
GE_SPDQ1,
GE_SPDQ2,
GE_SPDQ3
input
tDSSET
tSDHOLD
output
tOSDAT



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 1.8 kΩ

C_{AIN}: Input capacity of A/D = 12.05 pF

R_{EXT}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle