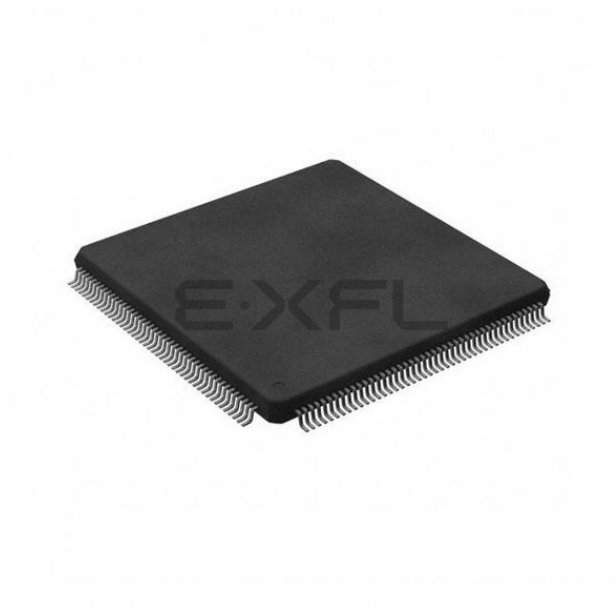

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What is "Embedded - Microcontrollers"?

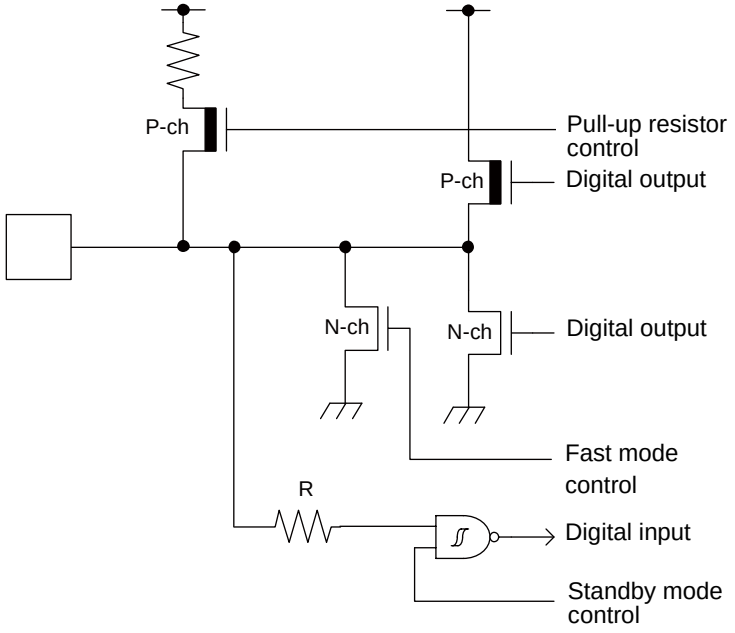
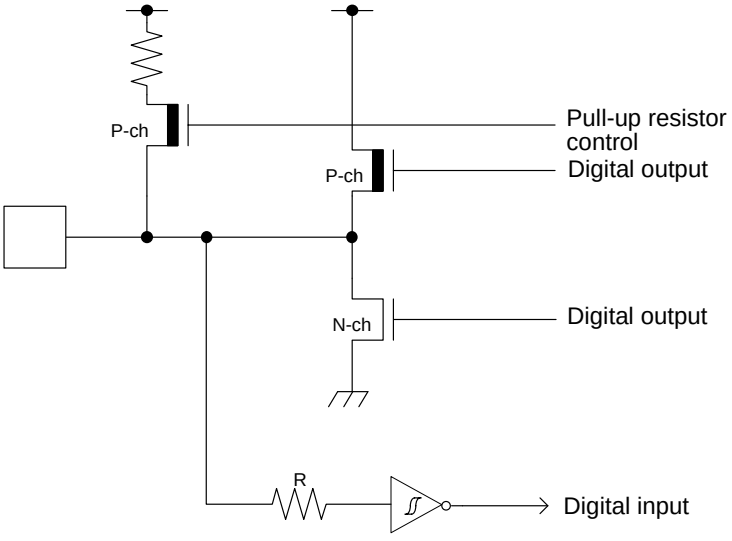
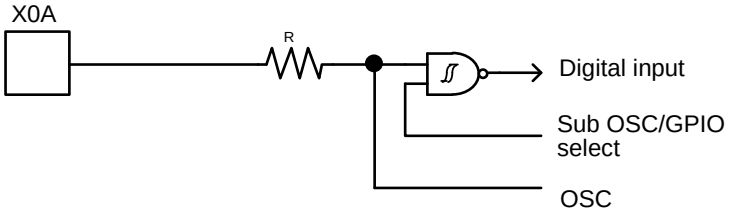
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	154
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2dh5j0agv2000a

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DH5GJA)	FBGA161			
125	87	87	D13	P95 AN21 SCK1_1 (SCL1_1) PNL_PD18 PNL_TSIG6 MAD19_0	F	L
126	–	–	–	PCA GE_SDA9	K	I
127	–	–	–	PCB GE_SDA8	K	I
128	–	–	–	PCC GE_SDA7	K	I
129	–	–	–	PCD GE_SDA6	K	I
130	88	88	C12	P96 AN22 PNL_PD17 PNL_TSIG5 MRASX_0	F	L
131	89	89	C13	P97 AN23 PNL_PD16 MCASX_0	F	L
132	90	90	B13	VSS	–	–
133	91	91	A12	VCC	–	–
134	–	–	–	PD0 GE_SDA5	K	I
135	–	–	–	PD1 GE_SDA4	K	I
136	–	–	–	PD2 GE_SDA3	K	I
137	–	–	–	PD3 GE_SDA2	K	I
138	–	–	–	PD4 GE_SDA1	K	I
139	92	92	B12	P00 TRSTX	E	G
140	93	93	A11	P01 TCK SWCLK	E	G

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DH5GJA)	FBGA161
I²S 0	I2SMCLK0_0	I²S ch.0 external clock pin	6	2	2	C3
	I2SDO0_0	I²S ch.0 serial transition data output pin	7	3	3	C2
	I2SWS0_0	I²S ch.0 frame synchronization signal pin	8	4	4	D3
	I2SDI0_0	I²S ch.0 serial received data input pin	9	5	5	D2
	I2SCK0_0	I²S ch.0 bit clock pin	10	6	6	D1
I²S 1	I2SMCLK1_0	I²S ch.1 external clock pin	51	33	33	M3
	I2SDO1_0	I²S ch.1 serial transition data output pin	52	34	34	L4
	I2SWS1_0	I²S ch.1 frame synchronization signal pin	53	35	35	M4
	I2SDI1_0	I²S ch.1 serial received data input pin	54	36	36	K5
	I2SCK1_0	I²S ch.1 bit clock pin	55	37	37	L5
GDC High-Speed Quad SPI	GE_SPCK	SPI clock output pin	34	20	-	J1
	GE_SPDQ0	SPI data input / output pin	35	21	-	K1
	GE_SPDQ1		38	24	-	J2
	GE_SPDQ2		39	25	-	J3
	GE_SPDQ3		36	22	-	H2
	GE_SPCSX0	SPI chip select output pin	37	23	-	H3
GDC HyperBus I/F	GE_HBCK	HBI clock output pin	34	20	-	J1
	GE_HBDQ0	HBI data input / output pin	36	22	-	H2
	GE_HBDQ1		37	23	-	H3
	GE_HBDQ2		38	24	-	J2
	GE_HBDQ3		39	25	-	J3
	GE_HBDQ4		40	26	-	K2
	GE_HBDQ5		41	27	-	K3
	GE_HBDQ6		42	28	-	L2
	GE_HBDQ7		43	29	-	L3
	GE_HBCSX0	HBI chip select output pin	35	21	-	K1
	GE_HBCSX1		12	8	-	E4
	GE_HBRWDS	HBI RWDS input / output pin	33	19	-	G2
	GE_HBRESETX	HBI hardware reset output pin	25	15	-	F3
	GE_HBINTX	HBI interrupt input pin	26	16	-	F2
	GE_HBRSTOX	HBI reset input pin	27	17	-	F1
	GE_HBWPX	HBI write protect output pin	28	18	-	G3

Type	Circuit	Remarks
N		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -3 mA, I_{OL} = 3 mA (GPIO) ・I_{OL} = 20 mA (Fast Mode Plus) ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
O		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・With pull-up resistor control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -2 mA, I_{OL} = 2 mA ・Available to control of PZR registers. ・Please refer to the "VBAT domain" setting of the IO in the “Peripheral Manual main part (002-04856)".
P		・CMOS level hysteresis input ・Please refer to the "VBAT domain" setting of the IO in the “Peripheral Manual main part (002-04856)".

7. Handling Devices

Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS, between AVCC and AVSS and between AVRH and AVRL near this device.

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/µs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

■Surface mount type

Size:	More than 3.2 mm × 1.5 mm
Load capacitance:	Approximately 6 pF to 7 pF When the Standard setting (CCS/CCB=11001110)
Load capacitance:	Approximately 4 pF to 7 pF When the low power setting (CCS/CCB=00000100)

■Lead type

Load capacitance:	Approximately 6 pF to 7 pF When the Standard setting (CCS/CCB=11001110)
Load capacitance:	Approximately 4 pF to 7 pF When the low power setting (CCS/CCB=00000100)

12.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	3.0	3.6	V	*1
				2.7 *5	3.6		*2
Power supply voltage (VBAT)		V_{BAT}	-	1.65	3.6	V	
Analog power supply voltage		AV_{CC}	-	2.7	3.6	V	$AV_{CC} = V_{CC}$
Analog reference voltage		AVRH	-	*4	AV_{CC}	V	
		AVRL	-	AVss	AVss	V	
Smoothing capacitor		C_S	-	1	10	µF	for built-in regulator *6
Operating temperature	Junction temperature	T_J	-	-40	+ 125	°C	
	Ambient temperature	T_A	-	-40	*3	°C	

*1: When using the GDC part .

When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0).

*2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80).

*3: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).
The calculation formula of the ambient temperature (T_A) is shown below.

$$T_A(Max) = T_J(Max) - Pd(Max) \times \theta_{JA}$$

Pd: Power dissipation (W)
θ_{JA}: Package thermal resistance (°C/W)

$$Pd\ (Max) = V_{CC} \times I_{CC}\ (Max) + \Sigma\ (I_{OL} \times V_{OL}) + \Sigma\ ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

*4: The minimum value of Analog reference voltage depends on the value of compare clock cycle (t_{CCK}). See 14.5 12-bit A/D Converter for the details.

*5: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

*6: See "C pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

12.4 AC Characteristics

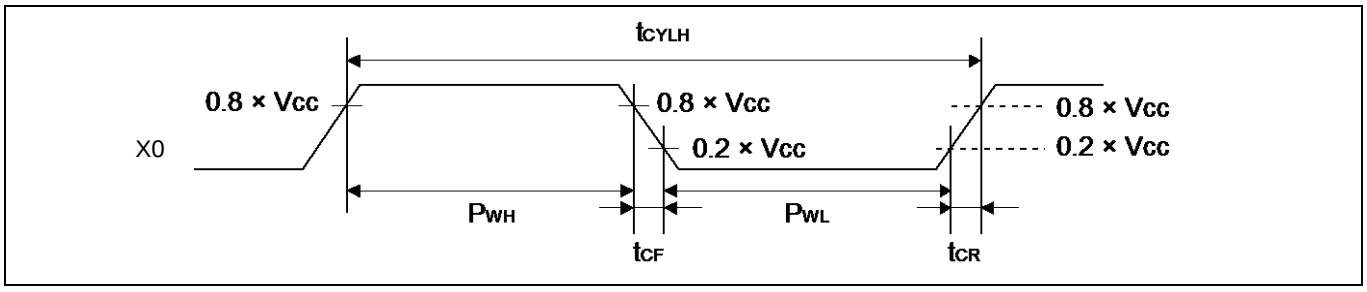
12.4.1 Main Clock Input Characteristics

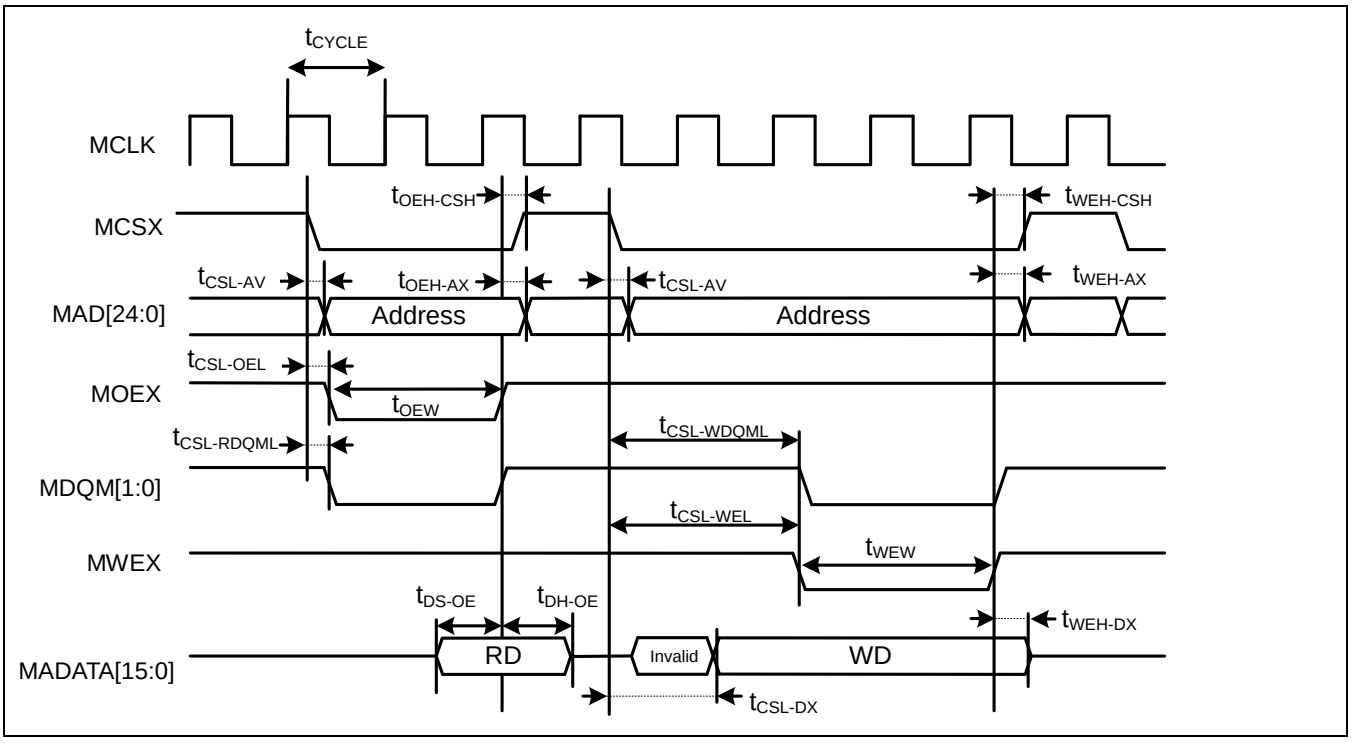
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	-	4	20	MHz	When crystal oscillator is connected
			-	4	20	MHz	When using external clock
Input clock cycle	t_{CYLH}		-	50	250	ns	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	f_{CM}	-	-	-	160	MHz	Master clock
	f_{CC}	-	-	-	160	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	80	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	160	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	80	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	10	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	5	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	10	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main part (002-04856).

*2: For about each APB bus which each peripheral is connected to, see Block Diagram in this data sheet.




tCYCLE
MCLK
MCSX
tOEH-CSH
tWEH-CSH
MAD[24:0]
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
MOEX
tCSL-OEL
tOEW
MDQM[1:0]
tCSL-RDQML
tCSL-WDQML
tCSL-WEL
MWEX
tWEW
MADATA[15:0]
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DX

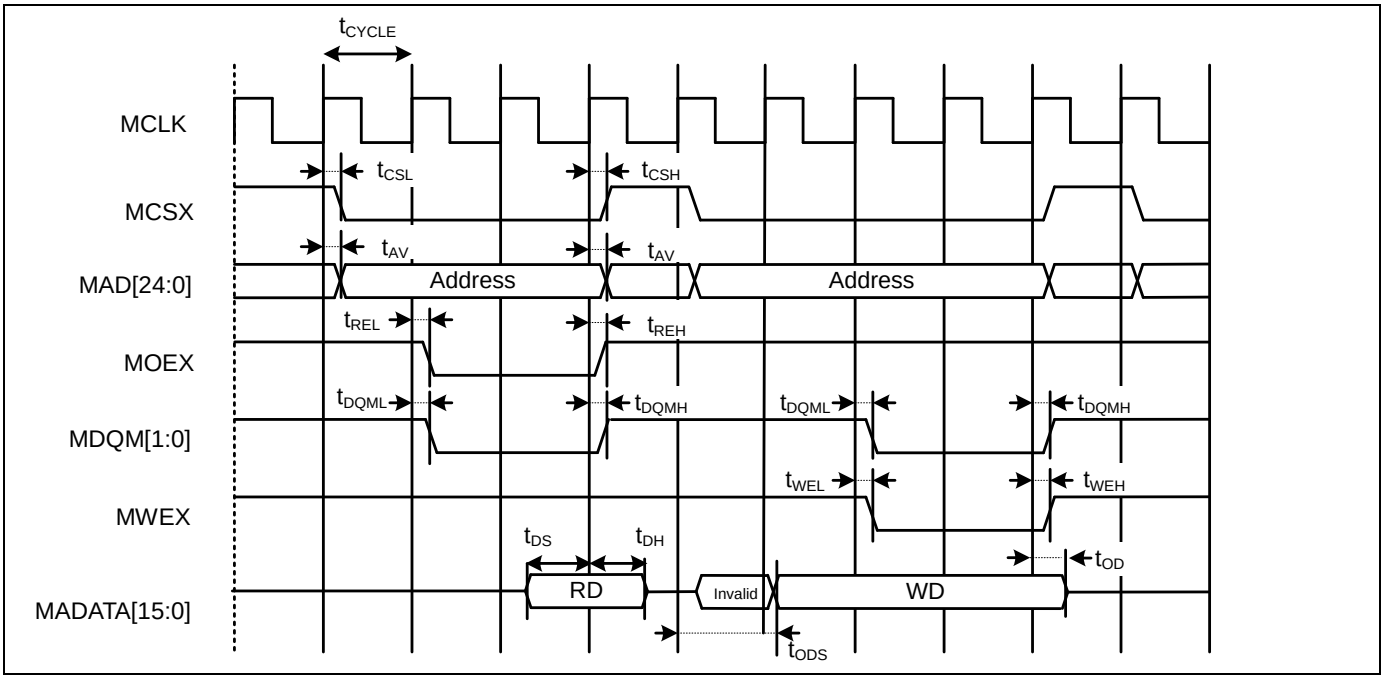
Separate Bus Access Synchronous SRAM Mode

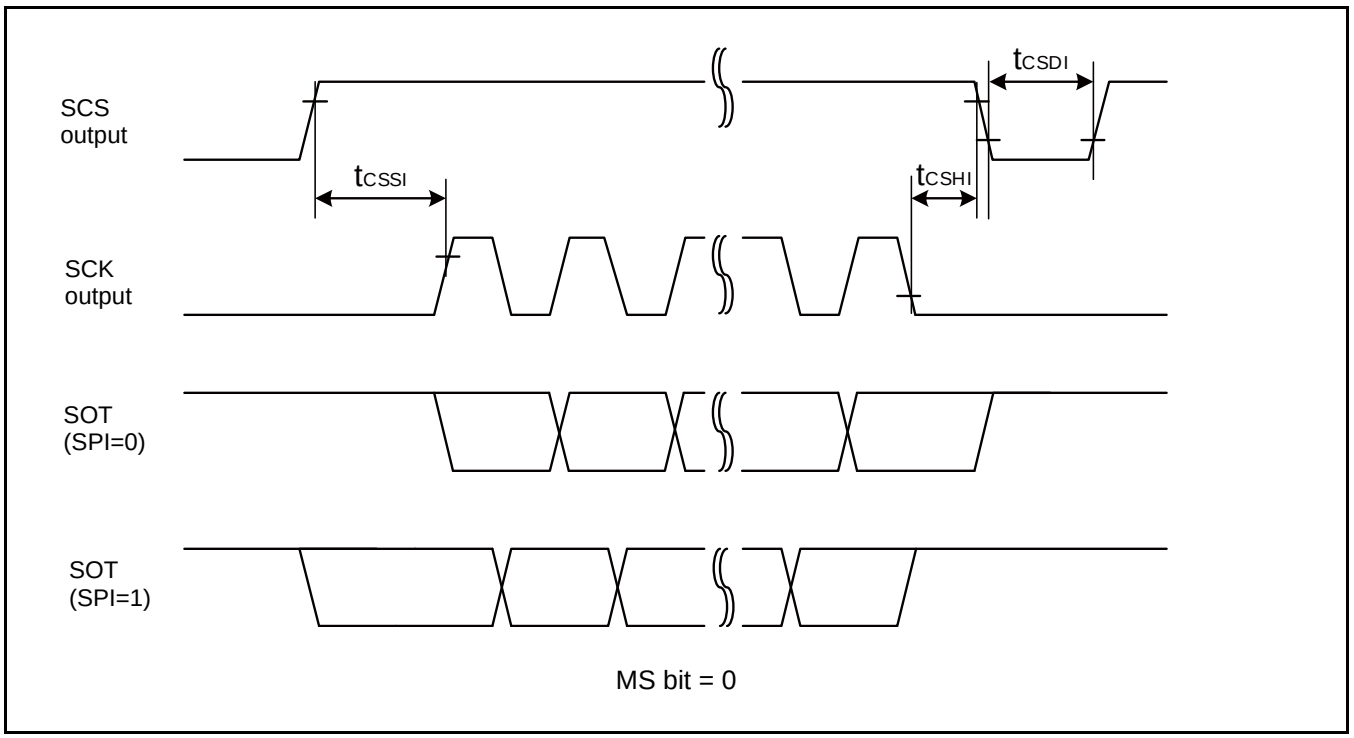
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24:0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up →MCLK ↑ time	t_{DS}	MCLK, MADATA[15:0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[15:0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[15:0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[15:0]	-	1	18	ns	

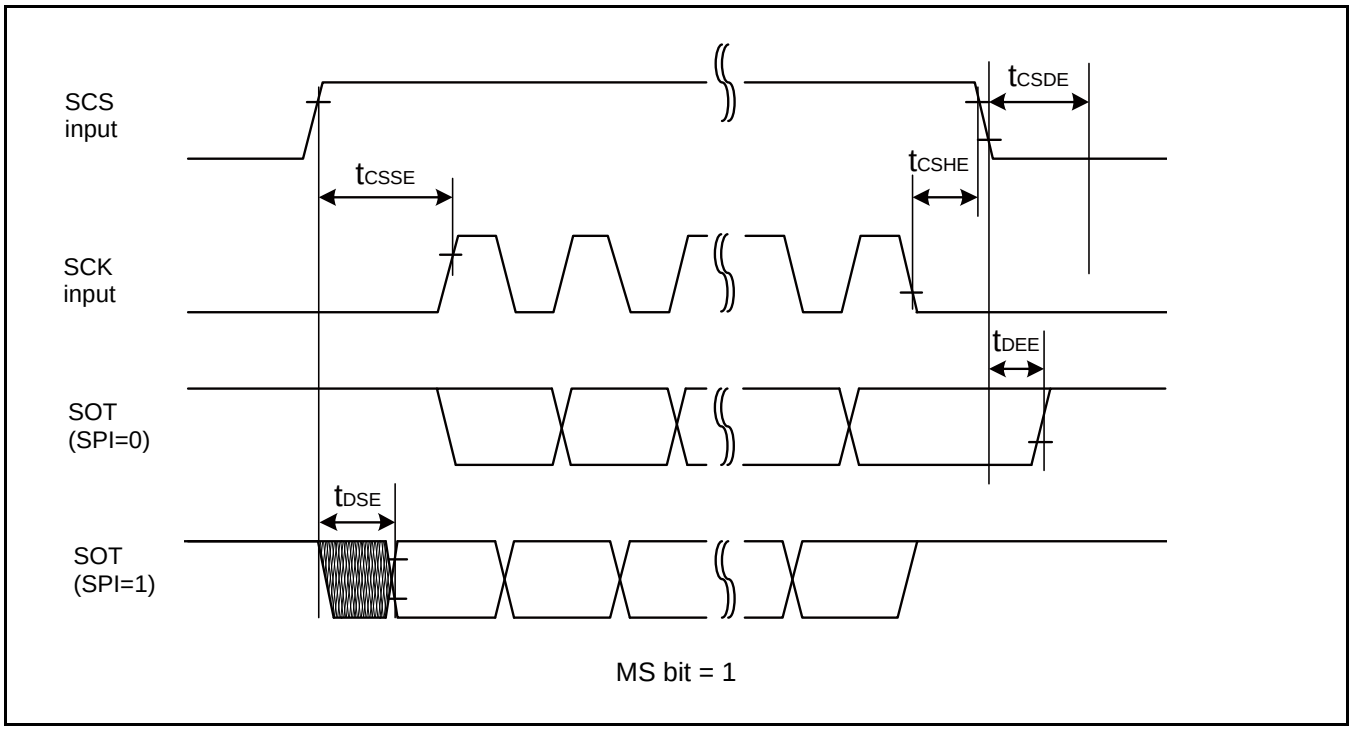
Note:

- *When the external load capacitance C_L = 30 pF*

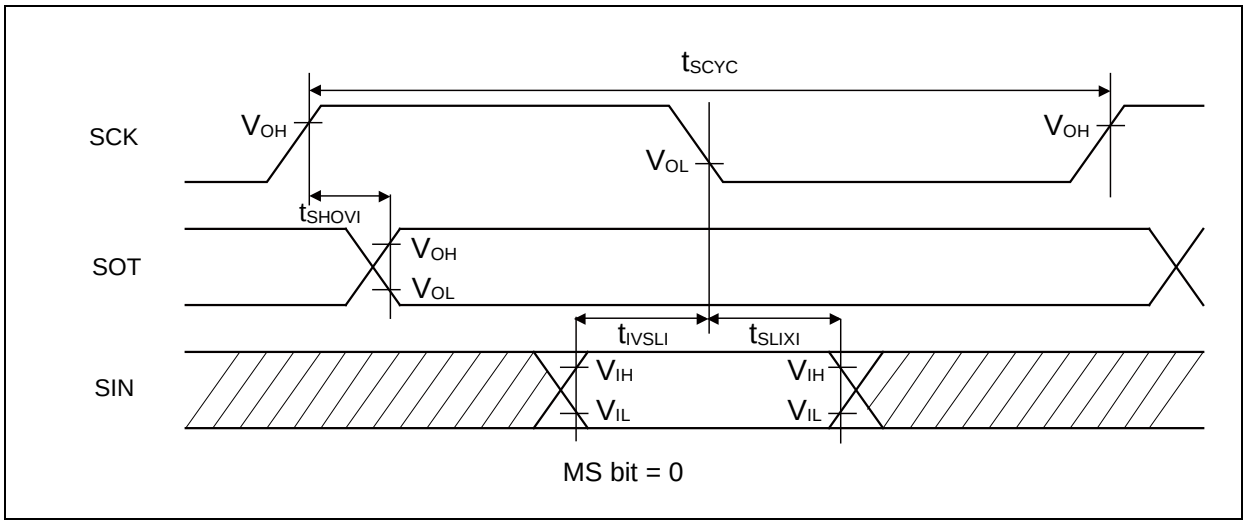




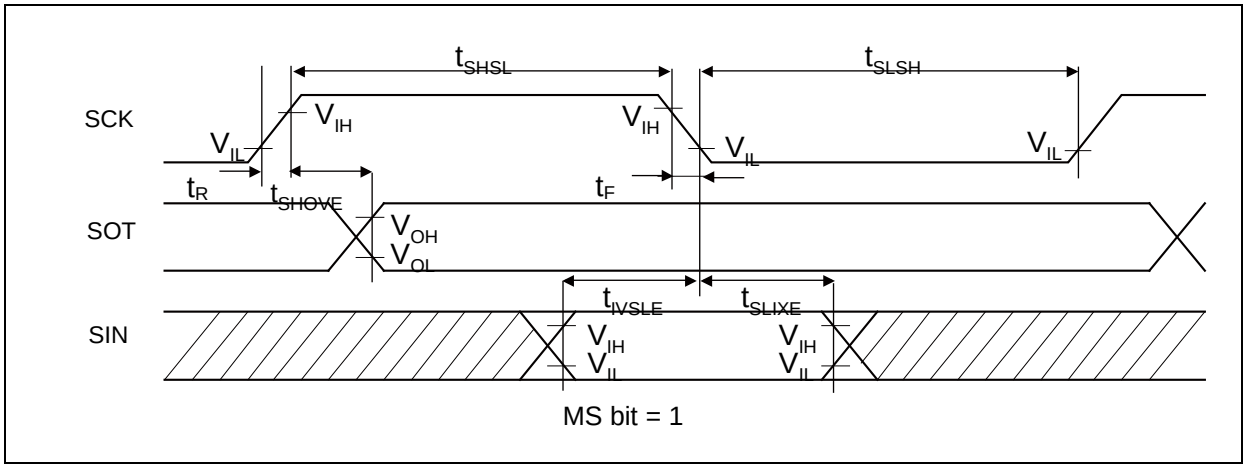
MS bit = 0



MS bit = 1



MS bit = 0



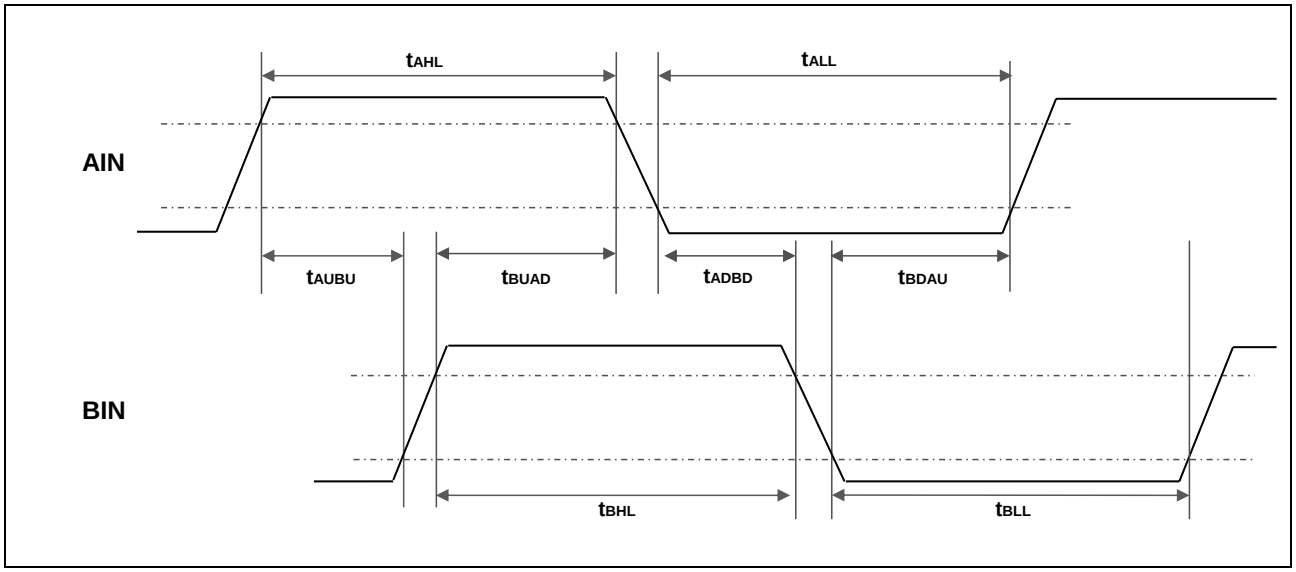
MS bit = 1

12.4.14 Quadrature Position/Revolution Counter Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC=0			
ZIN pin L width	t_{ZLL}	QCR:CGSC=0			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC=1			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC=1			

*: t_{CYCP} indicates the APB bus clock cycle time except when in Stop mode, in timer mode. About the APB bus number which Quadrature Position/Revolution Counter is connected to, see 8. Block Diagram in this data sheet.



High-Speed Mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1 card)	0	50	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rising time	t_{TLH}	S_CLK		-	3	ns
Clock falling time	t_{THL}	S_CLK		-	3	ns

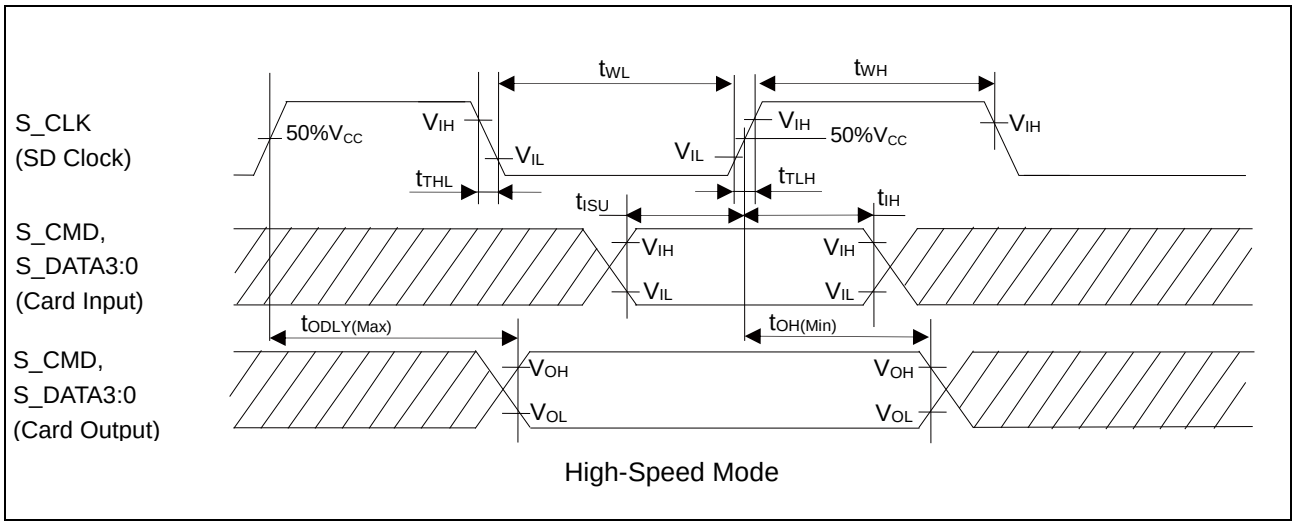
■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input setup time	t_{ISU}	S_CMD, S_DATA3:0	C_{CARD} ≤ 10 pF (1 card)	6	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3:0		2	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer Mode	t_{ODLY}	S_CMD, S_DATA3:0	C_L ≤ 40 pF (1 card)	0	14	ns
Output Hold time	t_{OH}	S_CMD, S_DATA3:0	C_L ≥ 15 pF (1 card)	2.5	-	ns
Total System capacitance for each line*	C_L	-	1 card	-	40	pF

*: In order to satisfy severe timing, host shall drive only one card.



High-Speed Mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *Please refer to: SD card interface Chapter 15 in FM4 Family Peripheral Manual Main part (002-04856) for Clock frequency (f_{PP}).*

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 3.6V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	-	± 4.5	LSB	AVRH=2.7 V to 3.6 V Offset calibration when used
Differential Nonlinearity	-	-	-	-	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 2	± 7	LSB	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 2	AVRH ± 7	LSB	
Total error	-	-	-	± 3	± 8	LSB	
Conversion time	-	-	1.0*1	-	-	µs	
Sampling time *2	t_S	-	0.3	-	10	µs	
Compare clock cycle*3	t_{CCK}	-	50	-	1000	ns	
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AV_{CC}	-	0.30	0.45	mA	A/D 1unit operation
			-	0.1	9.5	µA	When A/D stop
Reference power supply current(AVRH)	-	AVRH	-	0.66	1.18	mA	A/D 1unit operation AVRH=3.3 V
			-	0.2	3.2	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.8	kΩ	
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	t_{CCK} ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).

For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing.

For more information about the APB bus signal to which the A/D converter is connected, see 10. Block Diagram in this data sheet.

The sampling clock and compare clock are set at base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it set the sampling time to satisfy (Equation 1).

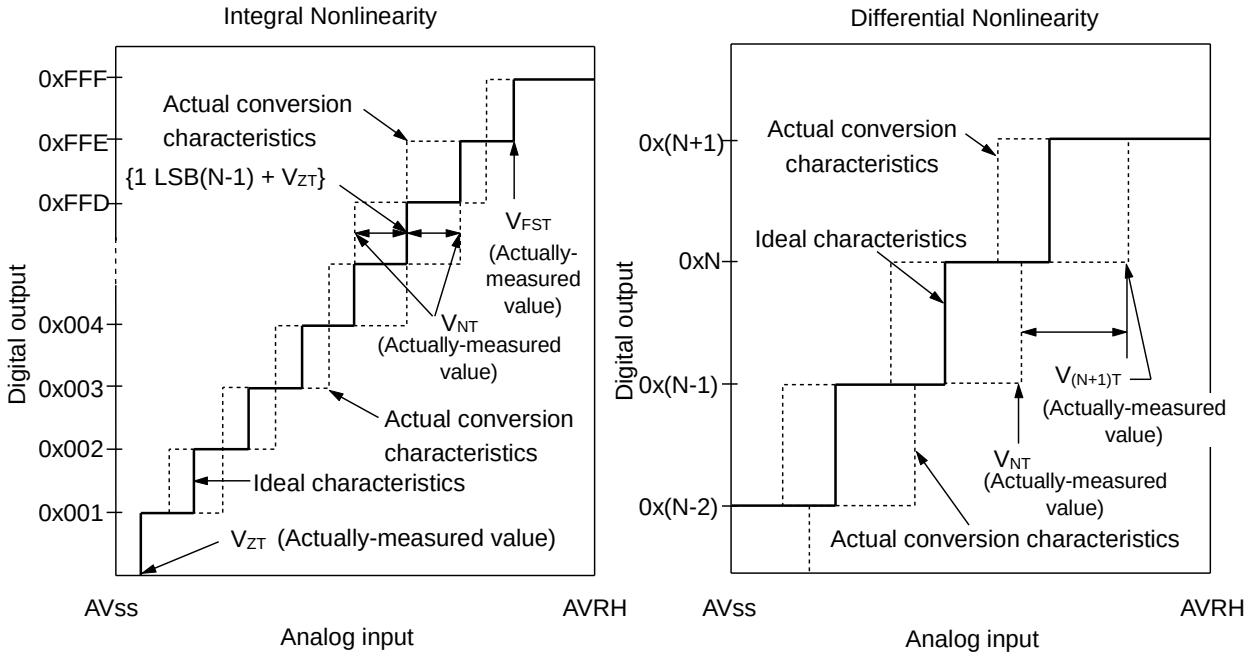
*3: The compare time (t_C) is the value of (Equation 2).

Definition of 12-bit A/D Converter Terms

■Resolution: Analog variation that is recognized by an A/D converter.

■Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.

■Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.

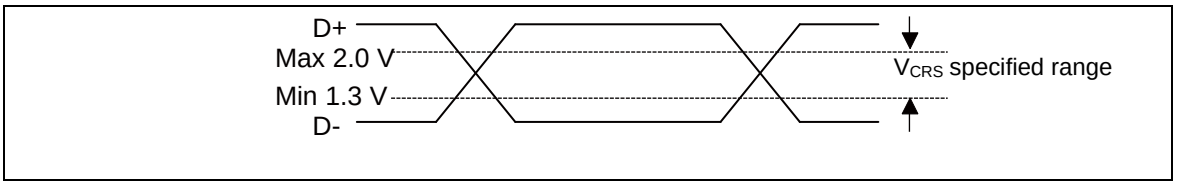


$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

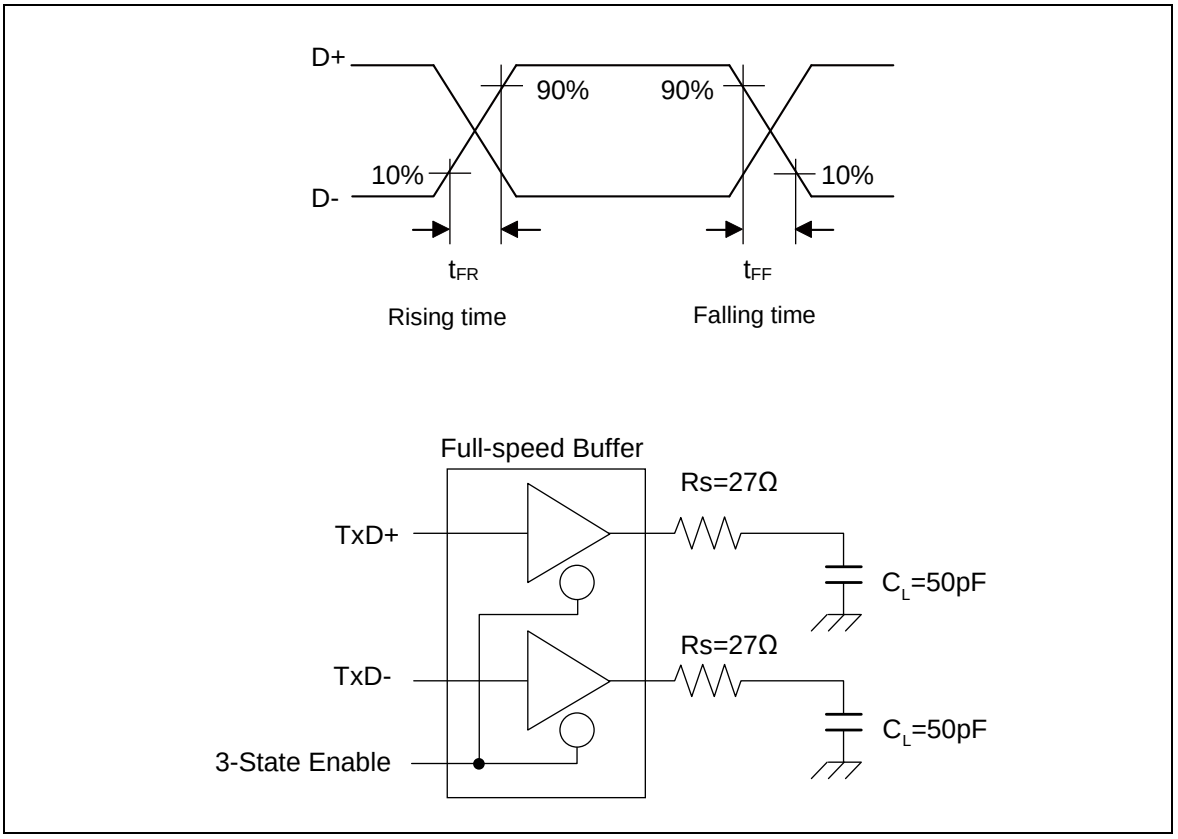
$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

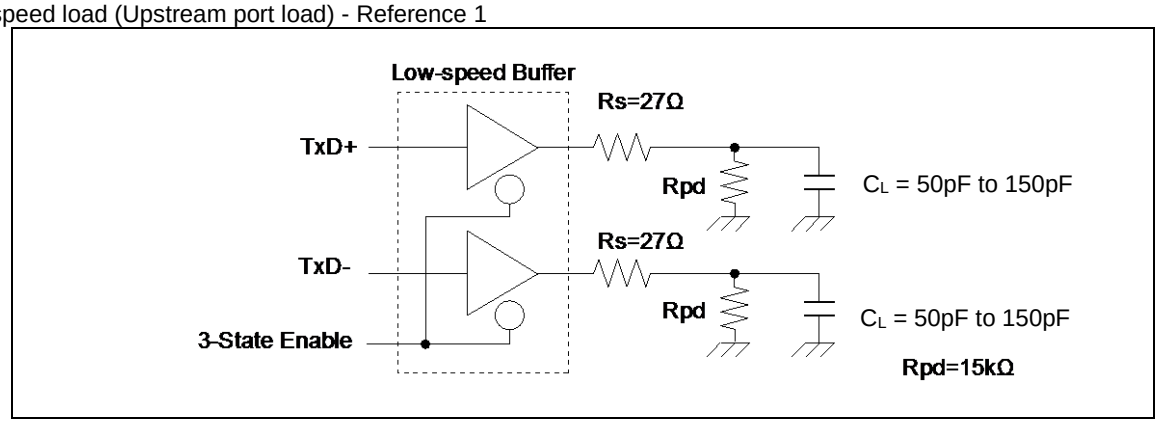
N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.



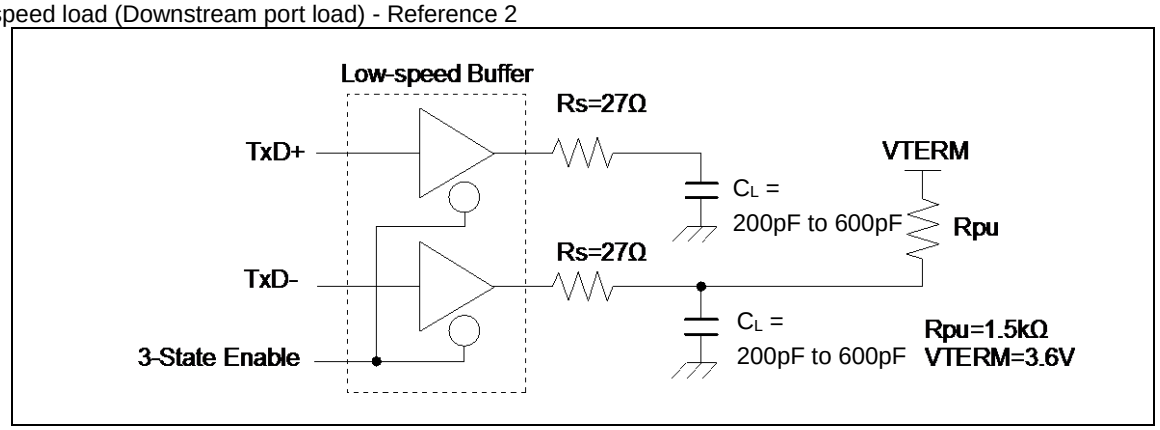
*5: They indicate Rising time (t_{FR}) and Falling time (t_{FF}) of the Full-speed differential data signal.
They are defined by the time between 10 % and 90 % of the output signal voltage.
For Full-speed buffer, t_{FR}/t_{FF} ratio is regulated as within ± 10 % to minimize RFI emission.



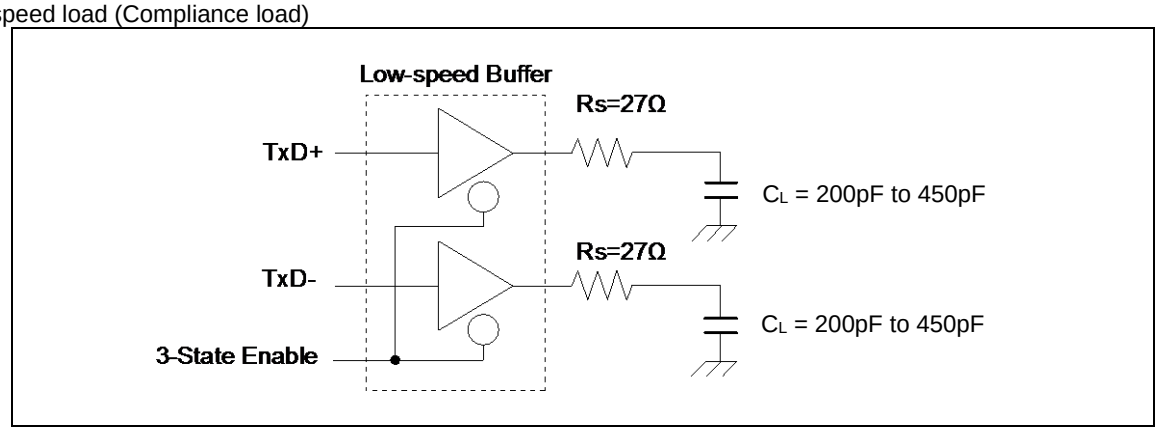
■Low-speed load (Upstream port load) - Reference 1



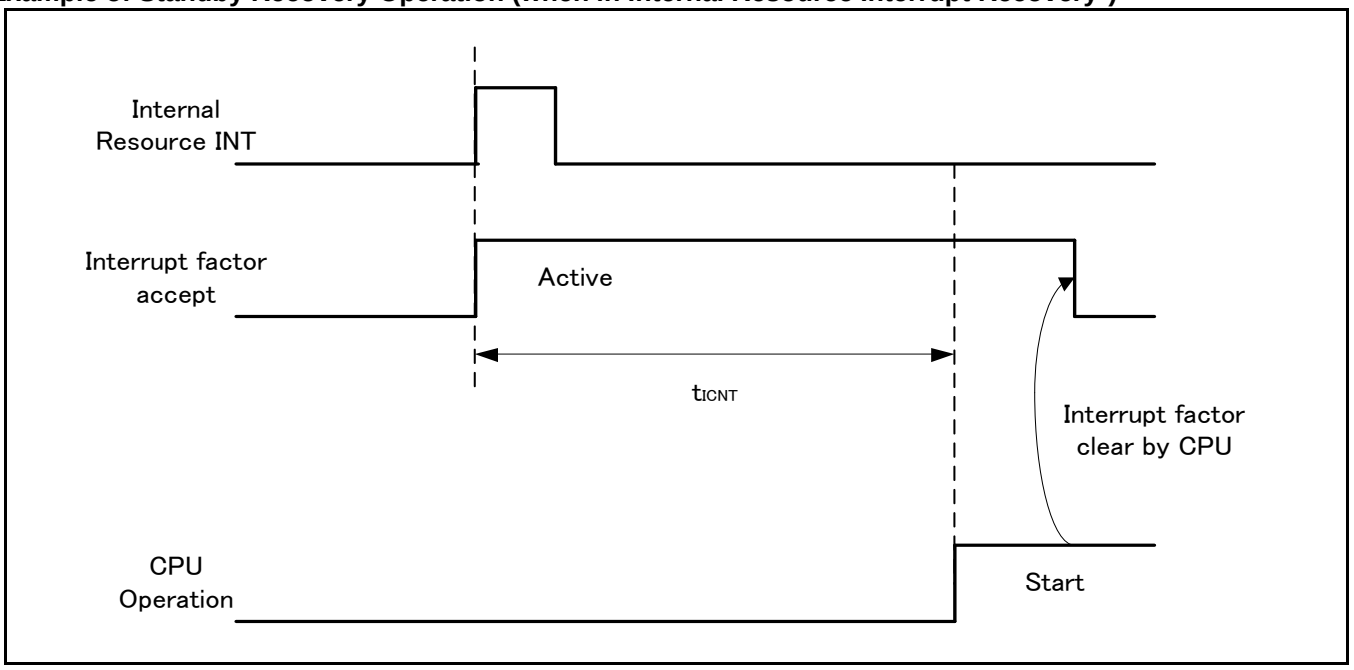
■Low-speed load (Downstream port load) - Reference 2



■Low-speed load (Compliance load)



Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery*)



*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See Chapter 6: The return factor from each low power consumption modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode" in "FM4 Family Peripheral Manual Main part (002-04856).*

12.10.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

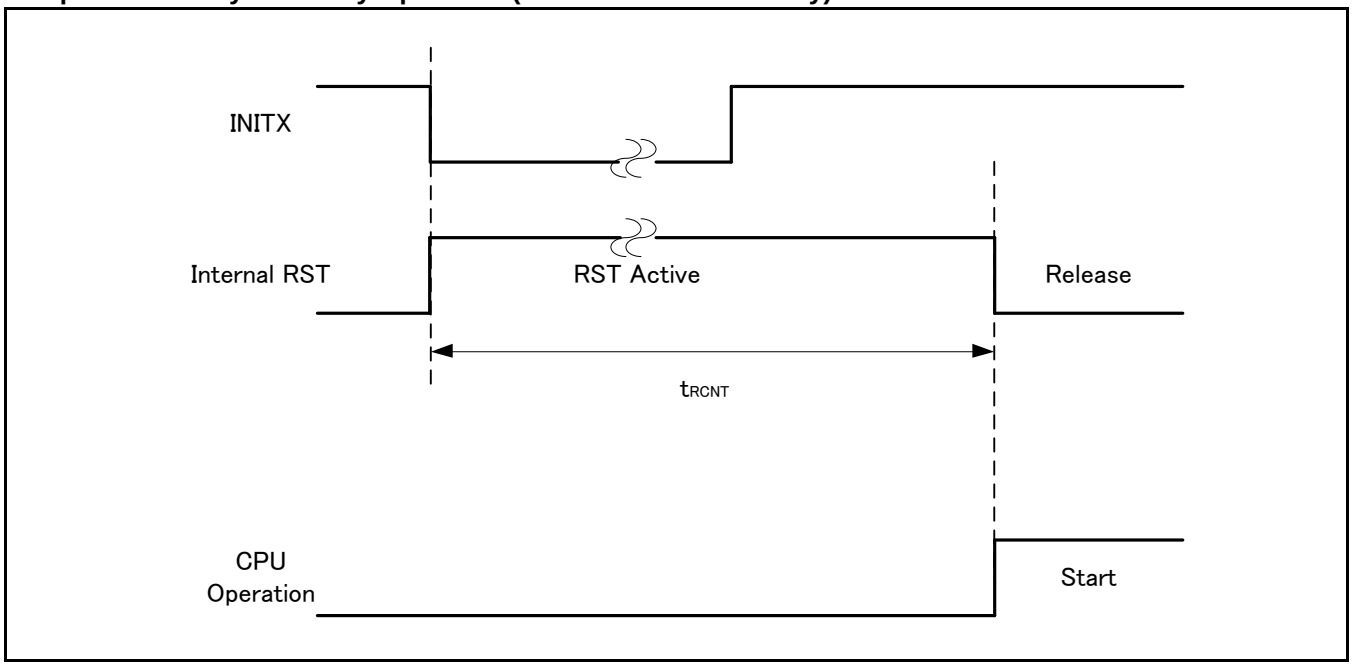
Recovery Count Time

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	µs	
Low-speed CR timer mode		315	567	µs	
Sub timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep standby RTC mode		336	667	µs	without RAM retention
Deep standby Stop mode		336	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)



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