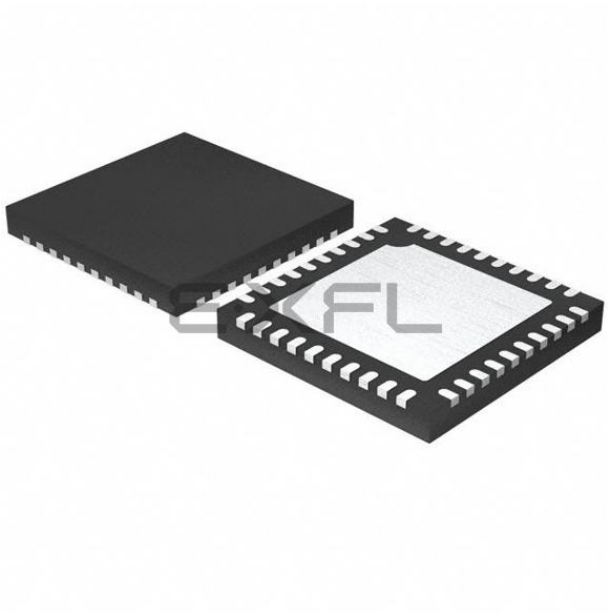


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (32KB)
Controller Series	-
RAM Size	4K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	34
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd1121-40lqxit

Contents

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the CCG1 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for CCG1 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The CCG1 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section Power on page 11. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). The CCG1 operates with a single external supply over the range of 3.2 V to 5.5 V operation and has three different power modes: Active, Sleep, and Deep Sleep; transitions between modes are managed by the power system.

Serial Communication Blocks (SCB)

The CCG1 has one SCB, which can implement an I^2C interface. The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZ-I^2C that creates a mailbox address range in the memory of the CCG1 and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices, as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

The CCG1 is not completely compliant with the I^2C spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8 mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I^2C Master, it interposes an IDLE state between NACK and Repeated Start; the I^2C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in the I^2C Slave mode, and Address Match on External Clock is enabled (EC_AM = 1) along with operation in the internally clocked mode (EC_OP = 0), then its I^2C address must be even.

GPIO

The CCG1 has up to 30 GPIOs, which are configured for various functions. Refer to the pinout tables for the definitions. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode).
- Selectable slew rates for dV/dt related noise control to improve EMI.

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network, known as a high-speed I/O matrix, is used to multiplex between various signals that may connect to an I/O pin.

Pin Definitions

Table 1 provides the pin definition for 35-Ball WLCSP for the Cable/EMCA application. Refer to Table 23 for part numbers to package mapping.

Table 1. Pin Definitions for 35-ball WLCSP for EMCA Cable Application

Functional Pin Name	CYPD1103-35FNXIT Balls	Type	Description
CC1_RX	C4	I	CC1 control 0: TX enabled z: RX sense
CC1_TX	D7	O	Configuration Channel 1
SWD_IO	D1	I/O	SWD I/O
SWD_CLK	C1	I	SWD clock
I2C_SCL	B1	I/O	I^2C clock signal
I2C_SDA	B2	I/O	I^2C data signal
XRES	B6	I	Reset
VCCD	A7	POWER	Regulated digital supply output. Connect a 1 to 1.6-µF capacitor. No external source should be connected
VDDD	C7	POWER	Power supply for both analog and digital sections
VSSA	B7	GND	Analog ground
CC_VREF	C5	I	Data reference signal for CC lines
TX_U	B3	O	Signals for internal use only. The TX_U output signal should be connected to the TX_M signal
TX_M	B5	I	–
TX_REF_IN	D3	I	Reference signal for internal use. Connect to TX_REF output via a 2.4K 1% resistor
TX_GND	A3	I	Connect to GND via 2K 1% resistor
TX_REF_OUT	D4	O	Reference signal generated by connecting internal current source to two 1K external resistors
RA_DISCONNECT	E4	O	Optional control signal to remove RA after assertion of VCONN 0: RA disconnected 1: RA connected
VCONN_DET	C6	I	Local VCONN detection signal 0: VCONN is not locally applied 1: VCONN is locally applied
CC1_LPREF	A5	I	Reference signal for internal use. Connect to the output of resistor divider from VDDD.
RA_FAR_DISCONNECT	E5	O	Optional control signal to remove RA after assertion of VCONN (NC for 2 chip/cable) 0: RA disconnected 1: RA connected
BYPASS	D5	I	Bypass capacitor for internal analog circuits
CC1_LPRX	C3	I	Configuration channel 1 RX signal for Low Power States
GPIO	A1, A2, A4, A6, B4, C2, D2, D6, E1, E2, E3, E6, E7	–	General-purpose I/Os

Table 2 provides the pin definitions for 40-pin QFN and 35-ball WLCSP for the notebook, tablet, smartphone, and monitor applications. Refer to Table 23 on page 23 for part numbers to package mapping.

Table 2. Pin Definitions for 40-QFN and 35-ball WLCSP for Notebook, Tablet, SmartPhone and Monitor Applications

Functional Pins	CYPD 1122-40LQXI Pins[8]	CYPD 1121-40LQXI Pins[9]	CYPD 1131-35FNXIT Balls[10]	Type	Description
MUXSEL_1	1	1	D5	O	External Data Mux Select signal 1
MUXSEL_2	2	2	D6	O	External Data Mux Select signal 2
CC1_CTRL	3	3	D3	I/O	CC1 control 0: TX enabled z: RX sense
CC2_CTRL	4	4	E4	I/O	CC2 control 0: TX enabled z: RX sense
MUXSEL_3	5	5	E5	O	External Data Mux Select signal 3
MUXSEL_4	6	6	E6	O	External Data Mux Select signal 4
CS_P	7	7	E3	I	Current Sensing Plus input
CS_M	8	8	E2	I	Current Sensing Minus input I
VSS	9	9	–	GND	Ground
CC1	10	10	-	I/O	Configuration Channel 1
CC_SEL_REF_1	11	11	E1	O	CC Reference Select signal
SWD_IO	12	12	D1	I/O	SWD IO
SWD_CLK	13	13	C1	I	SWD Clock
HOTPLUG_DET	14	14	C2	I/O	HotPlug Detection for Display Port Alternate Mode
GPIO1	15	–	–	I/O	General-purpose I/O
VSEL2	–	15	–	O	Voltage Select signal 2 for selecting output voltage
GPIO2	16	–	–	I/O	General-purpose I/O
GPIO3	17	–	–	I/O	General-purpose I/O
IFAULT	–	17	–	I	Current Fault Indication 0: No fault 1: Current fault
I2C_SCL	18	18	B1	I/O	I2C Clock signal
I2C_SDA	19	19	B2	I/O	I2C Data signal
I2C_INT	20	20	A2	O	I2C Interrupt
CC_SEL_REF_2	21	21	A1	O	CC Reference Select signal
CC1_RD	22	22	C3	O	Open Drain signal to connect RD to CC 1 line z: RD not connected 0: RD connected for Monitor application 1: RD connected for Notebook application
CC1_RP	23	23	A5	O	Open Source signal to connect RP to CC 1 line z: RP not connected 1: RP connected

Notes
8. Pinout for Notebook DRP application for 40-QFN.
9. Pinout for Monitor DRP application for 40-QFN.
10. Pinout for Notebook DRP application for 35-CSP.

Table 2. Pin Definitions for 40-QFN and 35-ball WLCSP for Notebook, Tablet, SmartPhone and Monitor Applications *(continued)*

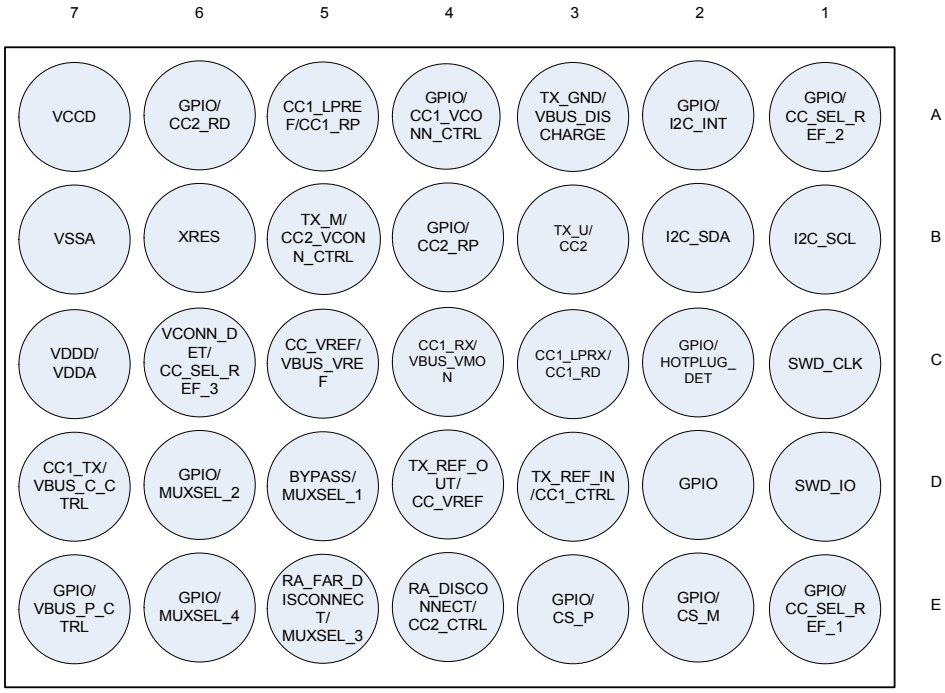
Functional Pins	CYPD 1122-40LQXI Pins[8]	CYPD 1121-40LQXI Pins[9]	CYPD 1131-35FNXIT Balls[10]	Type	Description
CC1_VCONN_CTRL	24	24	A4	O	Open Drain signal to control a PFET power switch for VCONN on CC 1 line 0: VCONN switch closed z: VCONN switch open
VBUS_DISCHARGE	25	25	A3	O	Signal used for discharging VBUS line during voltage change
CC2	26	26	B3	O	Configuration Channel 2
CC2_RD	27	27	A6	O	Open Drain signal to connect RD to CC 2 line z: RD not connected 0: RD connected for Monitor application 1: RD connected for Notebook application
CC2_RP	28	28	B4	O	Open Source signal to connect RP to CC 2 line z: RP not connected 1: RP connected
CC2_VCONN_CTRL	29	29	B5	O	Open Drain signal to control a PFET power switch for VCONN on CC 2 line 0: VCONN switch closed z: VCONN switch open
XRES	30	30	B6	I	Reset
VCCD	31	31	A7	POWER	Regulated digital supply output. Connect a 1 to 1.6-µF capacitor. No external source should be connected
VDDD	32	32	C7	POWER	Power supply for digital sections
VDDA	33	33	C7	POWER	Power Supply for analog sections
VSSA	34	34	B7	GND	Analog ground pin
VBUS_VMON	35	35	C4	I	VBUS Overvoltage Protection monitoring signal
VBUS_VREF	36	36	C5	I	VBUS reference signal for Overvoltage Protection detection
VSEL1	–	37	–	O	Voltage Select signal 1 for selecting the output voltage
CC_SEL_REF_3	37	16	C6	O	CC Reference Select signal
VBUS_C_CTRL	38	–	D7	O	Full rail control signal for enabling/disabling Consumer load FET
VBUS_OK	–	38	–		VBUS_OK=1 - VBUS Voltage ok VBUS_OK=0 - VBUS Overvoltage detected
CC_VREF	39	39	D4	I	Data reference signal for CC lines
VBUS_P_CTRL	40	40	E7	O	Full rail control signal for enabling/disabling Provider load FET

Notes
8. Pinout for Notebook DRP application for 40-QFN.
9. Pinout for Monitor DRP application for 40-QFN.
10. Pinout for Notebook DRP application for 35-CSP.

Table 3. Pin Definitions for 40-Pin QFN for Notebook (DFP) *(continued)*

Functional Pin Name	Active HIGH/ LOW	Drive Mode	CYPD 1134-40LQXI Pins	Type	Description
CC2_RP_3.0	Active HIGH	Open drain, drives high	21	O	Open Source signal to connect RP to CC2 line (3A current) z: RP not connected 1: RP connected
CC1_LPRX	–	Analog input	22	I	Configuration channel 1 RX signal for Low Power states
CC1_LPREF	–	Analog input	23	I	Reference signal for internal use.
CC2_LPRX	–	Analog input	24	I	Configuration channel 2 RX signal for Low Power states
CC2_LPREF	–	Analog input	25	I	Reference signal for internal use.
CC2	–	Strong drive (push pull)	26	O	Configuration Channel 2
CC1_VCONN_CTRL	Active LOW	Open drain, drives low	27	O	Open Drain signal to control a PFET power switch for VCONN on CC1 line 0: VCONN switch closed z: VCONN switch open
CC2_VCONN_CTRL	Active LOW	Open drain, drives low	28	O	Open Drain signal to control a PFET power switch for VCONN on CC2 line 0: VCONN switch closed z: VCONN switch open
IFAULT	Active HIGH	Digital input	29	I	Current Fault Indication on VBUS 0: No fault 1: Over Current fault
XRES	Active LOW	Analog input	30	I	Reset
VCCD	–	–	31	POWER	Connect 1uf Capacitor between VCCD and Ground
VDDD	–	–	32	POWER	5-V Supply
VDDA	–	–	33	POWER	5-V Supply
VSSA	–	–	34	GND	–
E-PAD	–	–	E-PAD	GND	–
VBUS_VMON	–	Analog input	35	I	VBUS Over-voltage Protection monitoring signal
VBUS_VREF	–	Analog input	36	I	VBUS reference signal for Over-voltage Protection detection
VBUS_P_CTRL	Active HIGH	Strong drive (Push Pull)	37	O	Full rail control signal for enabling/disabling Provider load FET
HOTPLUG_DET	Active HIGH	Open drain, drives low	38	IO	HotPlug Detection for Display Port Alternate Mode
CC_VREF/ VBUS_DISCHARGE	-/Active HIGH	Analog input/Strong drive (Push Pull)	39	IO	Data reference signal for CC lines / Signal used for discharging VBUS line during voltage change
MUXSEL_5	–	Open drain, drives low	40	O	External Data Mux Select signal 5

Figure 5. Pinout for CYPD1103-35FNXIT/CYPD1131-FNXIT



Power

The following power system diagram shows the minimum set of power supply pins as implemented for the CCG1. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the VDDA input. There is a separate regulator for the Deep Sleep mode. There is a separate low-noise regulator for the bandgap. The supply voltage range is 3.2 V to 5.5 V with all functions and circuits operating over that range.

VDDA and VDDD must be shorted together; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Refer to Application Diagrams for bypassing schemes.

I^2C

Table 12. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135.00	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310.00	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.40	µA	–

Table 13. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1.00	Mbps	–

Memory

Table 14. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	3.20	–	5.50	V	–

Table 15. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[13]	Row (block) write time (erase and program)	–	–	20.00	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[13]	Row erase time	–	–	13.00	ms	–
SID176	$T_{ROWPROGRAM}$[13]	Row program time after erase	–	–	7.00	ms	–
SID178	$T_{BULKERASE}$[13]	Bulk erase time (32 KB)	–	–	35.00	ms	–
SID180	$T_{DEVPROG}$[13]	Total device program time	–	–	7.00	seconds	Guaranteed by characterization
SID181	F_{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET}[14]	Flash retention. $T_A \le 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	–	Flash retention. $T_A \le 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	–	Flash retention. 85 °C < $T_A \le 105$ °C, 10K P/E cycles	3	–	–	years	Guaranteed by characterization

Notes

13. It can take as much as 20 milliseconds to write to flash. During this time the device should not be Reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
14. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customercare@cypress.com.

Internal Low-Speed Oscillator

Table 21. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.30	1.05	µA	Guaranteed by characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2.00	15.00	nA	Guaranteed by design

Table 22. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2.00	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40.00	50.00	60.00	%	Guaranteed by characterization
SID237	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15.00	32.00	50.00	kHz	±60% with trim

Applications in Detail

Figure 6. Single Chip/Cable, Component Count = 19

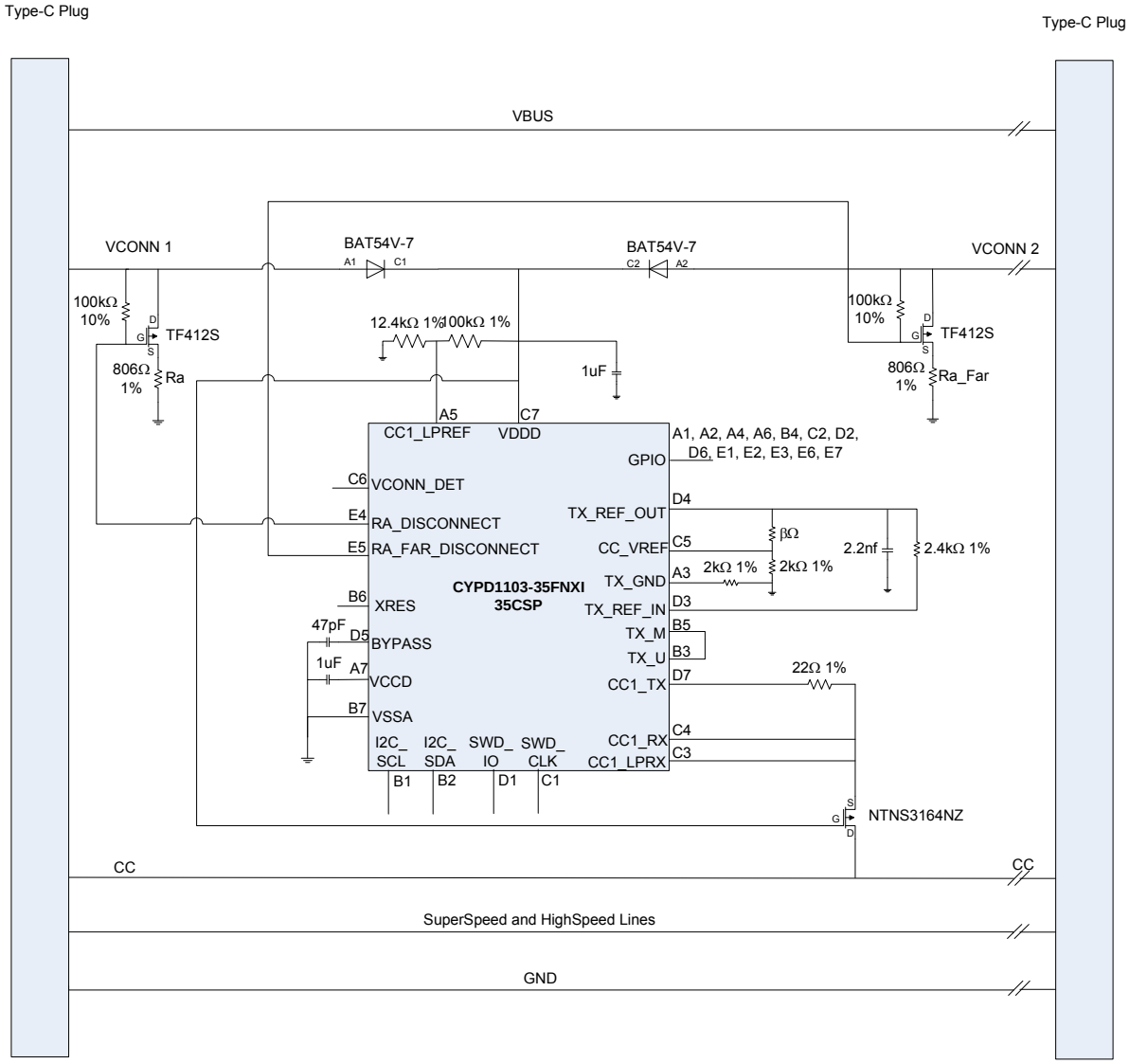


Figure 7. Two Chip/Cable, Component Count = 15/paddle

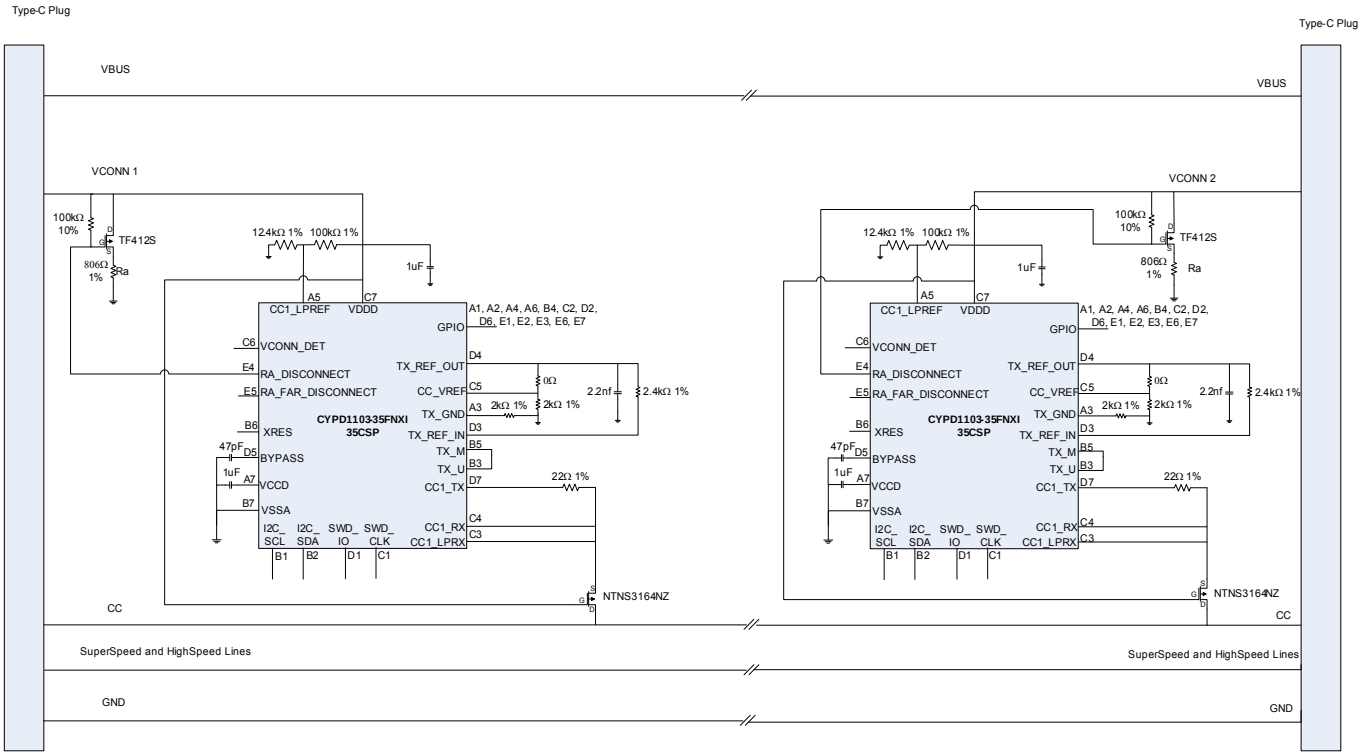


Figure 8. 16-pin SOIC Power Adapter Application Diagram

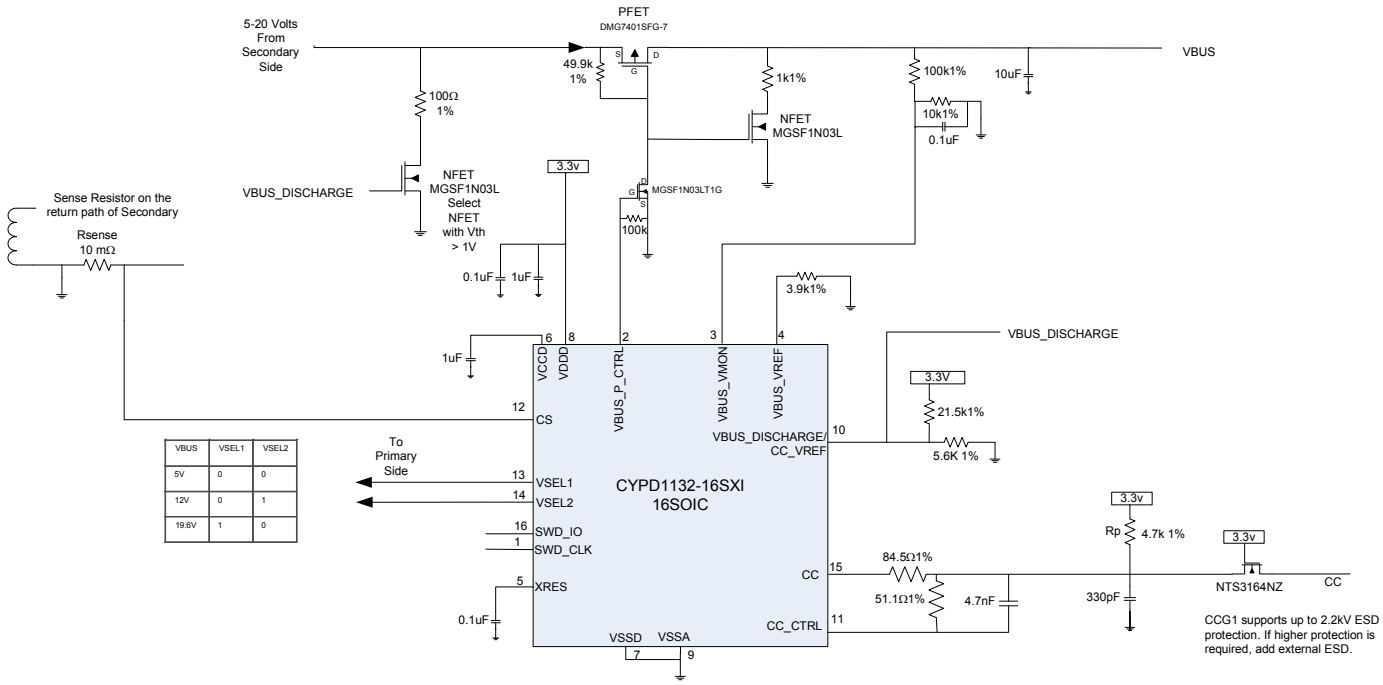


Figure 9. Notebook (DRP) Application Diagram

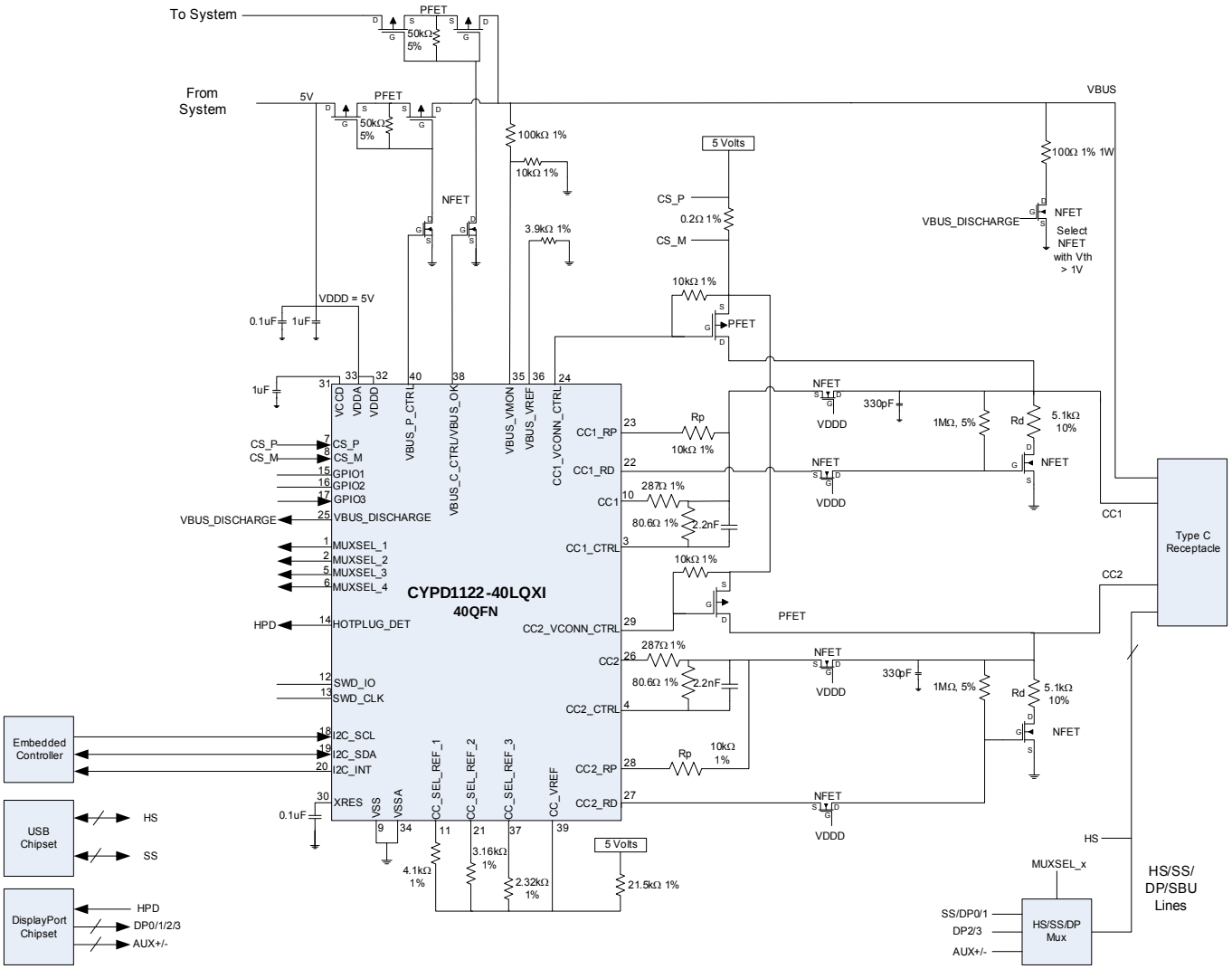


Figure 10. Notebook (DFP) Application Diagram

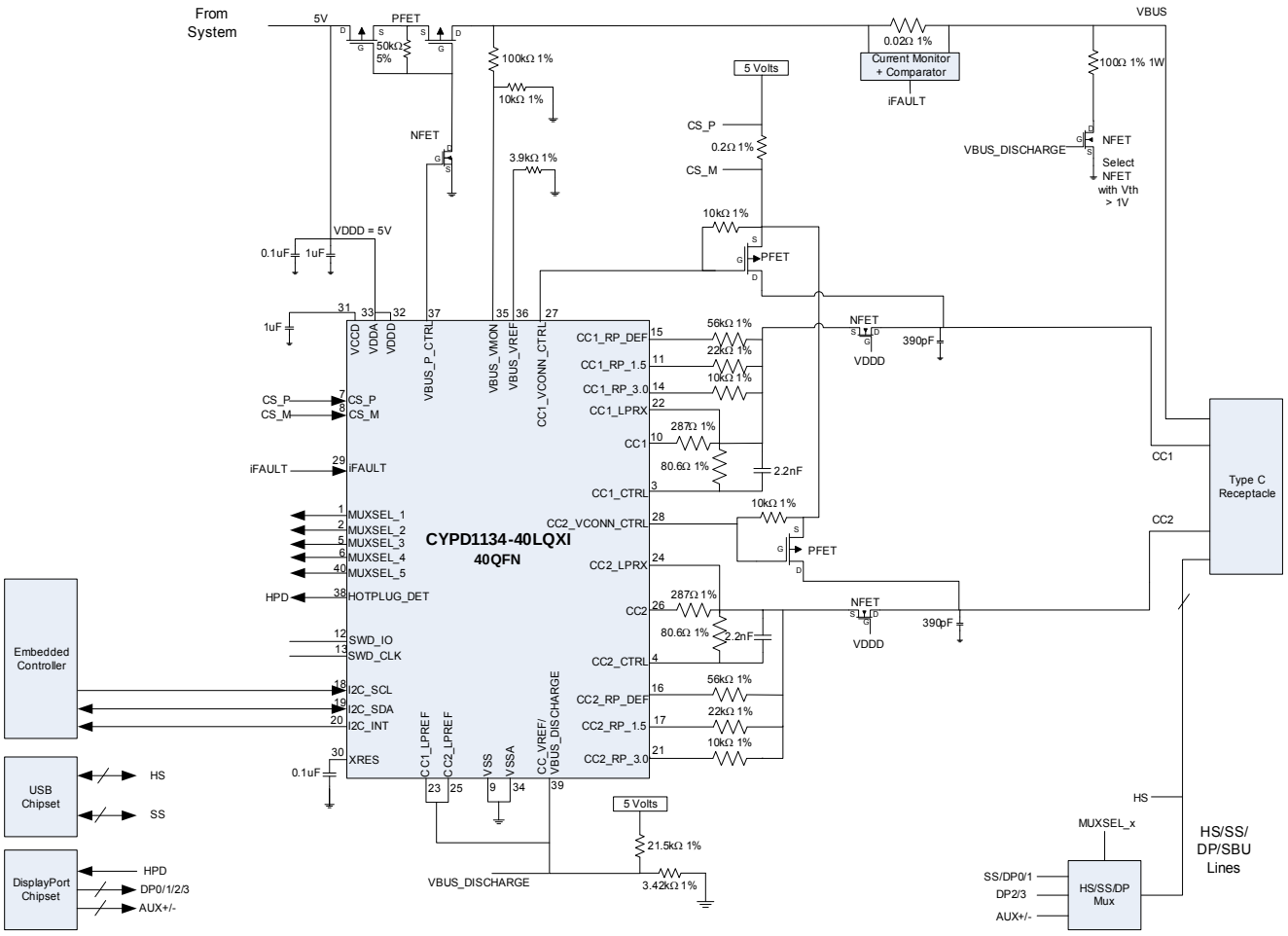
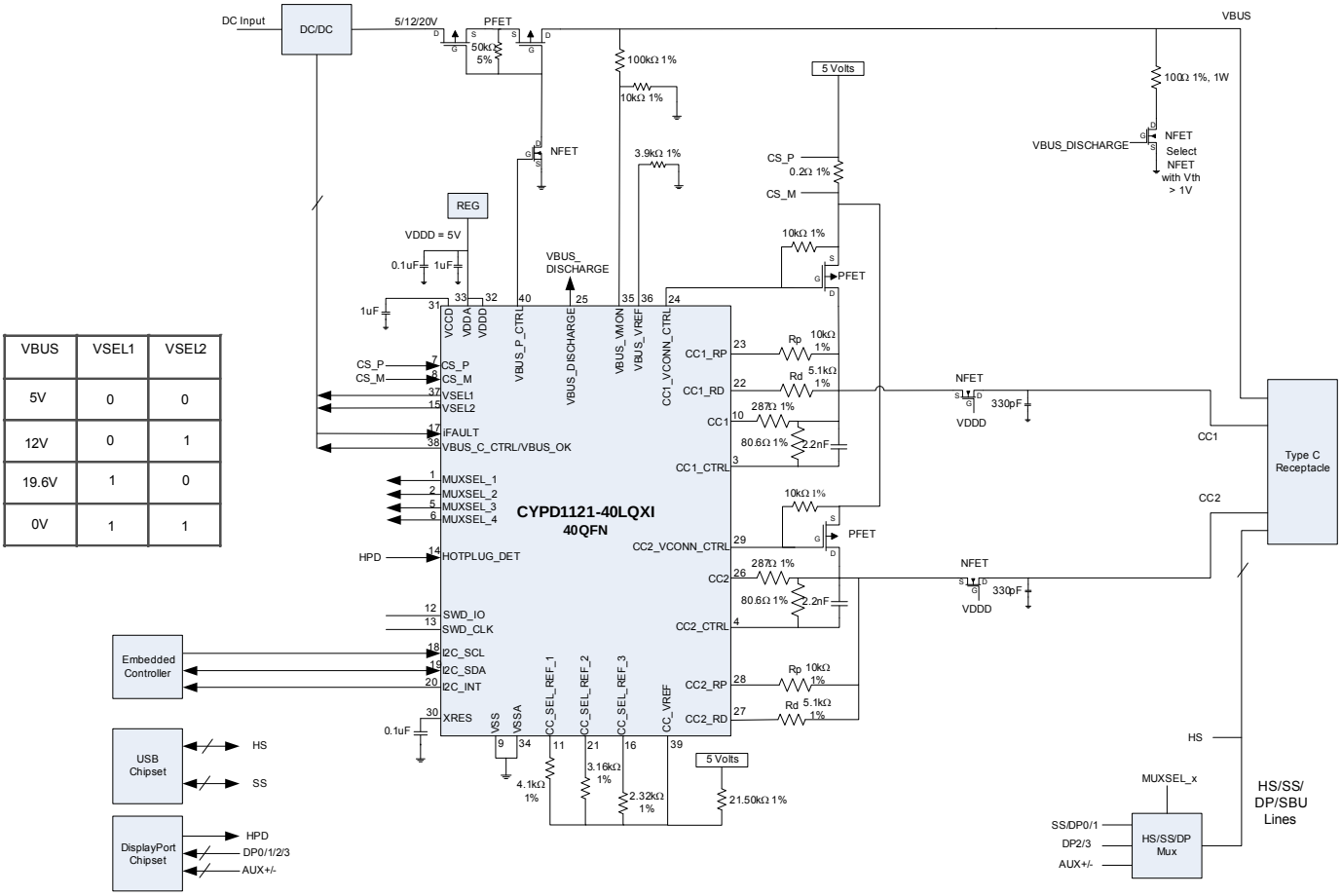


Figure 11. Monitor Application Block Diagram



VBUS	VSEL1	VSEL2
5V	0	0
12V	0	1
19.6V	1	0
0V	1	1

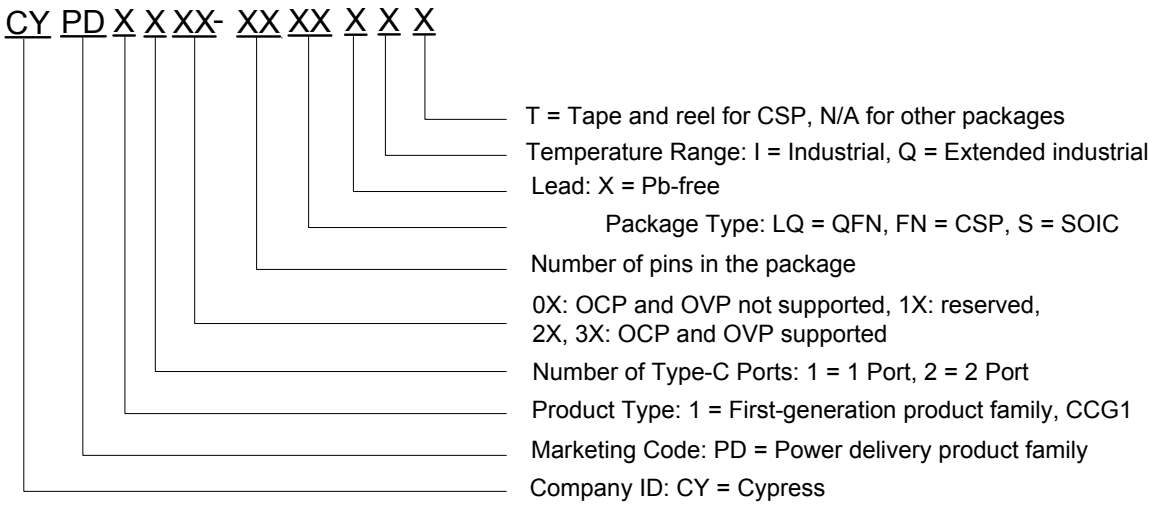
Ordering Information

The CCG1 part numbers and features are listed in the following table.

Table 23. CCG1 Ordering Information

Part Number[15]	Application	Type-C Ports[16]	Overcurrent Protection	Overvoltage Protection	Termination Resistor[17]	Role[18]	Package	Si ID
CYPD1103-35FNXIT	Cable, EMCA	1	No	No	R_a[19]	Cable	35-WLCSP[20]	0490
CYPD1131-35FNXIT	Notebook, Tablet, Smartphone	1	Yes	Yes	R_p[23], R_d[21]	DRP[24]	35-WLCSP[22]	0491
CYPD1121-40LQXI	Monitor	1	Yes	Yes	R_p[23], R_d[21]	DRP[24]	40-QFN	0489
CYPD1122-40LQXI	Notebook	1	Yes	Yes	R_p[23], R_d[21]	DRP[24]	40-QFN	048A
CYPD1134-40LQXI	Notebook, Desktop	1	Yes	Yes	R_p[23]	DFP	40-QFN	048B
CYPD1132-16SXI	Power Adapter	1	Yes	Yes	R_p[23]	DFP	16-SOIC	0498
CYPD1132-16SXQ	Power Adapter	1	Yes	Yes	R_p[23]	DFP	16-SOIC	0498

Ordering Code Definitions



Notes
15. All part numbers support: Input voltage range from 3.2 V to 5.5 V. Industrial parts support -40 °C to +85 °C, Extended Industrial parts support -40 °C to 105 °C.
16. Number of USB Type-C Ports supported .
17. Default V_{CONN} termination.
18. PD Role.
19. Type-C Cable Termination.
20. 35-WLCSP #1 pinout.
21. USB Device Termination.
22. 35-WLCSP #2 pinout.
23. USB Host Termination.
24. Dual Role Port.

Packaging

Table 24. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A (40-QFN, 35-CSP)	Operating ambient temperature	–	–40	25.00	85.00	°C
T_J (40-QFN, 35-CSP)	Operating junction temperature	–	–40	–	100.00	°C
T_A (16-SOIC)	Operating ambient temperature	–	–40	25.00	105.00	°C
T_J (16-SOIC)	Operating junction temperature	–	–40	–	120.00	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	15.34	–	°C/Watt
T_{JA}	Package θ_{JA} (35-CSP)	–	–	28.00	–	°C/Watt
T_{JA}	Package θ_{JA} (16-SOIC)	–	–	85.00	–	°C/Watt
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	02.50	–	°C/Watt
T_{JC}	Package θ_{JC} (35-CSP)	–	–	00.40	–	°C/Watt
T_{JC}	Package θ_{JC} (16-SOIC)	–	–	49.00	–	°C/Watt

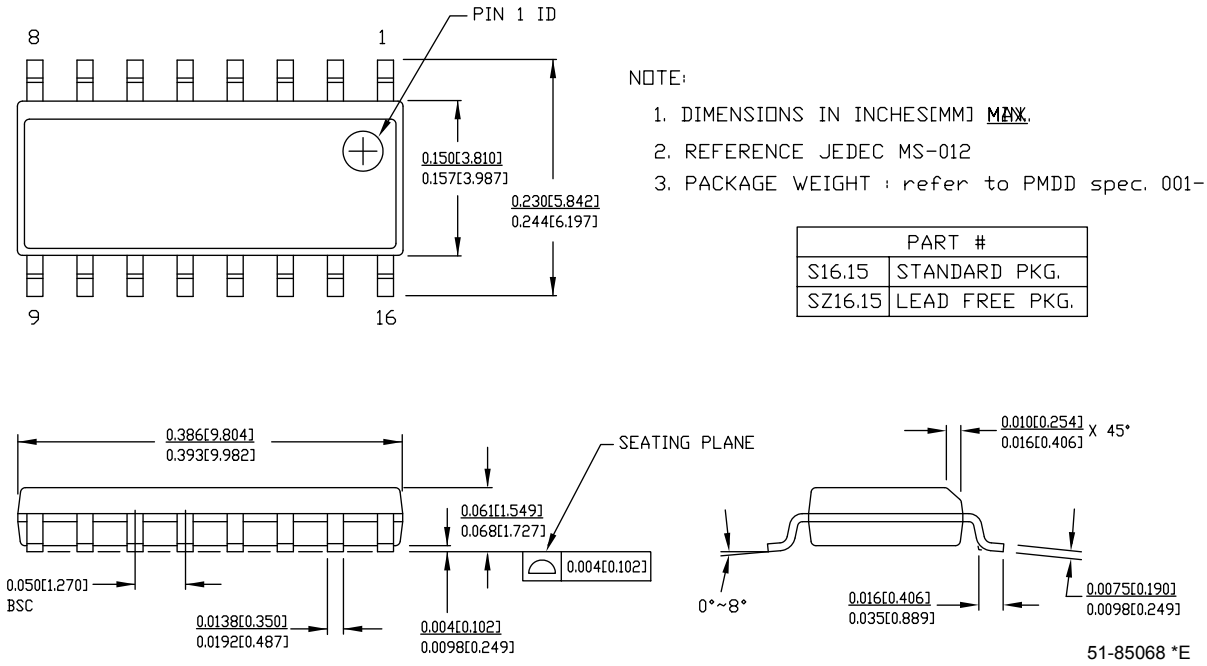
Table 25. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
16-pin SOIC	260 °C	30 seconds
40-pin QFN	260 °C	30 seconds
35-ball WLCSP	260 °C	30 seconds

Table 26. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
16-pin SOIC	MSL 3
40-pin QFN	MSL 3
35-ball WLCSP	MSL 1

Figure 14. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068



Acronyms

Table 27. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	Configuration Channel
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	Current Sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO, DIO, SIO, USBIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 27. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	Overcurrent protection
OVP	Overvoltage protection
PCB	printed circuit board
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UFP	upstream facing port
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 28. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision History *(continued)*

Description Title: CCG1 Datasheet USB Type-C Port Controller with Power Delivery Document Number: 001-93639				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G	4800534	VGT	07/02/2015	Updated Low-Power Operation. Updated the number of GPIOs to “up to 30” in GPIO. Updated “1.8 to 5.5 V” to “3.2 V to 5.5 V” in Low-Power Operation, Power System, Power, Device-Level Specifications and Note 15. Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 14 and Table 18. Added table footnotes 8, 9 and 10. Deleted footnotes 25 through 28. Updated Figure 2 and Figure 8 through Figure 11. Added Figure 3. Updated the following in Power: Removed Figures 5 through 8. Updated the section.
*H	4939764	VGT	09/29/2015	Removed specs SID241 and 242. Updated 40-pin QFN package to current revision.
*I	5179365	KISB	03/17/2016	Updated max value of I_{I2C1} from 10.50 µA to 50 µA. Updated copyright information and sales links at the end of the document.
*J	5459633	VGT	10/03/2016	Added compliance information regarding the USB Specification. Updated copyright notice to include WICED. Added IoT link in Sales, Solutions, and Legal Information.