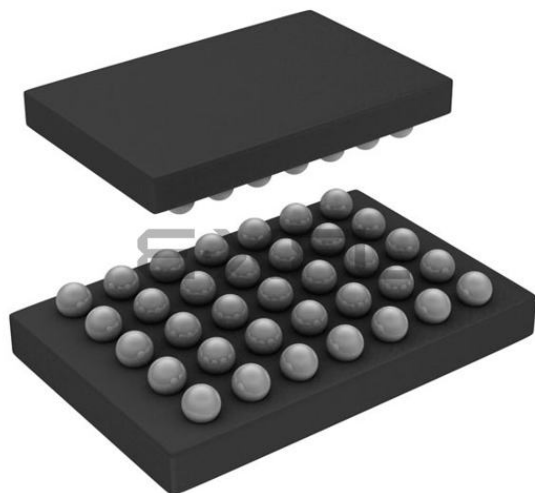




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Details

Product Status	Obsolete
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (32KB)
Controller Series	-
RAM Size	4K x 8
Interface	I ² C, SPI, UART/USART, USB
Number of I/O	31
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	35-UFBGA, WLCSP
Supplier Device Package	35-WLCSP (3.23x2.10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd1131-35fnxit

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Pin Definitions

Table 1 provides the pin definition for 35-Ball WLCSP for the Cable/EMCA application. Refer to Table 23 for part numbers to package mapping.

Table 1. Pin Definitions for 35-ball WLCSP for EMCA Cable Application

Functional Pin Name	CYPD1103-35FNXIT Balls	Type	Description
CC1_RX	C4	I	CC1 control 0: TX enabled z: RX sense
CC1_TX	D7	O	Configuration Channel 1
SWD_IO	D1	I/O	SWD I/O
SWD_CLK	C1	I	SWD clock
I2C_SCL	B1	I/O	I ² C clock signal
I2C_SDA	B2	I/O	I ² C data signal
XRES	B6	I	Reset
VCCD	A7	POWER	Regulated digital supply output. Connect a 1 to 1.6-μF capacitor. No external source should be connected
VDDD	C7	POWER	Power supply for both analog and digital sections
VSSA	B7	GND	Analog ground
CC_VREF	C5	I	Data reference signal for CC lines
TX_U	B3	O	Signals for internal use only. The TX_U output signal should be connected to the TX_M signal
TX_M	B5	I	—
TX_REF_IN	D3	I	Reference signal for internal use. Connect to TX_REF output via a 2.4K 1% resistor
TX_GND	A3	I	Connect to GND via 2K 1% resistor
TX_REF_OUT	D4	O	Reference signal generated by connecting internal current source to two 1K external resistors
RA_DISCONNECT	E4	O	Optional control signal to remove RA after assertion of VCONN 0: RA disconnected 1: RA connected
VCONN_DET	C6	I	Local VCONN detection signal 0: VCONN is not locally applied 1: VCONN is locally applied
CC1_LPREF	A5	I	Reference signal for internal use. Connect to the output of resistor divider from VDDD.
RA_FAR_DISCONNECT	E5	O	Optional control signal to remove RA after assertion of VCONN (NC for 2 chip/cable) 0: RA disconnected 1: RA connected
BYPASS	D5	I	Bypass capacitor for internal analog circuits
CC1_LPRX	C3	I	Configuration channel 1 RX signal for Low Power States
GPIO	A1, A2, A4, A6, B4, C2, D2, D6, E1, E2, E3, E6, E7	—	General-purpose I/Os

Table 2 provides the pin definitions for 40-pin QFN and 35-ball WLCSP for the notebook, tablet, smartphone, and monitor applications. Refer to Table 23 on page 23 for part numbers to package mapping.

Table 2. Pin Definitions for 40-QFN and 35-ball WLCSP for Notebook, Tablet, SmartPhone and Monitor Applications

Functional Pins	CYPD 1122-40LQXI Pins ^[8]	CYPD 1121-40LQXI Pins ^[9]	CYPD 1131-35FNXIT Balls ^[10]	Type	Description
MUXSEL_1	1	1	D5	O	External Data Mux Select signal 1
MUXSEL_2	2	2	D6	O	External Data Mux Select signal 2
CC1_CTRL	3	3	D3	I/O	CC1 control 0: TX enabled z: RX sense
CC2_CTRL	4	4	E4	I/O	CC2 control 0: TX enabled z: RX sense
MUXSEL_3	5	5	E5	O	External Data Mux Select signal 3
MUXSEL_4	6	6	E6	O	External Data Mux Select signal 4
CS_P	7	7	E3	I	Current Sensing Plus input
CS_M	8	8	E2	I	Current Sensing Minus input I
VSS	9	9	–	GND	Ground
CC1	10	10	–	I/O	Configuration Channel 1
CC_SEL_REF_1	11	11	E1	O	CC Reference Select signal
SWD_IO	12	12	D1	I/O	SWD IO
SWD_CLK	13	13	C1	I	SWD Clock
HOTPLUG_DET	14	14	C2	I/O	HotPlug Detection for Display Port Alternate Mode
GPIO1	15	–	–	I/O	General-purpose I/O
VSEL2	–	15	–	O	Voltage Select signal 2 for selecting output voltage
GPIO2	16	–	–	I/O	General-purpose I/O
GPIO3	17	–	–	I/O	General-purpose I/O
IFault	–	17	–	I	Current Fault Indication 0: No fault 1: Current fault
I2C_SCL	18	18	B1	I/O	I2C Clock signal
I2C_SDA	19	19	B2	I/O	I2C Data signal
I2C_INT	20	20	A2	O	I2C Interrupt
CC_SEL_REF_2	21	21	A1	O	CC Reference Select signal
CC1_RD	22	22	C3	O	Open Drain signal to connect RD to CC 1 line z: RD not connected 0: RD connected for Monitor application 1: RD connected for Notebook application
CC1_RP	23	23	A5	O	Open Source signal to connect RP to CC 1 line z: RP not connected 1: RP connected

Notes

8. Pinout for Notebook DRP application for 40-QFN.
9. Pinout for Monitor DRP application for 40-QFN.
10. Pinout for Notebook DRP application for 35-CSP.

Table 2. Pin Definitions for 40-QFN and 35-ball WLCSP for Notebook, Tablet, SmartPhone and Monitor Applications (continued)

Functional Pins	CYPD 1122-40L QXI Pins ^[8]	CYPD 1121-40L QXI Pins ^[9]	CYPD 1131-35FNXIT Balls ^[10]	Type	Description
CC1_VCONN_CTRL	24	24	A4	O	Open Drain signal to control a PFET power switch for VCONN on CC 1 line 0: VCONN switch closed z: VCONN switch open
VBUS_DISCHARGE	25	25	A3	O	Signal used for discharging VBUS line during voltage change
CC2	26	26	B3	O	Configuration Channel 2
CC2_RD	27	27	A6	O	Open Drain signal to connect RD to CC 2 line z: RD not connected 0: RD connected for Monitor application 1: RD connected for Notebook application
CC2_RP	28	28	B4	O	Open Source signal to connect RP to CC 2 line z: RP not connected 1: RP connected
CC2_VCONN_CTRL	29	29	B5	O	Open Drain signal to control a PFET power switch for VCONN on CC 2 line 0: VCONN switch closed z: VCONN switch open
XRES	30	30	B6	I	Reset
VCCD	31	31	A7	POWER	Regulated digital supply output. Connect a 1 to 1.6-μF capacitor. No external source should be connected
VDDD	32	32	C7	POWER	Power supply for digital sections
VDDA	33	33	C7	POWER	Power Supply for analog sections
VSSA	34	34	B7	GND	Analog ground pin
VBUS_VMON	35	35	C4	I	VBUS Overvoltage Protection monitoring signal
VBUS_VREF	36	36	C5	I	VBUS reference signal for Overvoltage Protection detection
VSEL1	–	37	–	O	Voltage Select signal 1 for selecting the output voltage
CC_SEL_REF_3	37	16	C6	O	CC Reference Select signal
VBUS_C_CTRL	38	–	D7	O	Full rail control signal for enabling/disabling Consumer load FET
VBUS_OK	–	38	–		VBUS_OK=1 - VBUS Voltage ok VBUS_OK=0 - VBUS Overvoltage detected
CC_VREF	39	39	D4	I	Data reference signal for CC lines
VBUS_P_CTRL	40	40	E7	O	Full rail control signal for enabling/disabling Provider load FET

Notes

8. Pinout for Notebook DRP application for 40-QFN.
9. Pinout for Monitor DRP application for 40-QFN.
10. Pinout for Notebook DRP application for 35-CSP.

Table 3. Pin Definitions for 40-Pin QFN for Notebook (DFP) (continued)

Functional Pin Name	Active HIGH/LOW	Drive Mode	CYPD 1134-40LQXI Pins	Type	Description
CC2_RP_3.0	Active HIGH	Open drain, drives high	21	O	Open Source signal to connect RP to CC2 line (3A current) z: RP not connected 1: RP connected
CC1_LPRX	–	Analog input	22	I	Configuration channel 1 RX signal for Low Power states
CC1_LPREF	–	Analog input	23	I	Reference signal for internal use.
CC2_LPRX	–	Analog input	24	I	Configuration channel 2 RX signal for Low Power states
CC2_LPREF	–	Analog input	25	I	Reference signal for internal use.
CC2	–	Strong drive (push pull)	26	O	Configuration Channel 2
CC1_VCONN_CTRL	Active LOW	Open drain, drives low	27	O	Open Drain signal to control a PFET power switch for VCONN on CC1 line 0: VCONN switch closed z: VCONN switch open
CC2_VCONN_CTRL	Active LOW	Open drain, drives low	28	O	Open Drain signal to control a PFET power switch for VCONN on CC2 line 0: VCONN switch closed z: VCONN switch open
IFault	Active HIGH	Digital input	29	I	Current Fault Indication on VBUS 0: No fault 1: Over Current fault
XRES	Active LOW	Analog input	30	I	Reset
VCCD	–	–	31	POWER	Connect 1uf Capacitor between VCCD and Ground
VDDD	–	–	32	POWER	5-V Supply
VDDA	–	–	33	POWER	5-V Supply
VSSA	–	–	34	GND	–
E-PAD	–	–	E-PAD	GND	–
VBUS_VMON	–	Analog input	35	I	VBUS Over-voltage Protection monitoring signal
VBUS_VREF	–	Analog input	36	I	VBUS reference signal for Over-voltage Protection detection
VBUS_P_CTRL	Active HIGH	Strong drive (Push Pull)	37	O	Full rail control signal for enabling/disabling Provider load FET
HOTPLUG_DET	Active HIGH	Open drain, drives low	38	IO	HotPlug Detection for Display Port Alternate Mode
CC_VREF/ VBUS_DISCHARGE	-/Active HIGH	Analog input/Strong drive (Push Pull)	39	IO	Data reference signal for CC lines / Signal used for discharging VBUS line during voltage change
MUXSEL_5	–	Open drain, drives low	40	O	External Data Mux Select signal 5

Table 4 provides the pin definition for 16-pin SOIC for the Power Adapter application. Refer to Table 23 on page 23 for part numbers to package mapping.

Table 4. Pin Definitions for 16-pin SOIC for Power Adapter Application

Functional Pin Name	CYPD 1132-16SXI Pins	Type	Description
SWD_CLK	1	I	SWD Clock
VBUS_P_CTRL	2	O	Full rail control signal for enabling/disabling provider load FET
VBUS_VMON	3	I	VBUS over-voltage protection monitoring signal
VBUS_VREF	4	I	VBUS reference signal for over-voltage protection detection
XRES	5	–	Active Low Reset
VCCD	6	–	Connect 1 μ F capacitor between VCCD and GROUND
VSSD	7	–	Ground
VDDD	8	–	Power 3.3 V/5 V
VSSA	9	–	Ground
CC_VREF/VBUS_DISCHARGE	10	I/O	Data reference signal for CC line (0.55 Volt) / Signal used for discharging VBUS line during voltage decrease
CC_CTRL	11	I/O	CC1 control 0: TX enabled z: RX sense
CS	12	I	Low Side Current Sense
VSEL1	13	O	Voltage select signal for selecting the output voltage 5/12/20 V
VSEL2	14	O	Voltage select signal for selecting the output voltage 5/12/20 V
CC	15	I/O	Configuration Channel TX/RX
SWD_IO	16	I/O	SWD I/O

Pinouts

Figure 2. Pinout for CYPD1122-40LQXI/CYPD1121-40LQXI

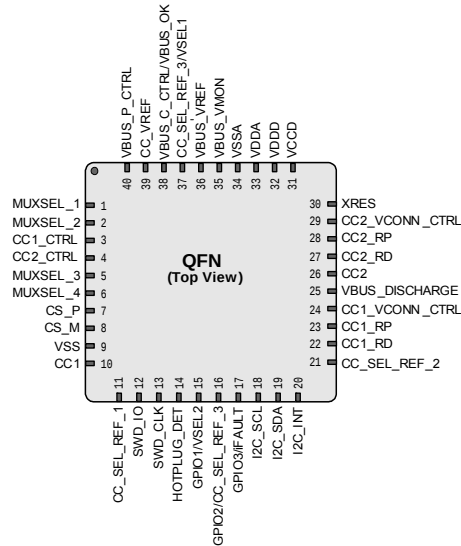


Figure 3. Pinout for CYPD1134-40LQXI

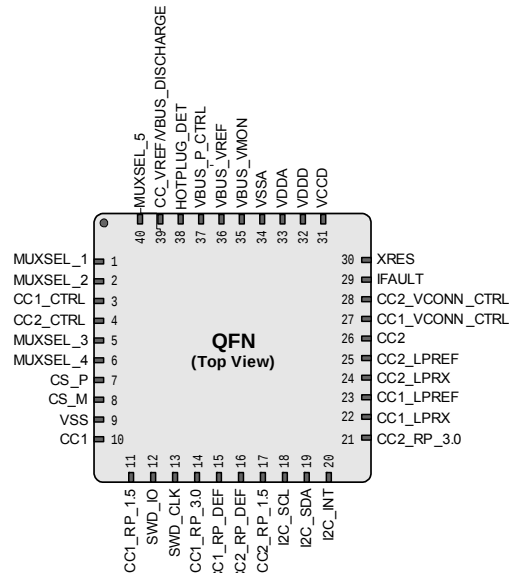


Figure 4. Pinout for CYPD1132-16SXI

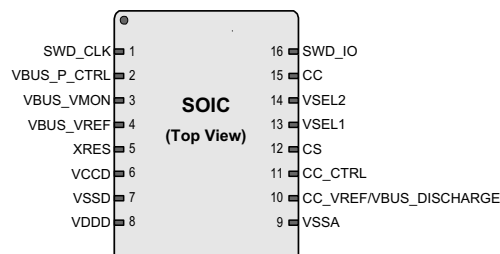
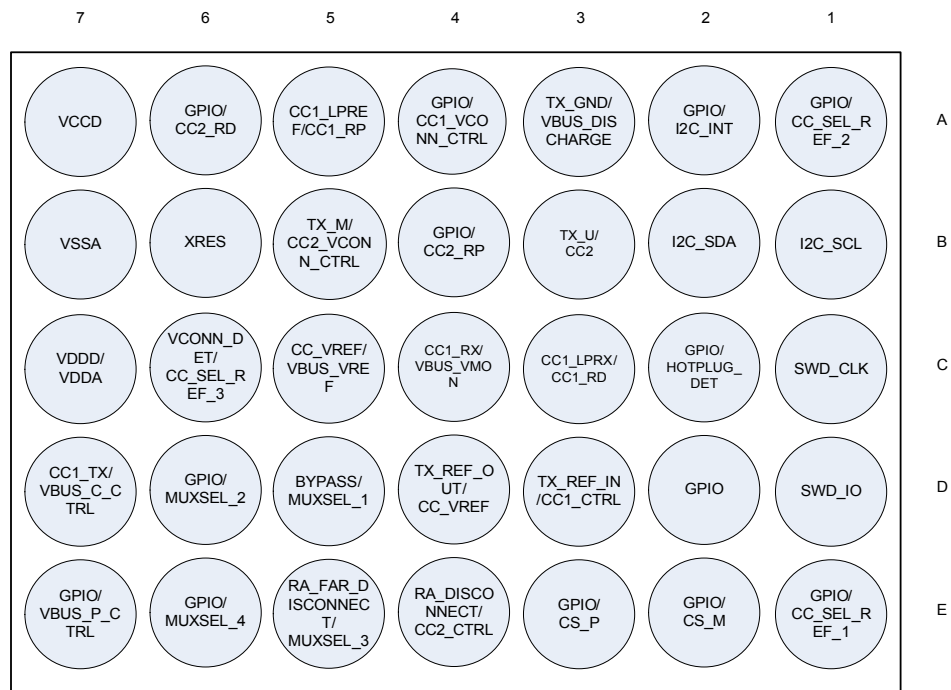


Figure 5. Pinout for CYPD1103-35FNXIT/CYPD1131-FNXIT



Power

The following power system diagram shows the minimum set of power supply pins as implemented for the CCG1. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the VDDA input. There is a separate regulator for the Deep Sleep mode. There is a separate low-noise regulator for the bandgap. The supply voltage range is 3.2 V to 5.5 V with all functions and circuits operating over that range.

VDDA and VDDD must be shorted together; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-μF range in parallel with a smaller capacitor (0.1 μF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Refer to Application Diagrams for bypassing schemes.

Table 7. AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F _{CPU}	CPU frequency	DC	–	48.00	MHz	3.2 ≤ V _{DD} ≤ 5.5
SID49	T _{SLEEP}	Wakeup from sleep mode	–	0.00	–	μs	Guaranteed by characterization
SID50	T _{DEEPSLEEP}	Wakeup from Deep Sleep mode	–	–	25.00	μs	24-MHz IMO. Guaranteed by characterization
SID52	T _{RESETWIDTH}	External reset pulse width	1.00	–	–	μs	Guaranteed by characterization

I/O

Table 8. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V _{IH} ^[12]	Input voltage high threshold	0.70 × V _{DDD}	–	–	V	CMOS Input
SID58	V _{IL}	Input voltage low threshold	–	–	0.30 × V _{DDD}	V	CMOS Input
SID243	V _{IH} ^[12]	LVTTL input	2.00	–	–	V	–
SID244	V _{IL}	LVTTL input	–	–	0.80	V	–
SID59	V _{OH}	Output voltage high level	V _{DDD} –0.60	–	–	V	I _{OH} = 4 mA at 3 V V _{DDD}
SID62	V _{OL}	Output voltage low level	–	–	0.60	V	I _{OL} = 8 mA at 3 V V _{DDD}
SID62A	V _{OL}	Output voltage low level	–	–	0.40	V	I _{OL} = 3 mA at 3 V V _{DDD}
SID63	R _{PULLUP}	Pull-up resistor	3.50	5.60	8.50	kΩ	–
SID64	R _{PULLDOWN}	Pull-down resistor	3.50	5.60	8.50	kΩ	–
SID65	I _{IL}	Input leakage current (absolute value)	–	–	2.00	nA	25 °C, V _{DDD} = 3.0 V
SID65A	I _{IL_CTBM}	Input leakage current (absolute value) for analog pins	–	–	4.00	nA	–
SID66	C _{IN}	Input capacitance	–	–	7.00	pF	–
SID67	V _{HYSTTL}	Input hysteresis LVTTL	15.00	40.00	–	mV	V _{DDD} ≥ 2.7 V. Guaranteed by characterization
SID68	V _{HYSCMOS}	Input hysteresis CMOS	200.00	–	–	mV	V _{DDD} ≥ 4.5 V. Guaranteed by characterization
SID69	I _{DIODE}	Current through protection diode to V _{DD} /V _{SS}	–	–	100.00	μA	Guaranteed by characterization
SID69A	I _{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200.00	mA	Guaranteed by characterization

Table 9. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T _{RISEF}	Rise time	2.00	–	12.00	ns	3.3-V V _{DDD} , Clload = 25 pF
SID71	T _{FALLF}	Fall time	2.00	–	12.00	ns	3.3-V V _{DDD} , Clload = 25 pF

Note

12. V_{IH} must not exceed V_{DDD} + 0.2 V.

I²C

Table 12. Fixed I²C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	–	–	50	μA	–
SID150	I _{I2C2}	Block current consumption at 400 kHz	–	–	135.00	μA	–
SID151	I _{I2C3}	Block current consumption at 1 Mbps	–	–	310.00	μA	–
SID152	I _{I2C4}	I ² C enabled in Deep Sleep mode	–	–	1.40	μA	–

Table 13. Fixed I²C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F _{I2C1}	Bit rate	–	–	1.00	Mbps	–

Memory

Table 14. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	3.20	–	5.50	V	–

Table 15. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE} ^[13]	Row (block) write time (erase and program)	–	–	20.00	ms	Row (block) = 128 bytes
SID175	T _{ROWERASE} ^[13]	Row erase time	–	–	13.00	ms	–
SID176	T _{ROWPROGRAM} ^[13]	Row program time after erase	–	–	7.00	ms	–
SID178	T _{BULKERASE} ^[13]	Bulk erase time (32 KB)	–	–	35.00	ms	–
SID180	T _{DEVPROG} ^[13]	Total device program time	–	–	7.00	seconds	Guaranteed by characterization
SID181	F _{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F _{RET} ^[14]	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	–	Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	–	Flash retention. 85 °C < T _A ≤ 105 °C, 10K P/E cycles	3	–	–	years	Guaranteed by characterization

Notes

13. It can take as much as 20 milliseconds to write to flash. During this time the device should not be Reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
14. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customer care@cypress.com.

System Resources

Power-on-Reset (POR) with Brown Out

Table 16. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	V _{FALLIPOR}	Falling trip voltage	0.75	–	1.40	V	Guaranteed by characterization
SID187	V _{IPOHYST}	Hysteresis	15.0	–	200.0	mV	Guaranteed by characterization

Table 17. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.64	–	–	V	Guaranteed by characterization
SID192	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.40	–	–	V	Guaranteed by characterization

SWD Interface

Table 18. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F _{SWDCLK1}	$3.2\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14.00	MHz	SWDCLK $\leq 1/3$ CPU clock frequency
SID215	T _{SWDI_SETUP}	$T = 1/f_{\text{SWDCLK}}$	$0.25 \times T$	–	–	ns	Guaranteed by characterization
SID216	T _{SWDI_HOLD}	$T = 1/f_{\text{SWDCLK}}$	$0.25 \times T$	–	–	ns	Guaranteed by characterization
SID217	T _{SWDO_VALID}	$T = 1/f_{\text{SWDCLK}}$	–	–	$0.50 \times T$	ns	Guaranteed by characterization
SID217A	T _{SWDO_HOLD}	$T = 1/f_{\text{SWDCLK}}$	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 19. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	1000.00	μA	–

Table 20. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F _{IMOTOL1}	Frequency variation	–	–	±2.00	%	With API-called calibration
SID226	T _{STARTIMO}	IMO startup time	–	–	12.00	μs	–
SID229	T _{JITRMSIMO3}	RMS Jitter at 48 MHz	–	139.00	–	ps	–

Internal Low-Speed Oscillator

Table 21. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I _{ILO1}	ILO operating current at 32 kHz	–	0.30	1.05	μA	Guaranteed by characterization
SID233	I _{ILOLEAK}	ILO leakage current	–	2.00	15.00	nA	Guaranteed by design

Table 22. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	T _{STARTILO1}	ILO startup time	–	–	2.00	ms	Guaranteed by characterization
SID236	T _{ILODUTY}	ILO duty cycle	40.00	50.00	60.00	%	Guaranteed by characterization
SID237	F _{ILOTRIM1}	32-kHz trimmed frequency	15.00	32.00	50.00	kHz	±60% with trim

Figure 7. Two Chip/Cable, Component Count = 15/paddle

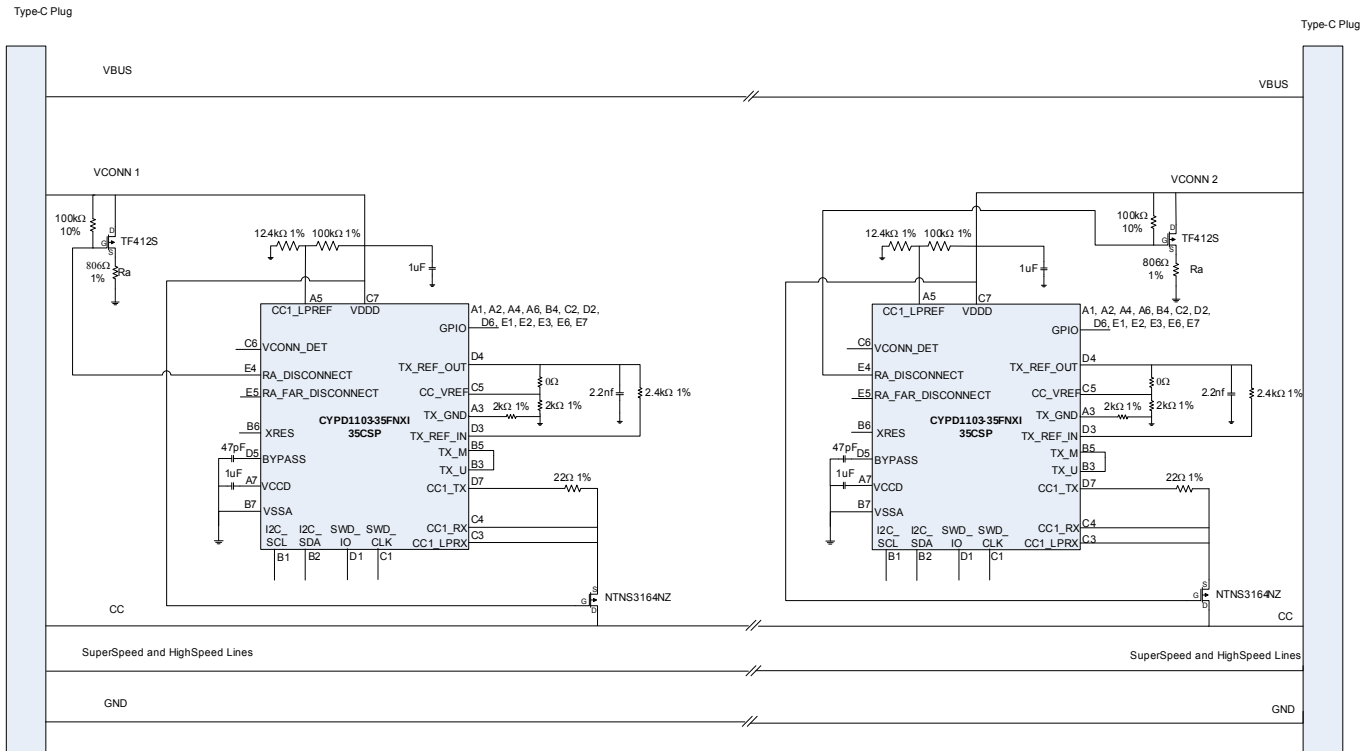
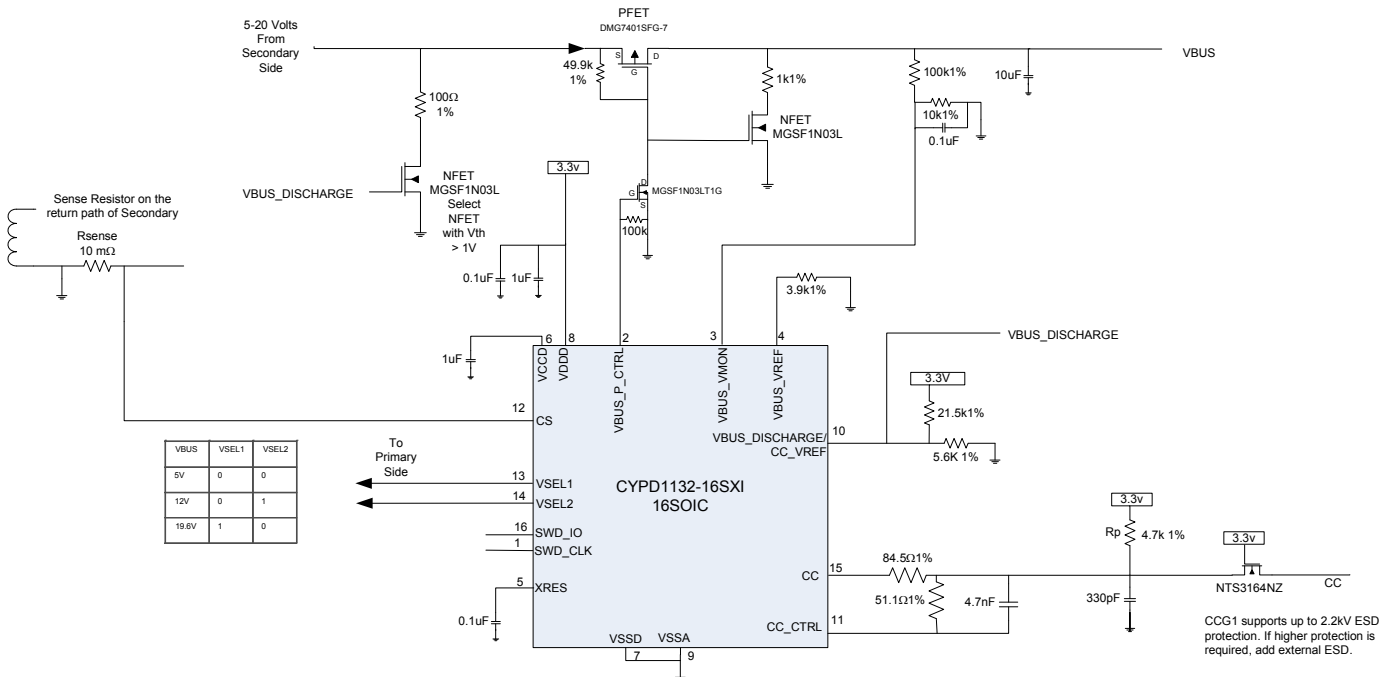


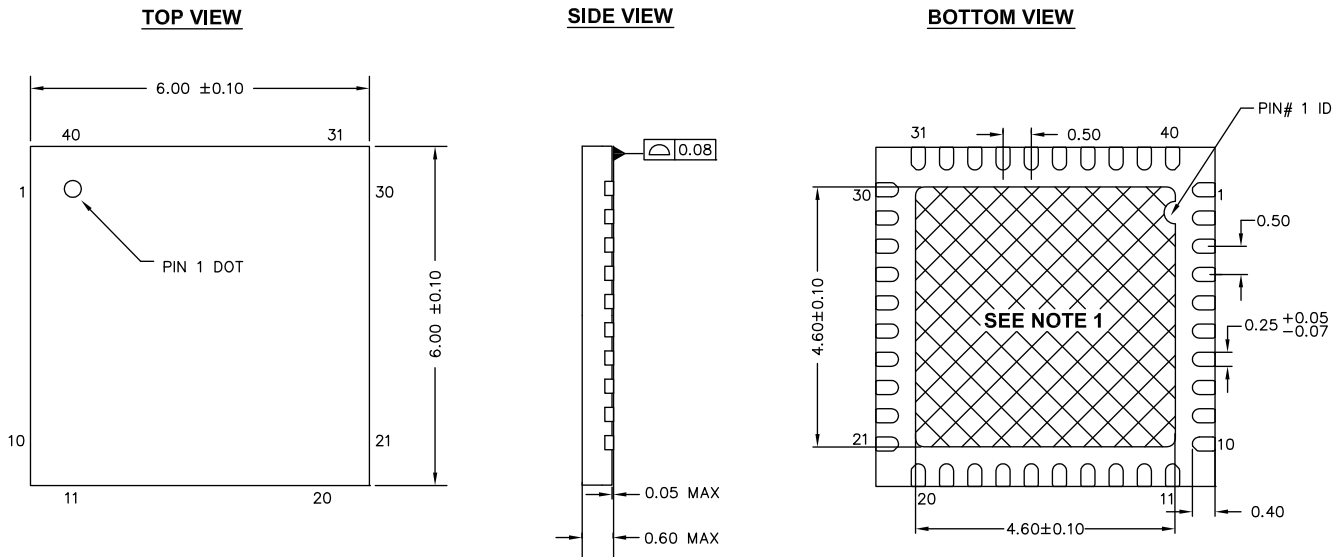
Figure 8. 16-pin SOIC Power Adapter Application Diagram



VBUS	VSEL1	VSEL2
5V	0	0
12V	0	1
19.6V	1	0
0V	1	1

The schematic diagram illustrates the internal structure and pin connections of the CYPD1121-40LQXI 40QFN chip. The chip is a USB-C to DisplayPort converter. The schematic includes a DC/DC converter, a 5V regulator, and various control and data lines. A table on the left shows the VBUS, VSEL1, and VSEL2 pin configurations for different voltage levels. The chip is connected to an Embedded Controller, USB Chipset, and DisplayPort Chipset. The schematic also shows the internal structure of the chip, including the CYPD1121-40LQXI 40QFN chip, the HS/SS/DP Mux, and the Type C Receptacle.

Figure 12. 40-pin QFN Package Outline, 001-80659



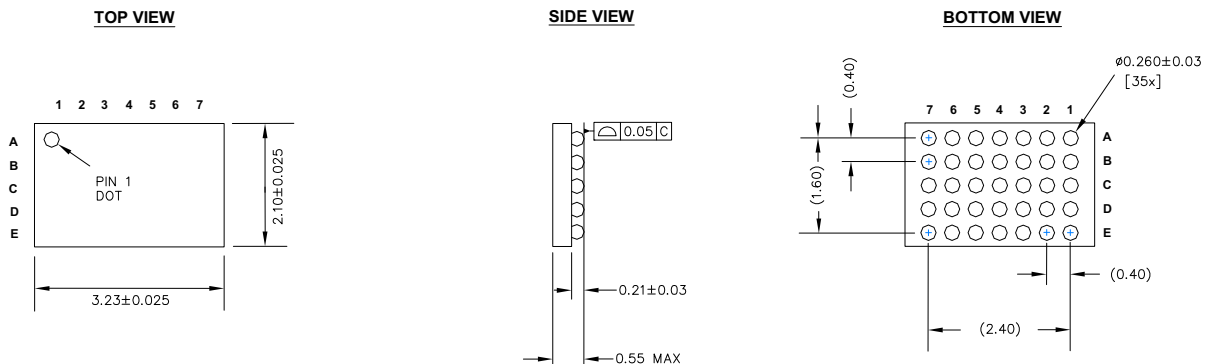
NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 13. 35-Ball WLCSP Package Outline, 001-93741

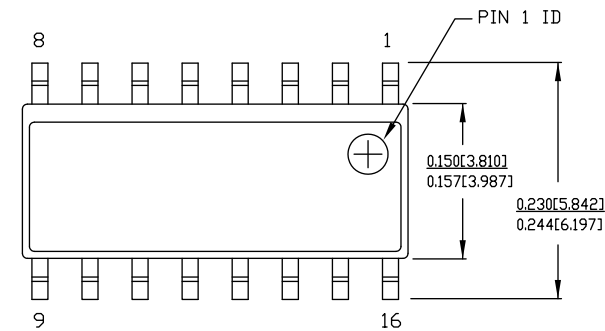


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-93741 **

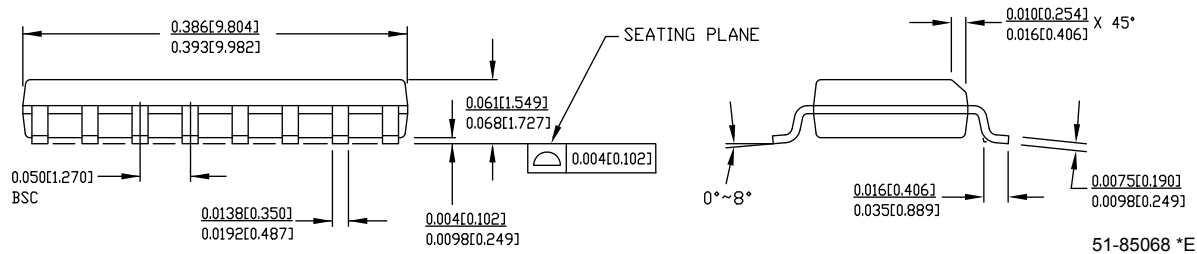
Figure 14. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068



NOTE:

1. DIMENSIONS IN INCHES[MM] **MAX.**
2. REFERENCE JEDEC MS-012
3. PACKAGE WEIGHT : refer to PMDD spec. 001-04308

PART #	
S16.15	STANDARD PKG.
SZ16.15	LEAD FREE PKG.



Acronyms

Table 27. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	Configuration Channel
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	Current Sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
IC	integrated circuit
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO, DIO, SIO, USBIO
LVD	low-voltage detect
LVTTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 27. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	Overcurrent protection
OVP	Overvoltage protection
PCB	printed circuit board
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UFP	upstream facing port
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 28. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision History

Description Title: CCG1 Datasheet USB Type-C Port Controller with Power Delivery Document Number: 001-93639				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4520316	MSMI	09/30/2014	New datasheet
*A	4531795	SJH	10/13/2014	Updated Functional Definition . Updated Figure 8, Figure , Figure 7 , Figure , Figure 14, Figure 9 . Added Figure 11 . Updated Pinouts . Updated Power . Updated Figure , Figure 8. Updated Ordering Information Added Note 24 and referred the same note in 40-pin QFN corresponding to CYPD1122-40LQXI. Added Note 27 and referred the same note in 40-pin QFN corresponding to CYPD1134-40LQXI.
*B	4569912	SJH	11/21/2014	Updated Features . Added 16-pin SOIC related information. Updated Functional Definition . Updated Pin Definitions . Added Table 2. Updated Pinouts . Updated Figure 2 , Figure 5 . Added Figure 4 . Updated Power . Updated Figure , Figure 8. Added Figure 6. Updated Electrical Specifications . Updated Device-Level Specifications . Updated Memory . Added Note 14 and referred the same note in F _{RET} parameter. Added details corresponding to spec ID SID182B under F _{RET} parameter. Updated Figure 14, Figure 9 , Figure 11 . Added Figure 8 and Figure 10 . Updated Ordering Information . Updated part numbers. Added a column "Si ID". Updated Packaging . Updated Table 24 . Updated details in maximum value column corresponding to T _A and T _J parameters. Added 16-pin SOIC related information. Updated Table 25 .
*C	4596141	SJH	12/14/2014	Updated Figure 6, Figure 14, Figure 16. Updated Table 8 , Table 23 .
*D	4646123	SJH	02/04/2015	Updated pin definitions for 40-pin QFN and 35-ball WLCSP. Updated Pinout for CYPD1122-40LQXI/CYPD1121-40LQXI and Ordering Information . Updated conditions for Device-Level Specifications . Updated diagrams in Applications in Detail section.
*E	4686050	VGT	03/13/2015	Removed information about 28-pin SSOP. Updated Table 3 , Table 23 , Table 24 , Table 25 , Table 26 , Table 27 . Updated Figure 2 , Figure .
*F	4747272	VGT	05/13/2015	Updated General Description . Added Note 1 and referenced it in Features . Updated Figure 6 , Figure 8 through Figure 11 . Removed Figure 9. Single Chip/Cable, Component Count = 13. Removed Figure 11. Two Chip/Cable, Component Count = 11/paddle.

Revision History *(continued)*

Description Title: CCG1 Datasheet USB Type-C Port Controller with Power Delivery Document Number: 001-93639				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*G	4800534	VGT	07/02/2015	Updated Low-Power Operation . Updated the number of GPIOs to “up to 30” in GPIO . Updated “1.8 to 5.5 V” to “3.2 V to 5.5 V” in Low-Power Operation , Power System , Power , Device-Level Specifications and Note 15 . Updated Table 2 , Table 4 , Table 5 , Table 6 , Table 7 , Table 8 , Table 14 and Table 18 . Added table footnotes 8 , 9 and 10 . Deleted footnotes 25 through 28. Updated Figure 2 and Figure 8 through Figure 11 . Added Figure 3 . Updated the following in Power : Removed Figures 5 through 8. Updated the section.
*H	4939764	VGT	09/29/2015	Removed specs SID241 and 242. Updated 40-pin QFN package to current revision.
*I	5179365	KISB	03/17/2016	Updated max value of I_{I2C1} from 10.50 μ A to 50 μ A. Updated copyright information and sales links at the end of the document.
*J	5459633	VGT	10/03/2016	Added compliance information regarding the USB Specification. Updated copyright notice to include WICED. Added IoT link in Sales , Solutions , and Legal Information .