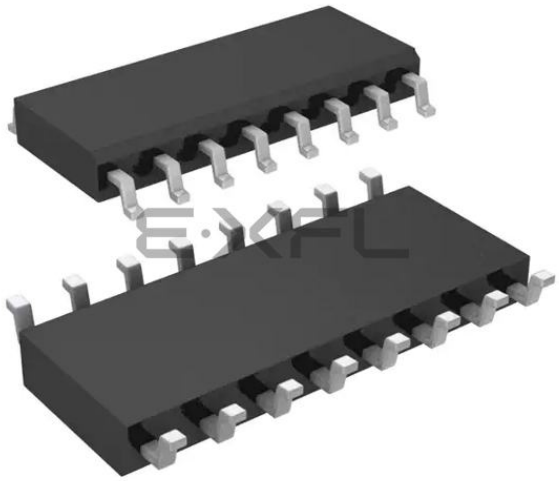

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Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (32KB)
Controller Series	-
RAM Size	4K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	11
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd1132-16sxqt

Contents

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the CCG1 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for CCG1 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The CCG1 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section Power on page 11. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). The CCG1 operates with a single external supply over the range of 3.2 V to 5.5 V operation and has three different power modes: Active, Sleep, and Deep Sleep; transitions between modes are managed by the power system.

Serial Communication Blocks (SCB)

The CCG1 has one SCB, which can implement an I^2C interface. The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZ-I^2C that creates a mailbox address range in the memory of the CCG1 and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices, as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

The CCG1 is not completely compliant with the I^2C spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8 mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I^2C Master, it interposes an IDLE state between NACK and Repeated Start; the I^2C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in the I^2C Slave mode, and Address Match on External Clock is enabled (EC_AM = 1) along with operation in the internally clocked mode (EC_OP = 0), then its I^2C address must be even.

GPIO

The CCG1 has up to 30 GPIOs, which are configured for various functions. Refer to the pinout tables for the definitions. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode).
- Selectable slew rates for dV/dt related noise control to improve EMI.

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network, known as a high-speed I/O matrix, is used to multiplex between various signals that may connect to an I/O pin.

Pin Definitions

Table 1 provides the pin definition for 35-Ball WLCSP for the Cable/EMCA application. Refer to Table 23 for part numbers to package mapping.

Table 1. Pin Definitions for 35-ball WLCSP for EMCA Cable Application

Functional Pin Name	CYPD1103-35FNXIT Balls	Type	Description
CC1_RX	C4	I	CC1 control 0: TX enabled z: RX sense
CC1_TX	D7	O	Configuration Channel 1
SWD_IO	D1	I/O	SWD I/O
SWD_CLK	C1	I	SWD clock
I2C_SCL	B1	I/O	I^2C clock signal
I2C_SDA	B2	I/O	I^2C data signal
XRES	B6	I	Reset
VCCD	A7	POWER	Regulated digital supply output. Connect a 1 to 1.6-µF capacitor. No external source should be connected
VDDD	C7	POWER	Power supply for both analog and digital sections
VSSA	B7	GND	Analog ground
CC_VREF	C5	I	Data reference signal for CC lines
TX_U	B3	O	Signals for internal use only. The TX_U output signal should be connected to the TX_M signal
TX_M	B5	I	–
TX_REF_IN	D3	I	Reference signal for internal use. Connect to TX_REF output via a 2.4K 1% resistor
TX_GND	A3	I	Connect to GND via 2K 1% resistor
TX_REF_OUT	D4	O	Reference signal generated by connecting internal current source to two 1K external resistors
RA_DISCONNECT	E4	O	Optional control signal to remove RA after assertion of VCONN 0: RA disconnected 1: RA connected
VCONN_DET	C6	I	Local VCONN detection signal 0: VCONN is not locally applied 1: VCONN is locally applied
CC1_LPREF	A5	I	Reference signal for internal use. Connect to the output of resistor divider from VDDD.
RA_FAR_DISCONNECT	E5	O	Optional control signal to remove RA after assertion of VCONN (NC for 2 chip/cable) 0: RA disconnected 1: RA connected
BYPASS	D5	I	Bypass capacitor for internal analog circuits
CC1_LPRX	C3	I	Configuration channel 1 RX signal for Low Power States
GPIO	A1, A2, A4, A6, B4, C2, D2, D6, E1, E2, E3, E6, E7	–	General-purpose I/Os

Table 2 provides the pin definitions for 40-pin QFN and 35-ball WLCSP for the notebook, tablet, smartphone, and monitor applications. Refer to Table 23 on page 23 for part numbers to package mapping.

Table 2. Pin Definitions for 40-QFN and 35-ball WLCSP for Notebook, Tablet, SmartPhone and Monitor Applications

Functional Pins	CYPD 1122-40LQXI Pins[8]	CYPD 1121-40LQXI Pins[9]	CYPD 1131-35FNXIT Balls[10]	Type	Description
MUXSEL_1	1	1	D5	O	External Data Mux Select signal 1
MUXSEL_2	2	2	D6	O	External Data Mux Select signal 2
CC1_CTRL	3	3	D3	I/O	CC1 control 0: TX enabled z: RX sense
CC2_CTRL	4	4	E4	I/O	CC2 control 0: TX enabled z: RX sense
MUXSEL_3	5	5	E5	O	External Data Mux Select signal 3
MUXSEL_4	6	6	E6	O	External Data Mux Select signal 4
CS_P	7	7	E3	I	Current Sensing Plus input
CS_M	8	8	E2	I	Current Sensing Minus input I
VSS	9	9	–	GND	Ground
CC1	10	10	-	I/O	Configuration Channel 1
CC_SEL_REF_1	11	11	E1	O	CC Reference Select signal
SWD_IO	12	12	D1	I/O	SWD IO
SWD_CLK	13	13	C1	I	SWD Clock
HOTPLUG_DET	14	14	C2	I/O	HotPlug Detection for Display Port Alternate Mode
GPIO1	15	–	–	I/O	General-purpose I/O
VSEL2	–	15	–	O	Voltage Select signal 2 for selecting output voltage
GPIO2	16	–	–	I/O	General-purpose I/O
GPIO3	17	–	–	I/O	General-purpose I/O
IFAULT	–	17	–	I	Current Fault Indication 0: No fault 1: Current fault
I2C_SCL	18	18	B1	I/O	I2C Clock signal
I2C_SDA	19	19	B2	I/O	I2C Data signal
I2C_INT	20	20	A2	O	I2C Interrupt
CC_SEL_REF_2	21	21	A1	O	CC Reference Select signal
CC1_RD	22	22	C3	O	Open Drain signal to connect RD to CC 1 line z: RD not connected 0: RD connected for Monitor application 1: RD connected for Notebook application
CC1_RP	23	23	A5	O	Open Source signal to connect RP to CC 1 line z: RP not connected 1: RP connected

Notes
8. Pinout for Notebook DRP application for 40-QFN.
9. Pinout for Monitor DRP application for 40-QFN.
10. Pinout for Notebook DRP application for 35-CSP.

Table 2. Pin Definitions for 40-QFN and 35-ball WLCSP for Notebook, Tablet, SmartPhone and Monitor Applications *(continued)*

Functional Pins	CYPD 1122-40LQXI Pins[8]	CYPD 1121-40LQXI Pins[9]	CYPD 1131-35FNXIT Balls[10]	Type	Description
CC1_VCONN_CTRL	24	24	A4	O	Open Drain signal to control a PFET power switch for VCONN on CC 1 line 0: VCONN switch closed z: VCONN switch open
VBUS_DISCHARGE	25	25	A3	O	Signal used for discharging VBUS line during voltage change
CC2	26	26	B3	O	Configuration Channel 2
CC2_RD	27	27	A6	O	Open Drain signal to connect RD to CC 2 line z: RD not connected 0: RD connected for Monitor application 1: RD connected for Notebook application
CC2_RP	28	28	B4	O	Open Source signal to connect RP to CC 2 line z: RP not connected 1: RP connected
CC2_VCONN_CTRL	29	29	B5	O	Open Drain signal to control a PFET power switch for VCONN on CC 2 line 0: VCONN switch closed z: VCONN switch open
XRES	30	30	B6	I	Reset
VCCD	31	31	A7	POWER	Regulated digital supply output. Connect a 1 to 1.6-µF capacitor. No external source should be connected
VDDD	32	32	C7	POWER	Power supply for digital sections
VDDA	33	33	C7	POWER	Power Supply for analog sections
VSSA	34	34	B7	GND	Analog ground pin
VBUS_VMON	35	35	C4	I	VBUS Overvoltage Protection monitoring signal
VBUS_VREF	36	36	C5	I	VBUS reference signal for Overvoltage Protection detection
VSEL1	–	37	–	O	Voltage Select signal 1 for selecting the output voltage
CC_SEL_REF_3	37	16	C6	O	CC Reference Select signal
VBUS_C_CTRL	38	–	D7	O	Full rail control signal for enabling/disabling Consumer load FET
VBUS_OK	–	38	–		VBUS_OK=1 - VBUS Voltage ok VBUS_OK=0 - VBUS Overvoltage detected
CC_VREF	39	39	D4	I	Data reference signal for CC lines
VBUS_P_CTRL	40	40	E7	O	Full rail control signal for enabling/disabling Provider load FET

Notes
8. Pinout for Notebook DRP application for 40-QFN.
9. Pinout for Monitor DRP application for 40-QFN.
10. Pinout for Notebook DRP application for 35-CSP.

Table 3 provides the pin definition for 40-pin QFN for Notebook (DFP) application. Refer to Table 23 for part numbers to package mapping.

Table 3. Pin Definitions for 40-Pin QFN for Notebook (DFP)

Functional Pin Name	Active HIGH/ LOW	Drive Mode	CYPD 1134-40LQXI Pins	Type	Description
MUXSEL_1	–	Open drain, drives low	1	O	External Data Mux Select signal 1
MUXSEL_2	–	Open drain, drives low	2	O	External Data Mux Select signal 2
CC1_CTRL	–	Analog input/Strong drive (push pull)	3	IO	CC1 control 0:Tx enabled z: RX sense
CC2_CTRL	–	Analog input/Strong drive (push pull)	4	IO	CC2 control 0: TX enabled z: RX sense
MUXSEL_3	–	Open drain, drives low	5	O	External Data Mux Select signal 3
MUXSEL_4	–	Open drain, drives low	6	O	External Data Mux Select signal 4
CS_P	–	Analog input	7	I	Current Sensing Plus input
CS_M	–	Analog input	8	I	Current Sensing Minus input
VSS	–	–	9	GND	Ground
CC1	–	Strong drive (push pull)	10	O	Configuration Channel 1
CC1_RP_1.5	Active HIGH	Open drain, drives high	11	O	Open Drain signal to connect RP to CC1 line (1.5A current) z: RP not connected 1: RP connected
SWD_IO	–	–	12	IO	SWD IO
SWD_CLK	–	–	13	I	SWD Clock
CC1_RP_3.0	Active HIGH	Open drain, drives high	14	O	Open Source signal to connect RP to CC1 line (3A current) z: RP not connected 1: RP connected
CC1_RP_DEF	Active HIGH	Open drain, drives high	15	O	Open Drain signal to connect RP to CC1 line (Default current) z: RP not connected 1: RP connected
CC2_RP_DEF	Active HIGH	Open drain, drives high	16	O	Open Drain signal to connect RP to CC2 line (Default current) z: RP not connected 1: RP connected
CC2_RP_1.5	Active HIGH	Open drain, drives high	17	O	Open Drain signal to connect RP to CC2 line (1.5A current) z: RP not connected 1: RP connected
I2C_SCL	Active LOW	Open drain, drives low	18	IO	I^2C Clock signal
I2C_SDA	Active LOW	Open drain, drives low	19	IO	I^2C Data signal
I2C_INT	Active LOW	Open drain, drives low	20	O	I^2C Interrupt

Table 4 provides the pin definition for 16-pin SOIC for the Power Adapter application. Refer to Table 23 on page 23 for part numbers to package mapping.

Table 4. Pin Definitions for 16-pin SOIC for Power Adapter Application

Functional Pin Name	CYPD 1132-16SXI Pins	Type	Description
SWD_CLK	1	I	SWD Clock
VBUS_P_CTRL	2	O	Full rail control signal for enabling/disabling provider load FET
VBUS_VMON	3	I	VBUS over-voltage protection monitoring signal
VBUS_VREF	4	I	VBUS reference signal for over-voltage protection detection
XRES	5	–	Active Low Reset
VCCD	6	–	Connect 1 µF capacitor between VCCD and GROUND
VSSD	7	–	Ground
VDDD	8	–	Power 3.3 V/5 V
VSSA	9	–	Ground
CC_VREF/VBUS_DISCHARGE	10	I/O	Data reference signal for CC line (0.55 Volt) / Signal used for discharging VBUS line during voltage decrease
CC_CTRL	11	I/O	CC1 control 0: TX enabled z: RX sense
CS	12	I	Low Side Current Sense
VSEL1	13	O	Voltage select signal for selecting the output voltage 5/12/20 V
VSEL2	14	O	Voltage select signal for selecting the output voltage 5/12/20 V
CC	15	I/O	Configuration Channel TX/RX
SWD_IO	16	I/O	SWD I/O

Pinouts

Figure 2. Pinout for CYPD1122-40LQXI/CYPD1121-40LQXI

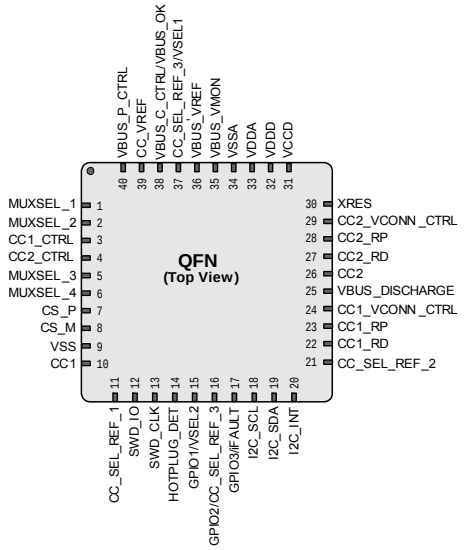


Figure 3. Pinout for CYPD1134-40LQXI

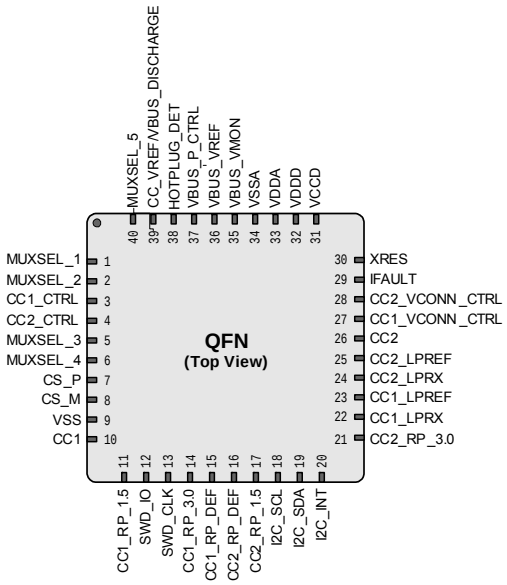


Figure 4. Pinout for CYPD1132-16SXI

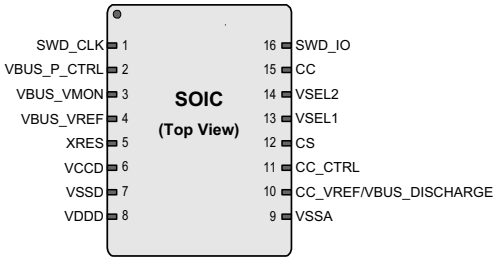
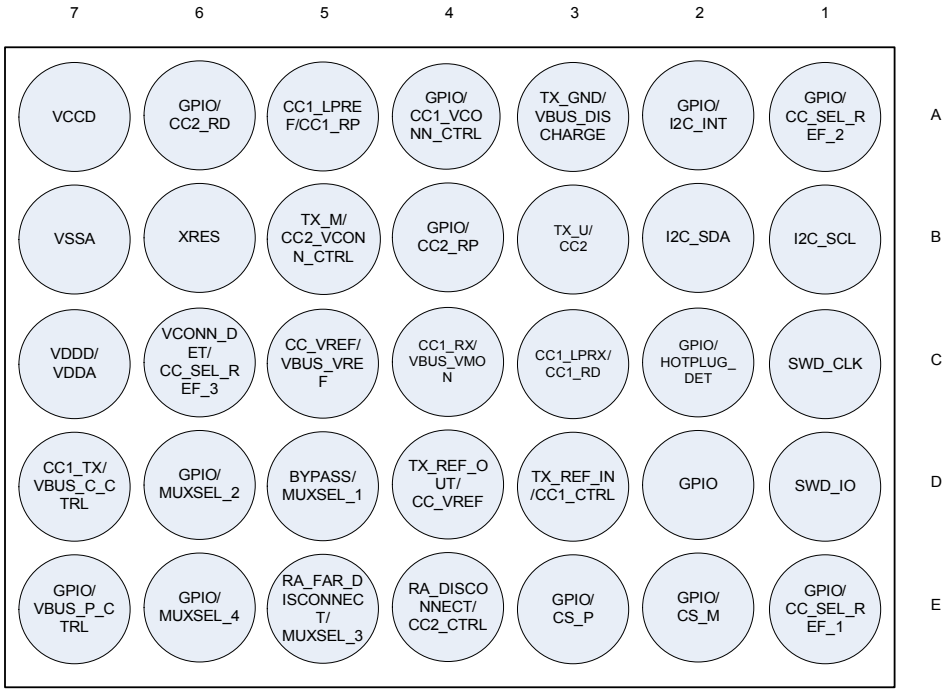


Figure 5. Pinout for CYPD1103-35FNXIT/CYPD1131-FNXIT



Power

The following power system diagram shows the minimum set of power supply pins as implemented for the CCG1. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the VDDA input. There is a separate regulator for the Deep Sleep mode. There is a separate low-noise regulator for the bandgap. The supply voltage range is 3.2 V to 5.5 V with all functions and circuits operating over that range.

VDDA and VDDD must be shorted together; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Refer to Application Diagrams for bypassing schemes.

XRES

Table 10. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.70 × V_{DDD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage low threshold	–	–	0.30 × V_{DDD}	V	CMOS input
SID79	R_{PULLUP}	Pull-up resistor	3.50	5.60	8.50	kΩ	–
SID80	C_{IN}	Input capacitance	–	3.00	–	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100.00	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100.00	µA	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for VSEL and CUR_LIM Pins

Table 11. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID140	$T_{PWMFREQ}$	Operating frequency	–	–	48.00	MHz	–
SID141	$T_{PWMPWINT}$	Pulse width (internal)	42.00	–	–	ns	–
SID142	T_{PWMEXT}	Pulse width (external)	42.00	–	–	ns	–
SID143	$T_{PWMKILLINT}$	Kill pulse width (internal)	42.00	–	–	ns	–
SID144	$T_{PWMKILLEXT}$	Kill pulse width (external)	42.00	–	–	ns	–
SID145	$T_{PWMEINT}$	Enable pulse width (internal)	42.00	–	–	ns	–
SID146	$T_{PWMENEXT}$	Enable pulse width (external)	42.00	–	–	ns	–
SID147	$T_{PWMRESWINT}$	Reset pulse width (internal)	42.00	–	–	ns	–
SID148	$T_{PWMRESWEXT}$	Reset pulse width (external)	42.00	–	–	ns	–

System Resources

Power-on-Reset (POR) with Brown Out

Table 16. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.40	V	Guaranteed by characterization
SID187	$V_{IPORHYST}$	Hysteresis	15.0	–	200.0	mV	Guaranteed by characterization

Table 17. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.64	–	–	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.40	–	–	V	Guaranteed by characterization

SWD Interface

Table 18. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	$3.2\ V \le V_{DDD} \le 5.5\ V$	–	–	14.00	MHz	SWDCLK ≤1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 19. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000.00	µA	–

Table 20. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation	–	–	±2.00	%	With API-called calibration
SID226	$T_{STARTIMO}$	IMO startup time	–	–	12.00	µs	–
SID229	$T_{JITRMSIMO3}$	RMS Jitter at 48 MHz	–	139.00	–	ps	–

Internal Low-Speed Oscillator

Table 21. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.30	1.05	µA	Guaranteed by characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2.00	15.00	nA	Guaranteed by design

Table 22. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2.00	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40.00	50.00	60.00	%	Guaranteed by characterization
SID237	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15.00	32.00	50.00	kHz	±60% with trim

Applications in Detail

Figure 6. Single Chip/Cable, Component Count = 19

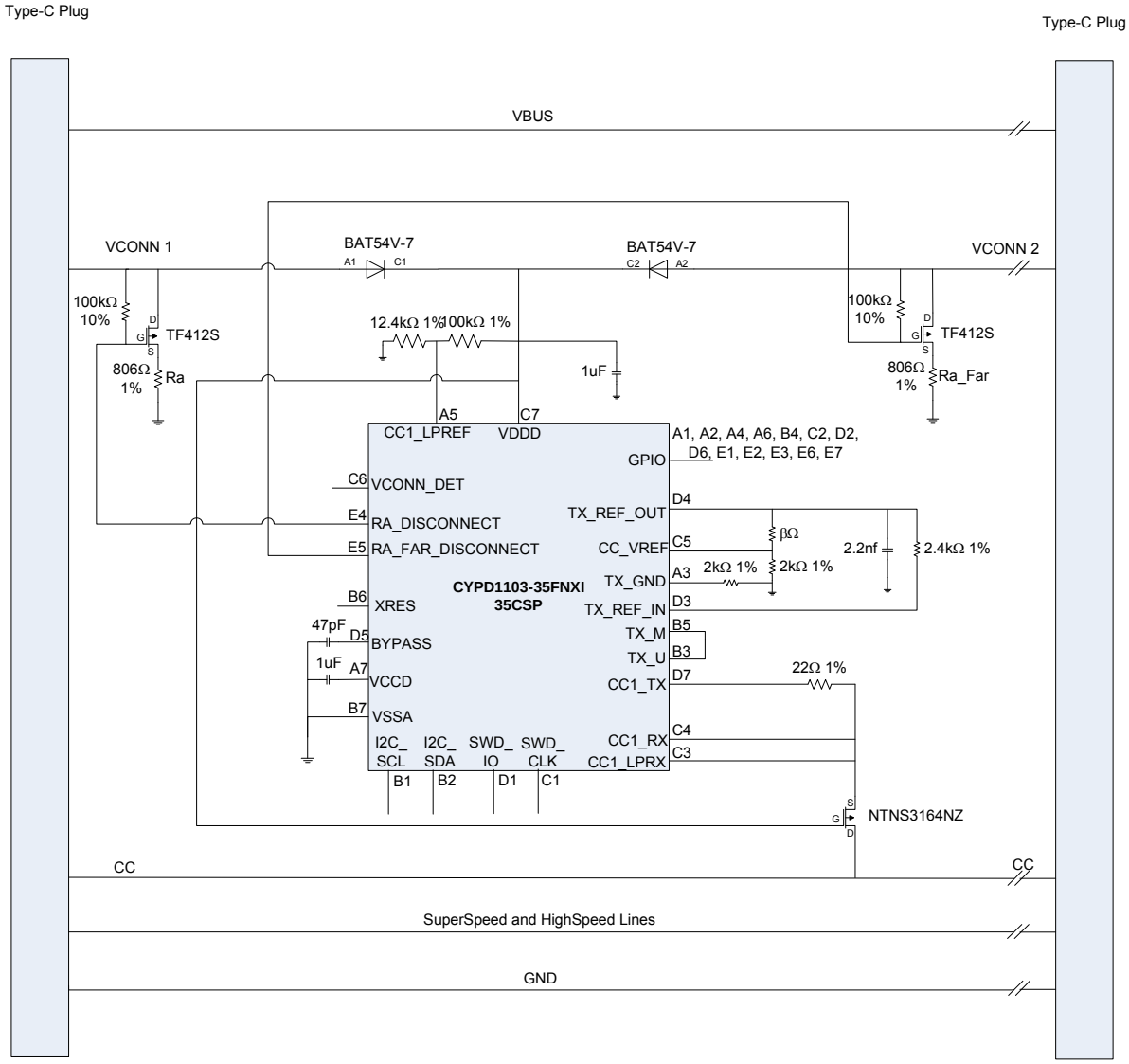


Figure 7. Two Chip/Cable, Component Count = 15/paddle

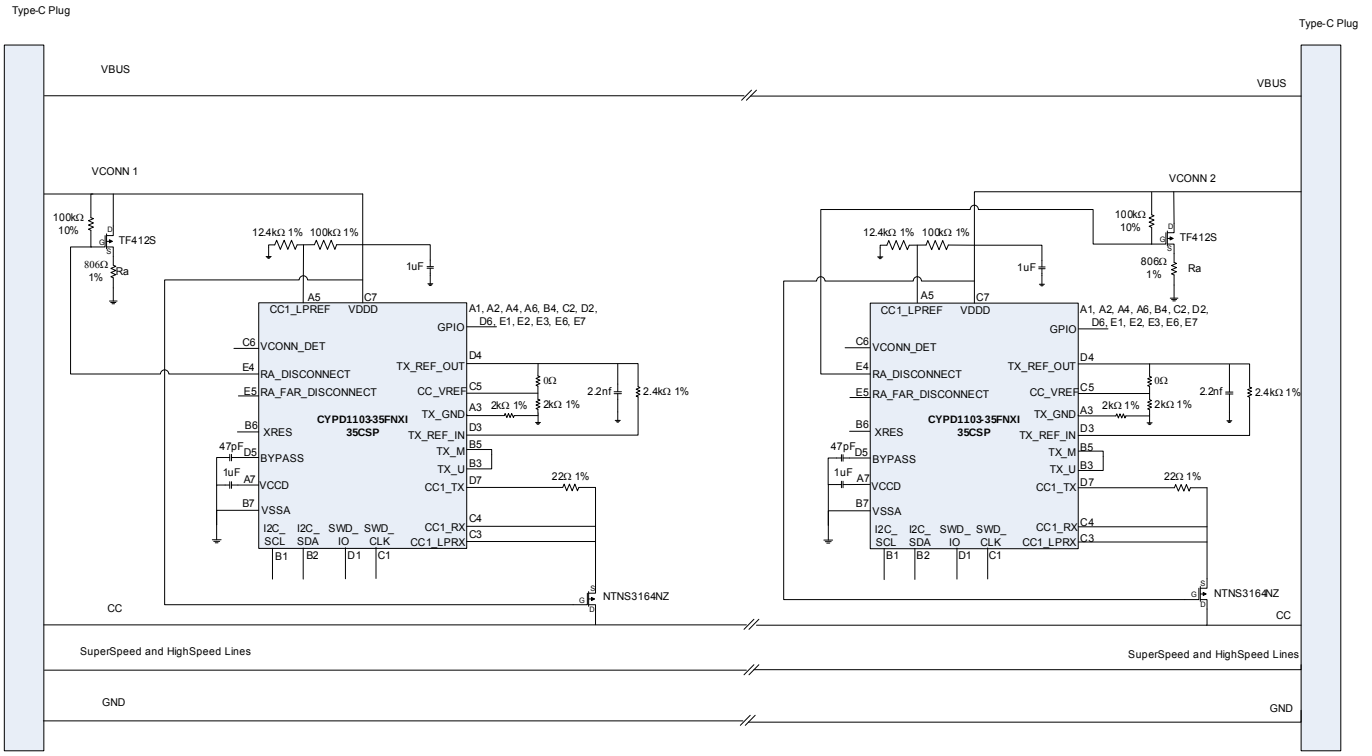


Figure 8. 16-pin SOIC Power Adapter Application Diagram

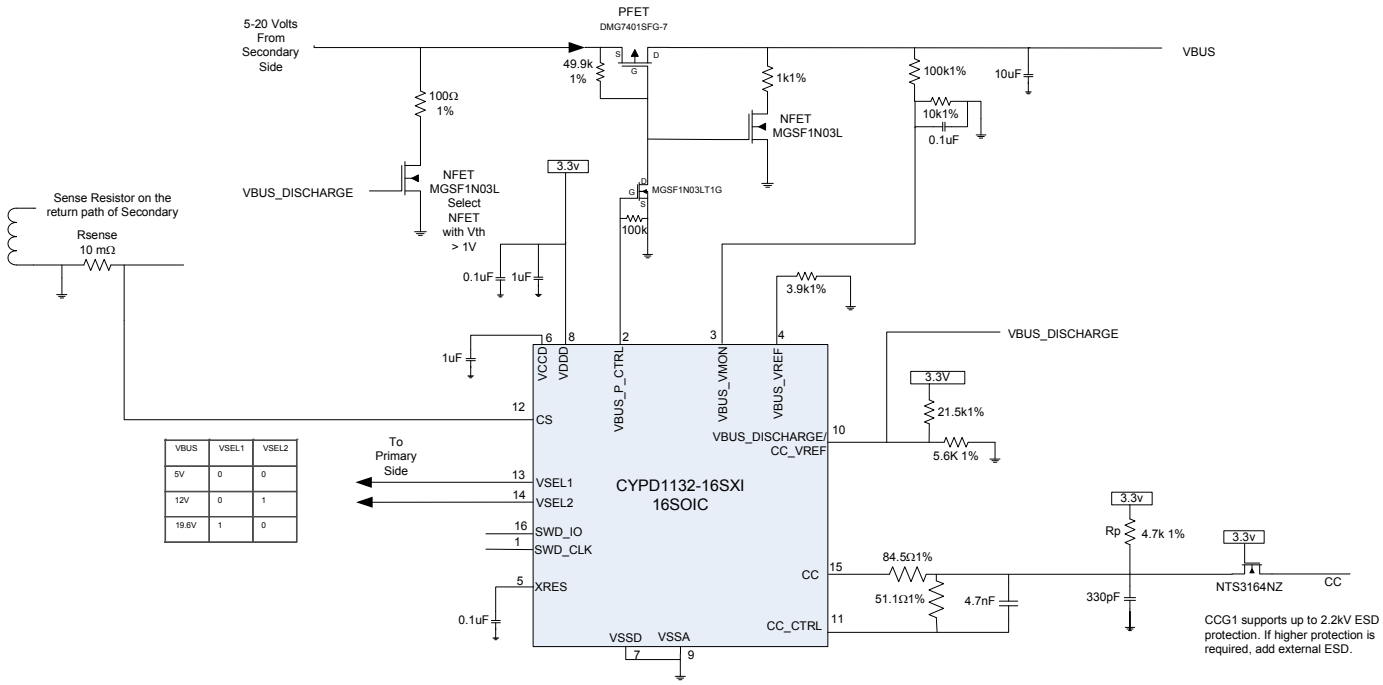


Figure 10. Notebook (DFP) Application Diagram

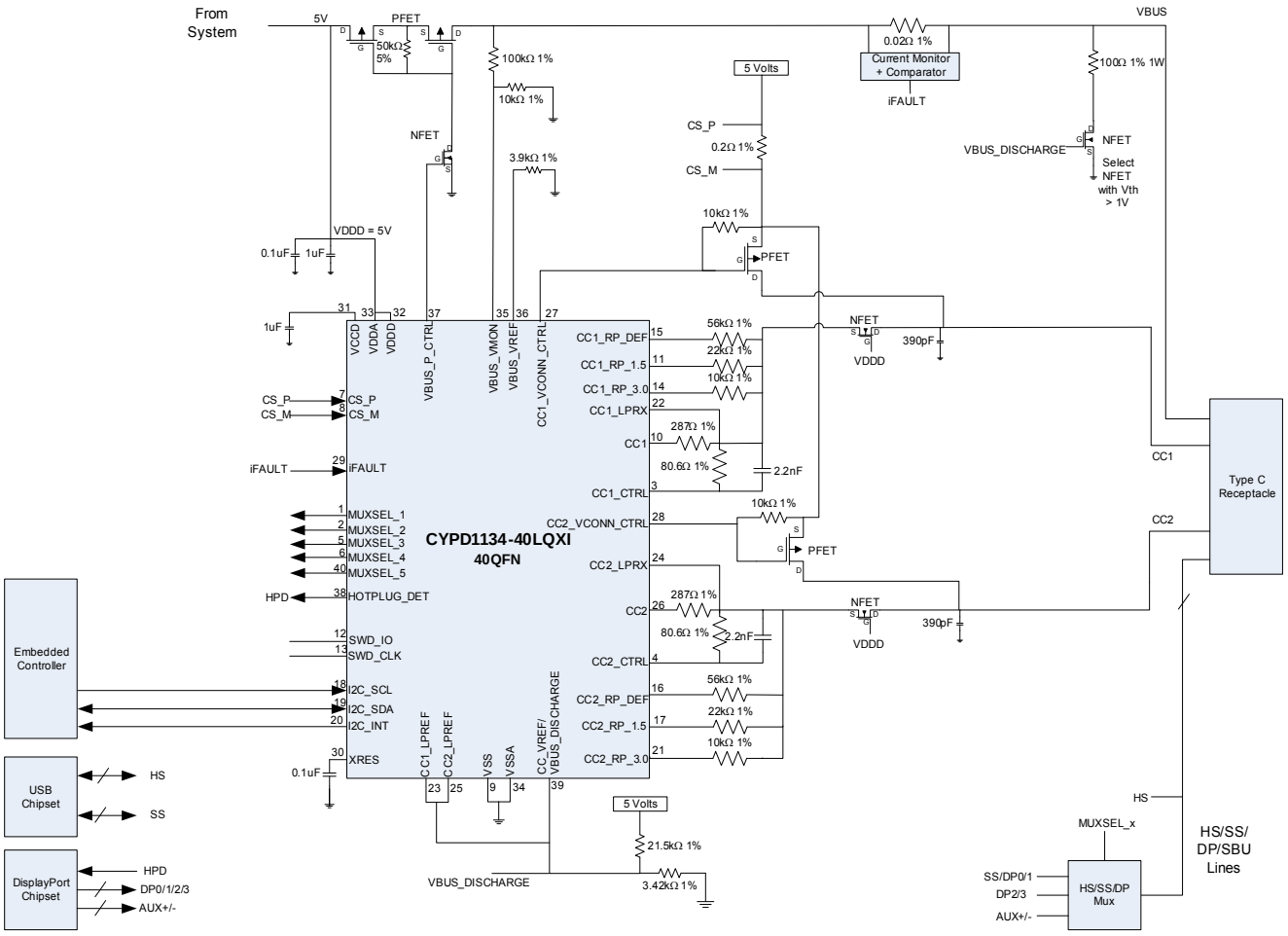
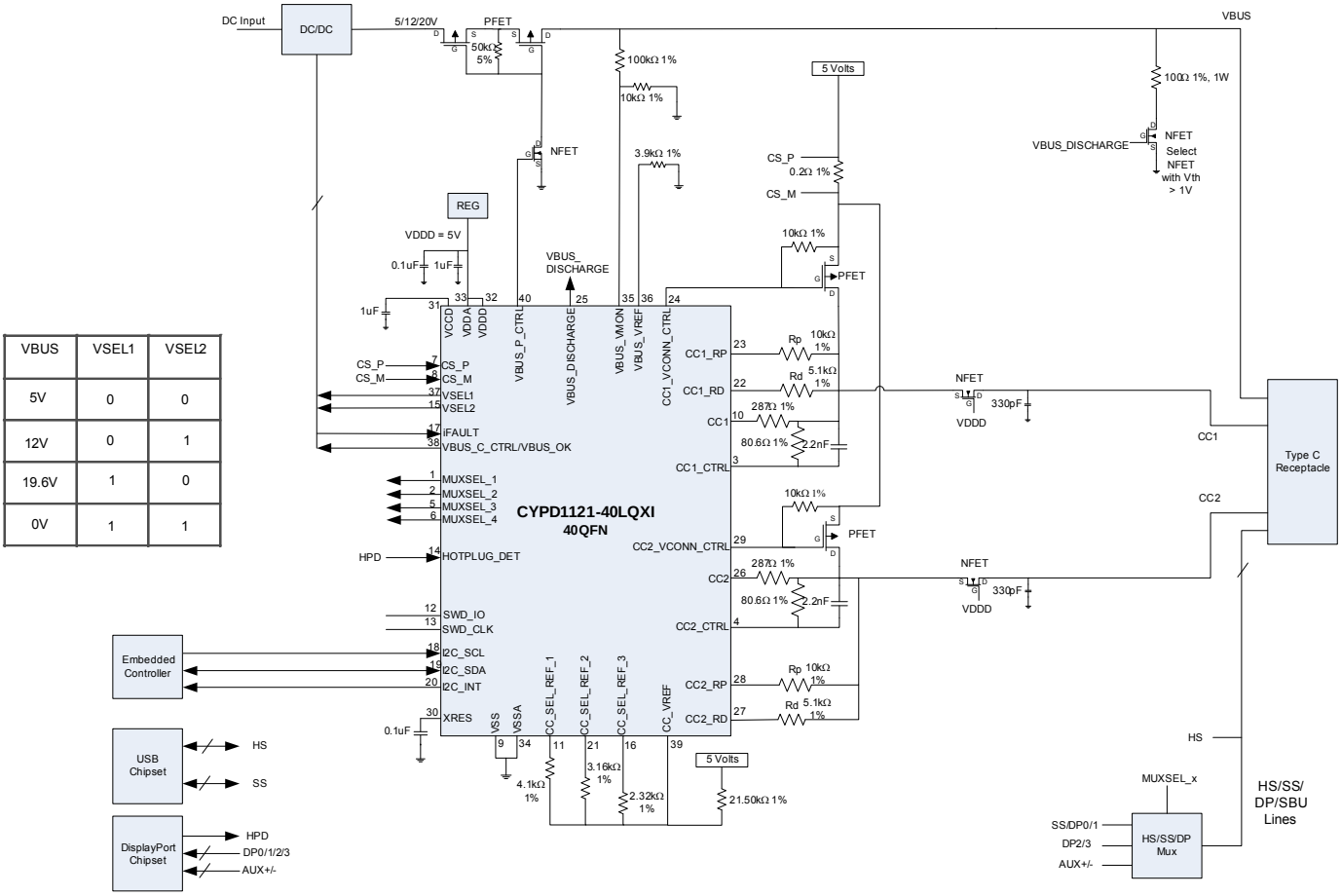


Figure 11. Monitor Application Block Diagram



VBUS	VSEL1	VSEL2
5V	0	0
12V	0	1
19.6V	1	0
0V	1	1

Packaging

Table 24. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A (40-QFN, 35-CSP)	Operating ambient temperature	–	–40	25.00	85.00	°C
T_J (40-QFN, 35-CSP)	Operating junction temperature	–	–40	–	100.00	°C
T_A (16-SOIC)	Operating ambient temperature	–	–40	25.00	105.00	°C
T_J (16-SOIC)	Operating junction temperature	–	–40	–	120.00	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	15.34	–	°C/Watt
T_{JA}	Package θ_{JA} (35-CSP)	–	–	28.00	–	°C/Watt
T_{JA}	Package θ_{JA} (16-SOIC)	–	–	85.00	–	°C/Watt
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	02.50	–	°C/Watt
T_{JC}	Package θ_{JC} (35-CSP)	–	–	00.40	–	°C/Watt
T_{JC}	Package θ_{JC} (16-SOIC)	–	–	49.00	–	°C/Watt

Table 25. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
16-pin SOIC	260 °C	30 seconds
40-pin QFN	260 °C	30 seconds
35-ball WLCSP	260 °C	30 seconds

Table 26. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
16-pin SOIC	MSL 3
40-pin QFN	MSL 3
35-ball WLCSP	MSL 1

Document Conventions

Units of Measure

Table 28. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision History

Description Title: CCG1 Datasheet USB Type-C Port Controller with Power Delivery Document Number: 001-93639				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4520316	MSMI	09/30/2014	New datasheet
*A	4531795	SJH	10/13/2014	Updated Functional Definition. Updated Figure 8, Figure , Figure 7, Figure , Figure 14, Figure 9. Added Figure 11. Updated Pinouts. Updated Power. Updated Figure , Figure 8. Updated Ordering Information Added Note 24 and referred the same note in 40-pin QFN corresponding to CYPD1122-40LQXI. Added Note 27 and referred the same note in 40-pin QFN corresponding to CYPD1134-40LQXI.
*B	4569912	SJH	11/21/2014	Updated Features. Added 16-pin SOIC related information. Updated Functional Definition. Updated Pin Definitions. Added Table 2. Updated Pinouts. Updated Figure 2, Figure 5. Added Figure 4. Updated Power. Updated Figure , Figure 8. Added Figure 6. Updated Electrical Specifications. Updated Device-Level Specifications. Updated Memory. Added Note 14 and referred the same note in F_{RET} parameter. Added details corresponding to spec ID SID182B under F_{RET} parameter. Updated Figure 14, Figure 9, Figure 11. Added Figure 8 and Figure 10. Updated Ordering Information. Updated part numbers. Added a column “Si ID”. Updated Packaging. Updated Table 24. Updated details in maximum value column corresponding to T_A and T_J parameters. Added 16-pin SOIC related information. Updated Table 25.
*C	4596141	SJH	12/14/2014	Updated Figure 6, Figure 14, Figure 16. Updated Table 8, Table 23.
*D	4646123	SJH	02/04/2015	Updated pin definitions for 40-pin QFN and 35-ball WLCSP. Updated Pinout for CYPD1122-40LQXI/CYPD1121-40LQXI and Ordering Information. Updated conditions for Device-Level Specifications. Updated diagrams in Applications in Detail section.
*E	4686050	VGT	03/13/2015	Removed information about 28-pin SSOP. Updated Table 3, Table 23, Table 24, Table 25, Table 26, Table 27. Updated Figure 2, Figure .
*F	4747272	VGT	05/13//2015	Updated General Description. Added Note 1 and referenced it in Features. Updated Figure 6, Figure 8 through Figure 11. Removed Figure 9. Single Chip/Cable, Component Count = 13. Removed Figure 11. Two Chip/Cable, Component Count = 11/paddle.

Revision History *(continued)*

Description Title: CCG1 Datasheet USB Type-C Port Controller with Power Delivery Document Number: 001-93639				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G	4800534	VGT	07/02/2015	Updated Low-Power Operation. Updated the number of GPIOs to “up to 30” in GPIO. Updated “1.8 to 5.5 V” to “3.2 V to 5.5 V” in Low-Power Operation, Power System, Power, Device-Level Specifications and Note 15. Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 14 and Table 18. Added table footnotes 8, 9 and 10. Deleted footnotes 25 through 28. Updated Figure 2 and Figure 8 through Figure 11. Added Figure 3. Updated the following in Power: Removed Figures 5 through 8. Updated the section.
*H	4939764	VGT	09/29/2015	Removed specs SID241 and 242. Updated 40-pin QFN package to current revision.
*I	5179365	KISB	03/17/2016	Updated max value of I_{I2C1} from 10.50 µA to 50 µA. Updated copyright information and sales links at the end of the document.
*J	5459633	VGT	10/03/2016	Added compliance information regarding the USB Specification. Updated copyright notice to include WICED. Added IoT link in Sales, Solutions, and Legal Information.