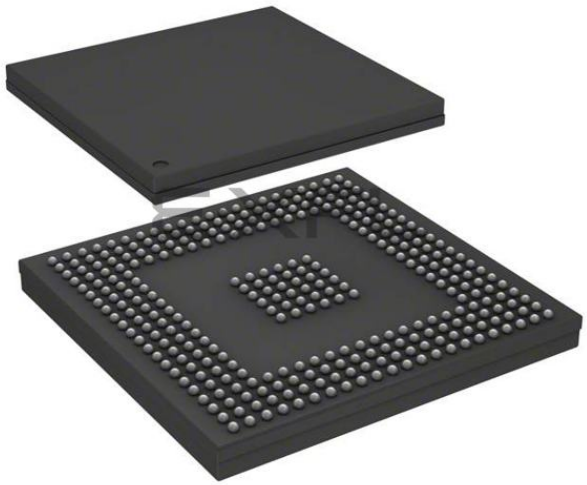

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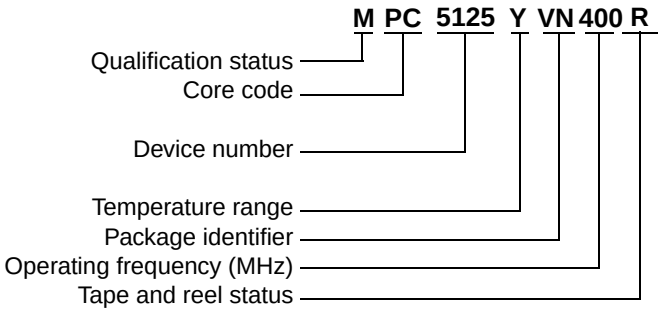
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e300
Core Size	32-Bit Single-Core
Speed	400MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, USB OTG
Peripherals	DMA, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5125yvn400r

1 Ordering Information



Temperature Range
Y = –40 °C to 125 °C, junction

Package Identifier
VN = 324 TEPBGA Pb-free

Operating Frequency
400 = 400 MHz

Tape and Reel Status
R = Tape and reel
(blank) = Trays

Qualification Status
P = Pre qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Note: Not all options are available on all devices. Refer to Table 1.

Figure 1. MPC5125 Orderable Part Number Description

Table 1 shows the orderable part numbers for the MPC5125.

Table 1. MPC5125 Orderable Part Numbers

Freescale Part Number[1]	Package Description	Speed (MHz)	Operating Temperature[2]	
		Max[3] (f_{MAX})	Min (T_L)	Max (T_H)
MPC5125YVN400	MPC5125 324TEPBGA package Lead-free (PbFree)	400 MHz core 200 MHz bus	–40 °C	125 °C

NOTES:
1 All packaged devices are PPC5125, rather than MPC125, until product qualifications are complete.
2 The lowest ambient operating temperature (T_A) is referenced by T_L; the highest junction temperature is referenced by T_H.
3 Maximum speed is the maximum frequency allowed including frequency modulation (FM).

2 MPC5125 Block Diagrams

Figure 2 shows a simplified MPC5125 block diagram.

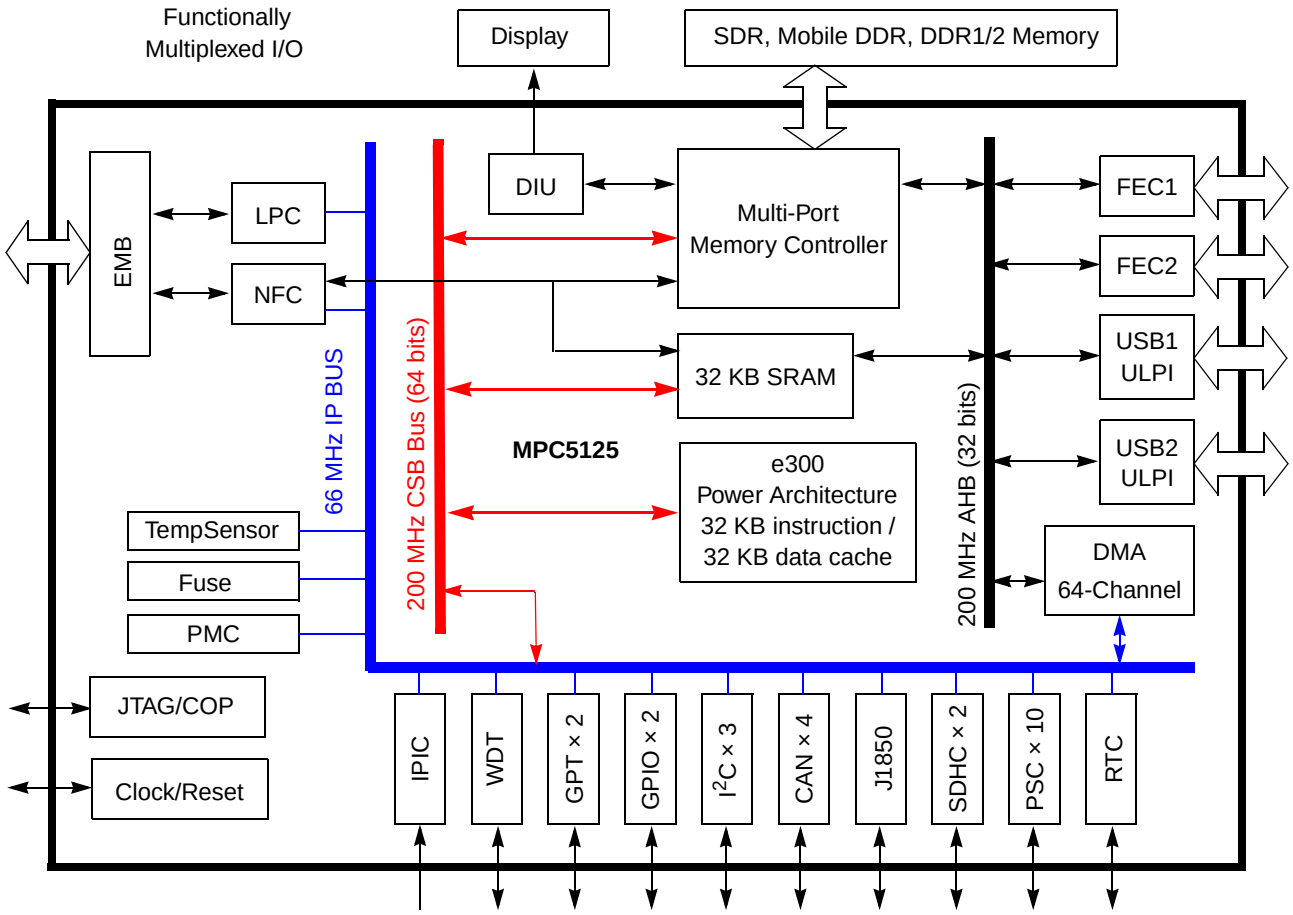


Figure 2. Simplified MPC5125 Block Diagram

Table 2. MPC5125 Pin Multiplexing (continued)

Pin	Pad I/O Control Register[1] and Offset[2]	Alternate Function[3]	Functions[4]	Peripheral[5]	I/O Direction	Power Domain	Notes	Pin
SPLL_ANAVIZ	—	ALT0 ALT1 ALT2 ALT3	SPLL_ANAVIZ — — —	 — — —	 — — —	—	—	D9
TMPS_ANAVIZ	—	ALT0 ALT1 ALT2 ALT3	TMPS_ANAVIZ — — —	 — — —	 — — —	—	—	D1
SYS_XTALI	—	ALT0 ALT1 ALT2 ALT3	SYS_XTALI — — —	SysClock — — —	I — — —	SYS_PLL_AVDD	—	A9
SYS_XTALO	—	ALT0 ALT1 ALT2 ALT3	SYS_XTALO — — —	SysClock — — —	O — — —	SYS_PLL_AVDD	—	A10
$\overline{\text{MCS}}$	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	$\overline{\text{MCS0}}$ — — —	DRAM — — —	O — — —	VDD_IO_MEM	—	D18
$\overline{\text{MCAS}}$	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	$\overline{\text{MCAS}}$ — — —	DRAM — — —	O — — —	VDD_IO_MEM	—	A20
$\overline{\text{MRAS}}$	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	$\overline{\text{MRAS}}$ — — —	DRAM — — —	O — — —	VDD_IO_MEM	—	C19
MVREF	—	ALT0 ALT1 ALT2 ALT3	MVREF — — —	DRAM — — —	I — — —	VDD_IO_MEM	—	N19

Table 2. MPC5125 Pin Multiplexing (continued)

Pin	Pad I/O Control Register[1] and Offset[2]	Alternate Function[3]	Functions[4]	Peripheral[5]	I/O Direction	Power Domain	Notes	Pin
MDQ27	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	MDQ27 — — GPIO24	DRAM — — GPIO1	I/O — — I/O	VDD_IO_MEM	—	L21
MDQ28	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	MDQ28 — — GPIO25	DRAM — — GPIO1	I/O — — I/O	VDD_IO_MEM	—	K20
MDQ29	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	MDQ29 — — GPIO26	DRAM — — GPIO1	I/O — — I/O	VDD_IO_MEM	—	J22
MDQ30	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	MDQ30 — — GPIO27	DRAM — — GPIO1	I/O — — I/O	VDD_IO_MEM	—	J21
MDQ31	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	MDQ31 — — GPIO28	DRAM — — GPIO1	I/O — — I/O	VDD_IO_MEM	—	J20
MDM0	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	MDM0 — — —	DRAM — — —	O — — —	VDD_IO_MEM	—	Y19
MDM1	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	MDM1 — — —	DRAM — — —	O — — —	VDD_IO_MEM	—	V21
MDM2	0x00 IO_CON-TROL_MEM	ALT0 ALT1 ALT2 ALT3	MDM2 — — GPIO29	DRAM — — GPIO1	O — — I/O	VDD_IO_MEM	—	R22

Table 2. MPC5125 Pin Multiplexing (continued)

Pin	Pad I/O Control Register[1] and Offset[2]	Alternate Function[3]	Functions[4]	Peripheral[5]	I/O Direction	Power Domain	Notes	Pin
USB1_DATA6	0x69 STD_PU	ALT0 ALT1 ALT2 ALT3	USB1_DATA6 PSC4_1 FEC2_TXD_0/RMII_TX0 —	USB2 PSC4 FEC2	I/O I/O O —	VDD_IO	—	Y6
USB1_DATA7	0x6A STD_PU_ST	ALT0 ALT1 ALT2 ALT3	USB1_DATA7 PSC4_2 FEC2_TX_CLK/RMII_REF_CLK —	USB2 PSC4 FEC2	I/O I/O I —	VDD_IO	—	AB5
USB1_STOP	0x6B STD_PU_ST	ALT0 ALT1 ALT2 ALT3	USB1_STOP PSC4_3 FEC2_RX_CLK —	USB2 PSC4 FEC2	O I/O I —	VDD_IO	—	W6
USB1_CLK	0x6C STD_PU_ST	ALT0 ALT1 ALT2 ALT3	USB1_CLK PSC4_4 FEC2_RX_DV/RMII_CRS_DV —	USB2 PSC4 FEC2	I I/O I —	VDD_IO	—	Y8
USB1_NEXT	0x6D STD_PU	ALT0 ALT1 ALT2 ALT3	USB1_NEXT — FEC2_TX_EN/RMII_TX_EN GPIO09	USB2 — FEC2 GPIO1	I — O I/O	VDD_IO	—	AA5
USB1_DIR	0x6E STD_PU_ST	ALT0 ALT1 ALT2 ALT3	USB1_DIR — FEC2_COL GPIO10	USB2 — FEC2 GPIO1	I — I I/O	VDD_IO	—	W7
SDHC								
SDHC1_CLK	0x6F STD_PU	ALT0 ALT1 ALT2 ALT3	SDHC1_CLK NFC_CE1 FEC2_TXD_2 GPIO11	SDHC1 NFC FEC2 GPIO1	O O O I/O	VDD_IO	—	T1

Table 2. MPC5125 Pin Multiplexing (continued)

Pin	Pad I/O Control Register[1] and Offset[2]	Alternate Function[3]	Functions[4]	Peripheral[5]	I/O Direction	Power Domain	Notes	Pin
PSC0_2	0x78 STD_PU	ALT0 ALT1 ALT2 ALT3	PSC0_2 SDHC2_D1_IRQ GPT1[2] GPIO17	PSC0 SDHC2 GPT1 GPIO1	I/O I/O I/O I/O	VDD_IO	—	A13
PSC0_3	0x79 STD_PU	ALT0 ALT1 ALT2 ALT3	PSC0_3 SDHC2_D2 GPT1[3] GPIO18	PSC0 SDHC2 GPT1 GPIO1	I/O I/O I/O I/O	VDD_IO	—	B13
PSC0_4	0x7A STD_PU	ALT0 ALT1 ALT2 ALT3	PSC0_4 SDHC2_D3_CD GPT1[4] CAN1_TX	PSC0 SDHC2 GPT1 CAN1	I/O I/O I/O O	VDD_IO	—	D11
PSC1_0	0x7B STD_PU	ALT0 ALT1 ALT2 ALT3	PSC1_0 SDHC2_CLK GPT1[5] CAN2_TX	PSC1 SDHC2 GPT1 CAN2	I/O O O O	VDD_IO	—	C12
PSC1_1	0x7C STD_PU	ALT0 ALT1 ALT2 ALT3	PSC1_1 CAN_CLK GPT1[6] IRQ0	PSC1 GPT1	I/O I/O I	VDD_IO	—	C13
PSC1_2	0x7D STD_PU	ALT0 ALT1 ALT2 ALT3	PSC1_2 TPA2 GPT1[7] IRQ1	PSC1 GPT1	I/O I/O I	VDD_IO	—	B14
PSC1_3	0x7E STD_PU	ALT0 ALT1 ALT2 ALT3	PSC1_3 CKSTP_IN NFC_R/$\overline{B}$2 GPIO19	PSC1 NFC GPIO1	I/O I I/O	VDD_IO	—	D13
PSC1_4	0x7F STD_PU	ALT0 ALT1 ALT2 ALT3	PSC1_4 CKSTP_OUT NFC_CE2 GPIO20	PSC1 MFC GPIO1	I/O O I/O	VDD_IO	—	A15

4 Electrical and Thermal Characteristics

4.1 DC Electrical Characteristics

4.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5125 DC electrical characteristics. Table 4 gives the absolute maximum ratings.

Table 4. Absolute Maximum Ratings[1]

Characteristic	Sym	Min	Max	Unit	SpecID
Supply voltage — e300 core and peripheral logic	V_{DD}	–0.3	1.47	V	D1.1
Supply voltage — I/O buffers	V_{DD_IO}, $V_{DD\_IO\_MEM}$	–0.3	3.6	V	D1.2
Input reference voltage (DDR/DDR2)	MV_{REF}	–0.3	3.6	V	D1.15
Termination Voltage (DDR2)	MV_{TT}	–0.3	3.6	V	D1.16
Supply voltage — system APLL	AV_{DD_SPLL}	–0.3	3.6	V	D1.3
Supply voltage — system oscillator and temperature sensor	$AV_{DD\_OSC\_TMPS}$	–0.3	3.6	V	D1.4
Supply voltage — e300 APLL	AV_{DD_CPLL}	–0.3	3.6	V	D1.5
Supply voltage — RTC (hibernation)	V_{BAT}	–0.3	3.6	V	D1.6
Supply voltage — FUSE programming	AV_{DD_FUSEWR}	–0.3	3.6	V	D1.7
Input voltage (V_{DD_IO})	V_{in}	–0.3	V_{DD_IO} + 0.3	V	D1.9
Input voltage ($V_{DD\_IO\_MEM}$)	V_{in}	–0.3	$V_{DD\_IO\_MEM}$ + 0.3	V	D1.10
Input voltage (V_{BAT})	V_{in}	–0.3	V_{BAT} + 0.3	V	D1.11
Input voltage overshoot	V_{inos}	—	1	V	D1.12
Input voltage undershoot	V_{inus}	—	1	V	D1.13
Storage temperature range	T_{stg}	–55	150	°C	D1.14

NOTES:
1 Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

4.1.2 Recommended Operating Conditions

Table 5 gives the recommended operating conditions.

Table 5. Recommended Operating Conditions

Characteristic	Sym	Min[1]	Typ	Max[1]	Unit	SpecID
Supply voltage — e300 core and peripheral logic	V_{DD}	1.33	1.4	1.47	V	D2.1
State retention voltage — e300 core and peripheral logic [2]		1.08	—	—	V	D2.2

3 Doze, Nap, and Sleep power are measured with the e300 core in Doze/Nap/Sleep mode; the system oscillator, system PLL, and core PLL active; and all other system modules inactive.

4 Deep-sleep power is measured with the e300 core in Sleep mode. The system oscillator, system PLL, core PLL, and other system modules are inactive.

5 PLL power is measured at AV_{DD_SPLL} = AV_{DD_CPLL} = $AV_{DD\_OSC\_TMPS}$ = 3.3 V, T_J = 25 °C.

6 Unloaded typical I/O power is measured at V_{DD_IO} = 3.3 V, $V_{DD\_MEM\_IO}$ = 1.8 V, T_J = 25 °C.

NOTE

The maximum power depends on the supply voltage, process corner, junction temperature, and the concrete application and clock configurations.

4.1.6 Thermal Characteristics

Table 11. Thermal Resistance Data[1]

Rating	Conditions	Sym	Value	Unit	SpecID
Thermal resistance junction-to-ambient natural convection[2]	Single layer board – 1s	$R_{\theta JA}$	35	°C/W	D6.1
Thermal resistance junction-to-ambient natural convection[2]	Four layer board – 2s2p	$R_{\theta JA}$	25	°C/W	D6.2
Thermal resistance junction-to-moving-air ambient[2]	@ 200 ft./min., single layer board – 1s	$R_{\theta JMA}$	29	°C/W	D6.3
Thermal resistance junction-to-moving-air ambient[2]	@ 200 ft./min., four layer board 2s2p	$R_{\theta JMA}$	22	°C/W	D6.4
Thermal resistance junction-to-board[3]	—	$R_{\theta JB}$	16	°C/W	D6.5
Thermal resistance junction-to-case[4]	—	$R_{\theta JC}$	11	°C/W	D6.6
Junction-to-package-top natural convection[5]	Natural convection	Ψ_{JT}	3	°C/W	D6.7

NOTES:

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J, can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 3}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in package (W)

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The e300 core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The e300 core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

4.2.1 System Oscillator Electrical Characteristics

Table 12. System Oscillator Electrical Characteristics

Characteristic	Sym	Min	Typical	Max	Unit	SpecID
SYS_XTAL frequency	f_{sys_xtal}	15.6	33.3	35.0	MHz	O1.1

The system oscillator can work in oscillator mode or in bypass mode to support an external input clock as clock reference.

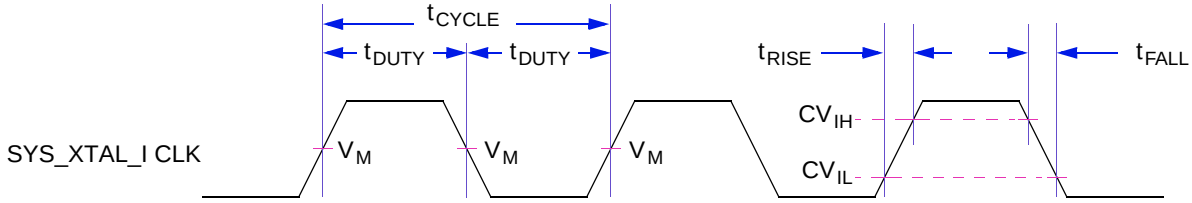


Figure 4. Timing Diagram — SYS_XTAL_IN

Table 13. SYS_XTAL_IN Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTALI cycle time[1,2]	64.1	28.57	ns	O.1.2
t_{RISE}	SYS_XTALI rise time[3]	1	4	ns	O.1.3
t_{FALL}	SYS_XTALI fall time[4]	1	4	ns	O.1.4
t_{DUTY}	SYS_XTALI duty cycle (measured at V_M)[5]	40	60	%	O.1.5

NOTES:
1. The SYS_XTALI frequency and system PLL settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the *MPC5125 Reference Manual* (MPC5125RM).
2. The min/max cycle times are calculated using $1/f_{sys\_xtal\ (MIN/MAX)}$ where the $f_{sys\_xtal\ (MIN/MAX)}$ (15.6 / 35 MHz) are taken from Table 12 (system oscillator electrical characteristics).
3. Rise time is measured from 20% of VDD to 80% of VDD.
4. Fall time is measured from 20% of VDD to 80% of VDD.
5. SYS_XTALI duty cycle is measured at V_M.

4.2.2 RTC Oscillator Electrical Characteristics

Table 14. RTC Oscillator Electrical Characteristics

Characteristic	Sym	Min	Typical	Max	Unit	SpecID
RTC_XTAL frequency	f_{rtc_xtal}	—	32.768	—	kHz	O2.1

Table 22. MobileDDR/LPDDR SDRAM Timing Specifications (continued)

At recommended operating conditions with $V_{DD\_IO\_MEM}$ of ±5%

Parameter	Symbol	Min	Max	Unit	Notes	SpecID
Address and control output hold time relative to MCK rising edge	$t_{OH(base)}$	$t_{CK}/2 - 1000$	—	ps	2,3	A5.7
DQ and DM output setup time relative to DQS	$t_{DS1(base)}$	$t_{CK}/4 - 750$	—	ps	2,3	A5.8
DQ and DM output hold time relative to DQS	$t_{DH1(base)}$	$t_{CK}/4 - 750$	—	ps	2,3	A5.9
DQS-DQ skew for DQS and associated DQ inputs	t_{DQSQ}	$-(t_{CK}/4 - 600)$	$t_{CK}/4 - 600$	ps	3	A5.10
DQS window position related to CAS read command	t_{DQSEN}	$2t_{CK} - 500$	$3t_{CK} - 1000$	ps	1,2,3,4,5	A5.11

NOTES:
1. Measured with clock pin loaded with differential 100 Ω termination resistor.
2. Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_IO\_MEM}/2$.
3. All transitions measured at mid-supply ($V_{DD\_IO\_MEM}/2$).
4. In this window, the first rising edge of DQS should occur. From the start of the window to DQS rising edge, DQS should be low.
5. The window position is given for $t_{DQSEN} = 2.0\ t_{CK}$ (RDLY = 2, HALF DQS DLY = QUART DQS DLY = 0) with CL = 3 MobileDDR/LPDDR SDRAM device. For other values of t_{DQSEN}, the window position is shifted accordingly.

4.3.5.3 DDR2 SDRAM AC Timing Specifications

Table 23. DDR2 (DDR2-400) SDRAM Timing Specifications

At recommended operating conditions with $V_{DD\_IO\_MEM}$ of ±5%

Parameter	Symbol	Min	Max	Unit	Notes	SpecID
Clock cycle time, CL = x	t_{CK}	5000	—	ps		A5.1
MCK AC differential crosspoint voltage	V_{OX-AC}	$(V_{DD\_IO\_MEM} \times 0.5) - 0.1$	$(V_{DD\_IO\_MEM} \times 0.5) + 0.1$	V	1	A5.2
CK HIGH pulse width	t_{CH}	0.47	0.53	t_{CK}	1,3	A5.3
CK LOW pulse width	t_{CL}	0.47	0.53	t_{CK}	1,3	A5.4
Skew between MCK and DQS transitions	t_{DQSS}	–0.25	0.25	t_{CK}	2,3	A5.5
Address and control output setup time relative to MCK rising edge	$t_{OS(base)}$	$t_{CK}/2 - 750$	—	ps	2,3	A5.6
Address and control output hold time relative to MCK rising edge	$t_{OH(base)}$	$t_{CK}/2 - 750$	—	ps	2,3	A5.7
DQ and DM output setup time relative to DQS	$t_{DS1(base)}$	$t_{CK}/4 - 500$	—	ps	2,3	A5.8
DQ and DM output hold time relative to DQS	$t_{DH1(base)}$	$t_{CK}/4 - 500$	—	ps	2,3	A5.9
DQS-DQ skew for DQS and associated DQ inputs	t_{DQSQ}	$-(t_{CK}/4 - 600)$	$t_{CK}/4 - 600$	ps	3	A5.10
DQS window position related to CAS read command	t_{DQSEN}	$2.5t_{CK}$	$3t_{CK} + 1500$	ps	1,2,3,4,5	A5.11

NOTES:
1. Measured with clock pin loaded with differential 100 Ω termination resistor.
2. Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_IO\_MEM}/2$.
3. All transitions measured at mid-supply ($V_{DD\_IO\_MEM}/2$).
4. In this window, the first rising edge of DQS should occur. From the start of the window to DQS rising edge, DQS should be low.
5. The window position is given for t_{DQSEN} = 2.5 t_{CK} (RDLY = 2, HALF DQS DLY = 1, QUART DQS DLY = 0) with CL = 3 DDR2 SDRAM device. For other values of t_{DQSEN}, the window position is shifted accordingly.

4.3.5.4 SDR SDRAM AC Timing Specifications

Table 24. SDR SDRAM Timing Specifications

At recommended operating conditions with $V_{DD\_IO\_MEM}$ of ±5%

Parameter	Symbol	Min	Max	Unit	Notes	SpecID
Clock cycle time, CL = x	t_{CK}	7500	—	ps		A5.1
CK HIGH pulse width	t_{CH}	0.43	0.57	t_{CK}	1,3	A5.3
CK LOW pulse width	t_{CL}	0.43	0.57	t_{CK}	1,3	A5.4
Address, control, and data output setup time relative to MCK rising edge	$t_{OS(base)}$	$t_{CK}/2 – 1000$	—	ps	2,3	A5.6
Address, control, and data output hold time relative to MCK rising edge	$t_{OH(base)}$	$t_{CK}/2 – 1000$	—	ps	2,3	A5.7
Input data set-up time, relative to MCK	t_{IS}	1000	—	ps	3	A5.15
Input data hold time, relative to MCK	t_{IH}	1000	—	ps	3	A5.16

NOTES:
1. Measured with clock pin loaded with 50 Ω termination resistor to mid-supply.
2. Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_IO\_MEM}/2$.
3. All transitions measured at mid-supply ($V_{DD\_IO\_MEM}/2$).

NOTE

To achieve better timing, balance the loading of DQS as MCK although DQS is not used in SDR mode.

Figure 9 shows the DDR SDRAM write timing.

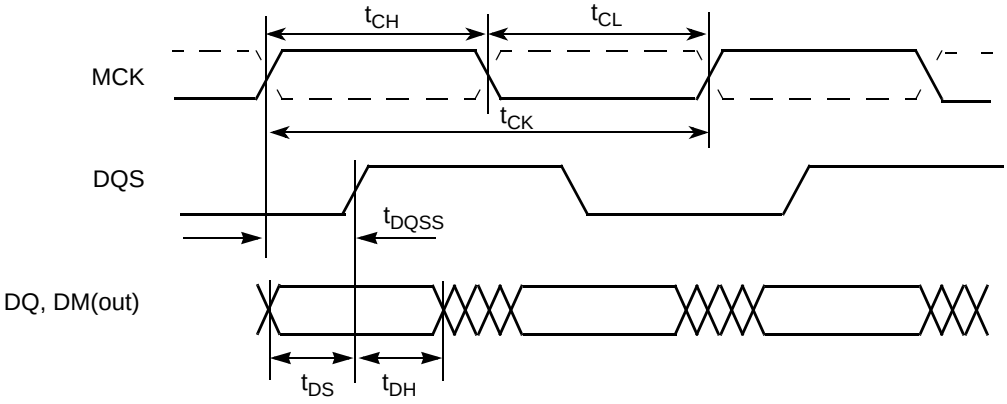


Figure 9. DDR Write Timing

4.3.6.2 MUXed Mode

4.3.6.2.1 MUXed Non-Burst Mode

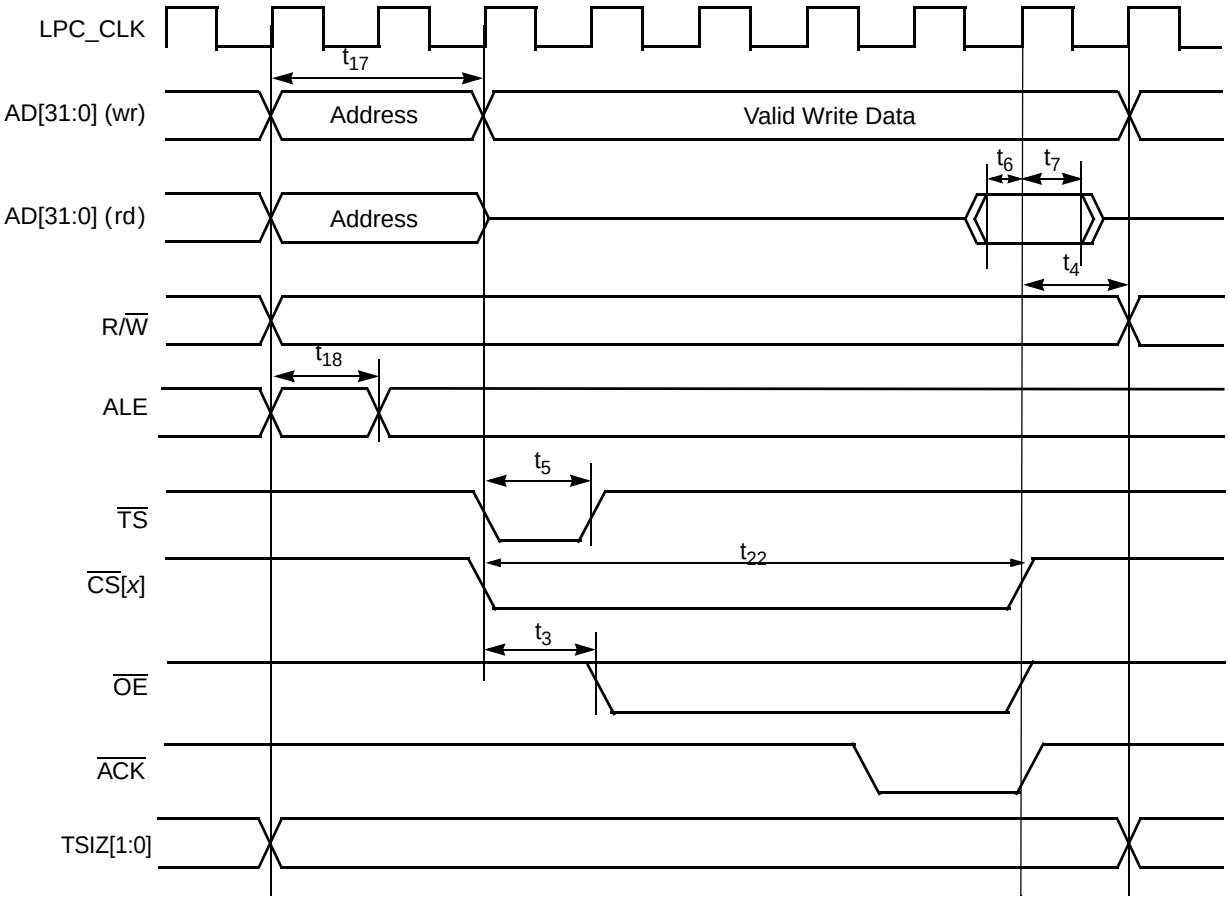


Figure 19. Timing Diagram — MUXed non-Burst Mode

NOTE

ACK is asynchronous input signal and has no timing requirements. ACK needs to be deasserted after CS[x] is deasserted.

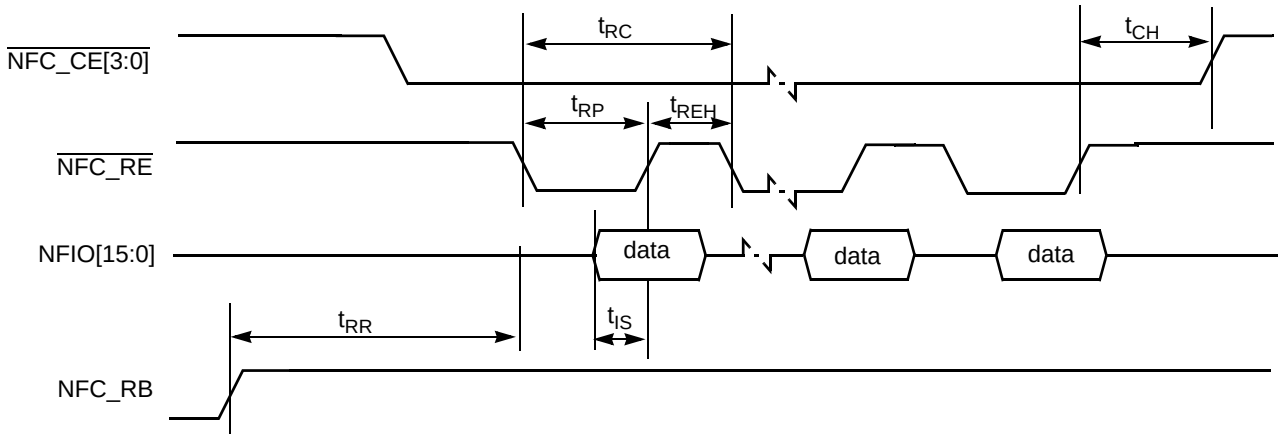


Figure 25. Read Data Latch Timing in Non-Fast Mode

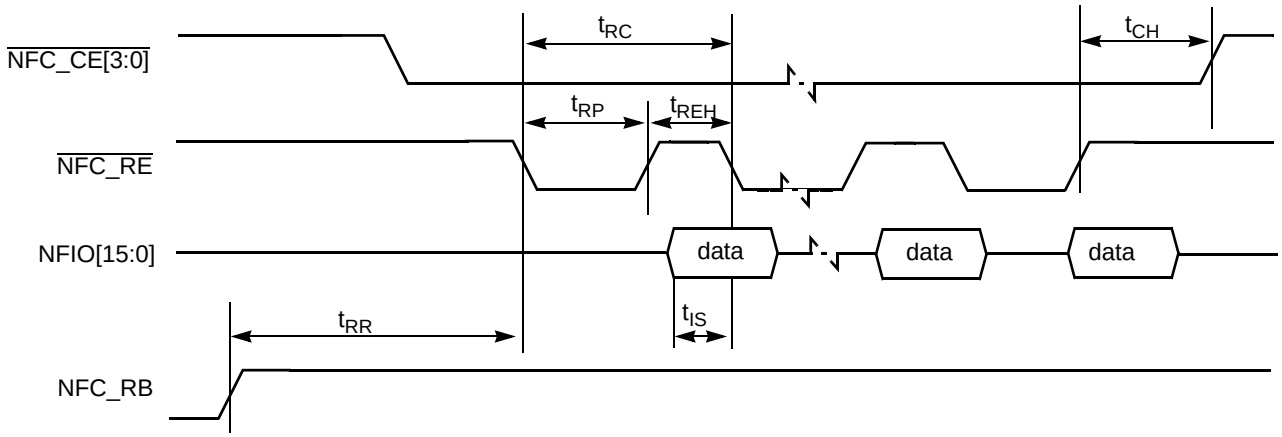


Figure 26. Read Data Latch Timing in Fast Mode

4.3.8 FEC

AC test timing conditions:

- Output Loading
  All Outputs: 25 pF

Table 27. MII Rx Signal Timing

Sym	Description	Min	Max	Unit	SpecID
t_1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns	A11.1
t_2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns	A11.2
t_3	RX_CLK pulse width high	35%	65%	RX_CLK period[1]	A11.3
t_4	RX_CLK pulse width low	35%	65%	RX_CLK period[1]	A11.4

NOTES:
1 RX_CLK shall have a frequency of 25% of the data rate of the received signal. See the IEEE 802.3 specification.

Table 35. LCD Interface Timing Parameters — Pixel Level

Sym	Description	Value	Unit	SpecID
t_{FPH}	HSYNC Front Porch Width	FP_H × t_{PCP}	ns	A15.4
t_{SW}	Screen Width	DELTA_X × t_{PCP}	ns	A15.5
t_{HSP}	HSYNC (Line) Period	(PW_H + BP_H + DELTA_X + FP_H) × t_{PCP}	ns	A15.6
t_{PWV}	VSYNC Pulse Width	PW_V × t_{HSP}	ns	A15.7
t_{BPV}	VSYNC Back Porch Width	BP_V × t_{HSP}	ns	A15.8
t_{FPV}	VSYNC Front Porch Width	FP_V × t_{HSP}	ns	A15.9
t_{SH}	Screen Height	DELTA_Y × t_{HSP}	ns	A15.10
t_{VSP}	VSYNC (Frame) Period	(PW_V + BP_V + DELTA_Y + FP_H) × t_{HSP}	ns	A15.11

NOTES:
1 Display interface pixel clock period immediate value (in nanoseconds).

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register; The PW_H, BP_H, and FP_H parameters are programmed via the HSYN_PARA register; and the PW_V, BP_V, and FP_V parameters are programmed via the VSYN_PARA register. See appropriate section in the reference manual for detailed descriptions of these parameters.

Figure 36 depicts the synchronous display interface timing for access level, and Table 36 lists the timing parameters.

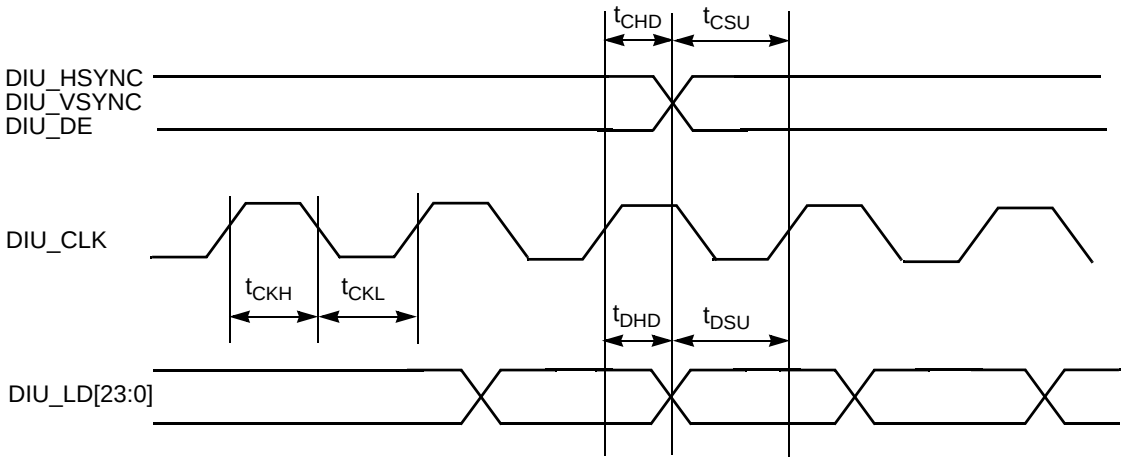


Figure 36. LCD Interface Timing Diagram — Access Level

Table 36. LCD Interface Timing Parameters — Access Level

Parameter	Description	Min	Typ	Max	Unit	SpecID
t_{CKH}	LCD interface pixel clock high time	t_{PCP} × 0.4	t_{PCP} × 0.5	t_{PCP} × 0.6	ns	A15.12
t_{CKL}	LCD interface pixel clock low time	t_{PCP} × 0.4	t_{PCP} × 0.5	t_{PCP} × 0.6	ns	A15.13
t_{DSU}	LCD interface data setup time	5.0	—	—	ns	A15.14
t_{DHD}	LCD interface data hold time	6.0	—	—	ns	A15.15
t_{CSU}	LCD interface control signal setup time	5.0	—	—	ns	A15.16
t_{CHD}	LCD interface control signal hold time	6.0	—	—	ns	A15.17

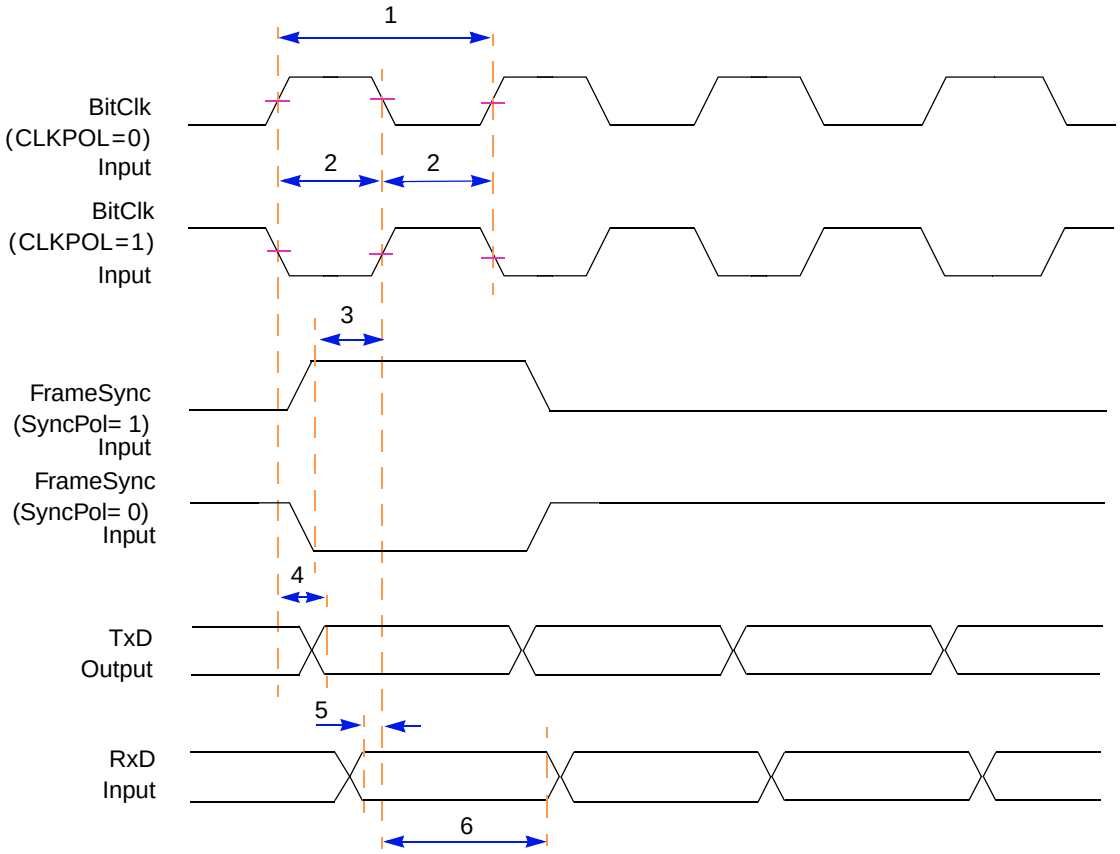


Figure 39. Timing Diagram — 8-,16-, 24-, and 32-bit CODEC/I^{2}S Slave Mode

4.3.15.2 AC97 Mode

Table 41. Timing Specifications — AC97 Mode [1]

Sym	Description	Min	Typ	Max	Units	SpecID
1	Bit clock cycle time	—	81.4	—	ns	A20.15
2	Clock pulse high time	—	40.7	—	ns	A20.16
3	Clock pulse low time	—	40.7	—	ns	A20.17
4	Frame sync valid after rising clock edge	—	—	13.0	ns	A20.18
5	Output data valid after rising clock edge	—	—	14.0	ns	A20.19
6	Input data setup time	1.0	—	—	ns	A20.20
7	Input data hold time	1.0	—	—	ns	A20.21

NOTES:
1 Output timing is specified at a nominal 50 pF load.

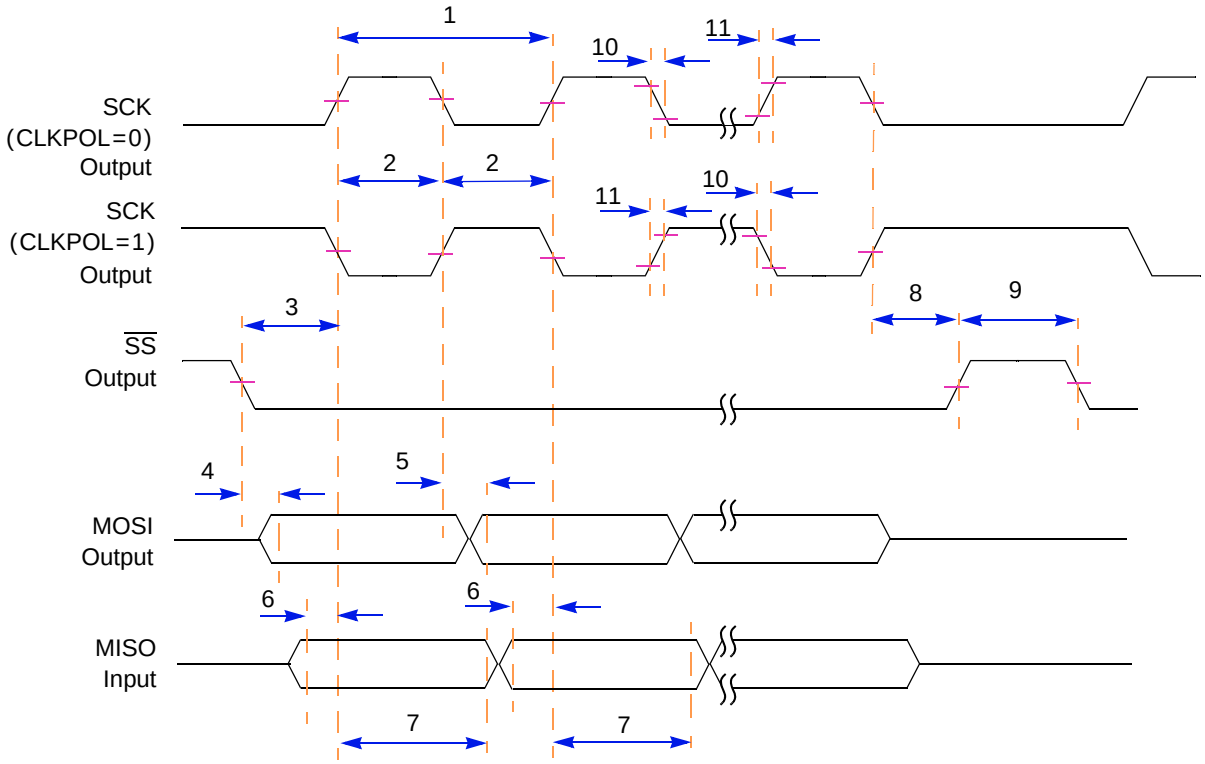


Figure 41. Timing Diagram — SPI Master Mode, Format 0 (CPHA = 0)

Table 43. Timing Specifications — SPI Slave Mode, Format 0 (CPHA = 0) [1]

Sym	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.37
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.38
3	Slave select clock delay	1.0	—	ns	A20.39
4	Input data setup time	1.0	—	ns	A20.40
5	Input data hold time	1.0	—	ns	A20.41
6	Output data valid after $\overline{SS}$	—	14.0	ns	A20.42
7	Output data valid after SCK	—	14.0	ns	A20.43
8	Slave disable lag time	0.0	—	ns	A20.44
9	Minimum sequential transfer delay = 2 × IP bus clock cycle time	30.0	—	—	A20.45

NOTES:
1 Output timing is specified at a nominal 50 pF load.

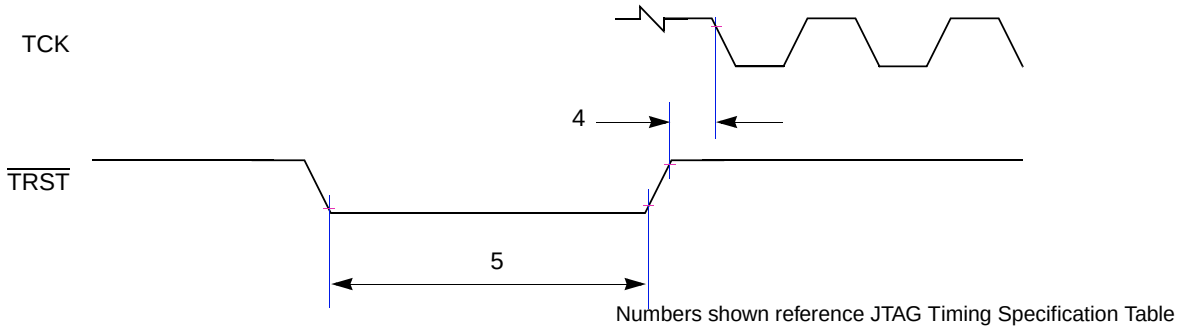


Figure 46. Timing Diagram — JTAG TRST

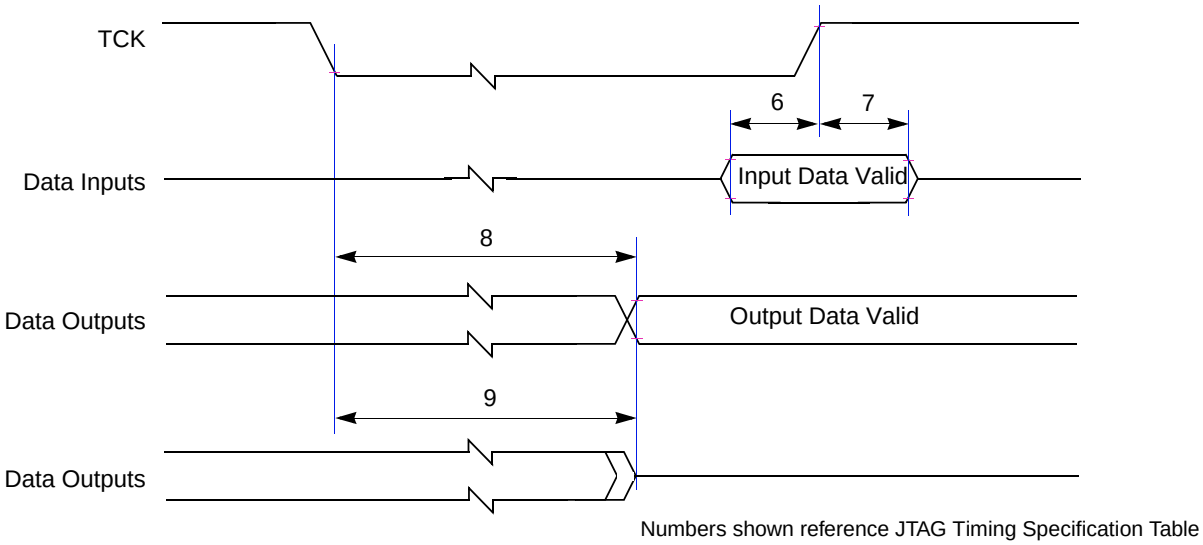


Figure 47. Timing Diagram — JTAG Boundary Scan

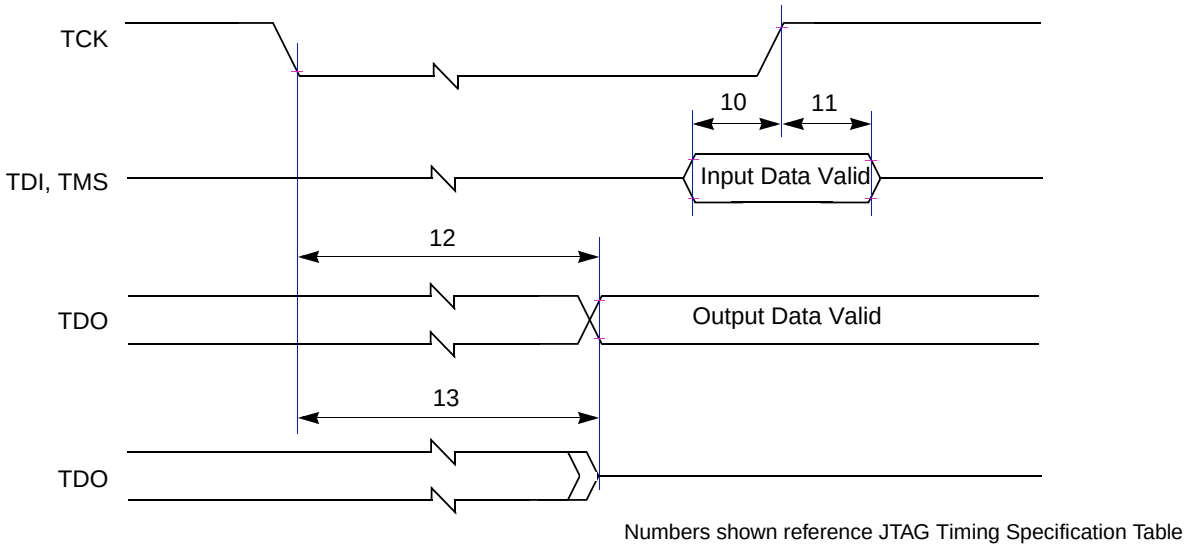


Figure 48. Timing Diagram — Test Access Port

Table 49. COP/BDM Interface Signals

BDM Pin #	I/O Pin	BDM Connector	Internal Pullup/Pulldown	External Pullup/Pulldown	I/O[1]
16	—	GND	—	—	—
15	$\overline{\text{CKSTP\_OUT}}$	ckstp_out	—	10 kΩ Pullup	I
14	—	KEY	—	—	—
13	$\overline{\text{HRESET}}$	hreset	Pullup	10 kΩ Pullup	O
12	—	GND	—	—	—
11	$\overline{\text{SRESET}}$	sreset	Pullup	10 kΩ Pullup	O
10	—	N/C	—	—	—
9	TMS	tms	Pullup	10 kΩ Pullup	O
8	$\overline{\text{CKSTP\_IN}}$	ckstp_in	—	10 kΩ Pullup	O
7	TCK	tck	Pullup	10 kΩ Pullup	O
6	—	VDD[2]	—	—	—
5	See Note[3]	halted[3]	—	—	I
4	$\overline{\text{TRST}}$	trst	Pullup	10 kΩ Pullup	O
3	TDI	tdi	Pullup	10 kΩ Pullup	O
2	See Note^{pci_frame}	qack[4]	—	—	O
1	TDO	tdo	—	—	I

NOTES:
1. With respect to the emulator tool's perspective:
   Input is really an output from the embedded e300 core.
   Output is really an input to the core.
2. From the board under test, power sense for chip power.
3. HALTED is not available from e300 core.

For a board with a COP (common on-chip processor) connector that accesses the JTAG interface and needs to reset the JTAG module, it is not recommended to wire only $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$.

To reset the MPC5125 via the COP connector, the $\overline{\text{HRESET}}$ pin of the COP should be connected to the $\overline{\text{HRESET}}$ pin of the MPC5125. The circuitry shown in Figure 51 allows the COP to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ separately, while any other board sources can drive $\overline{\text{PORESET}}$.

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23840W
		PAGE: 1158
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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. PACKAGE CODES:
   5241: 2 LAYER 324 PBGA
   5366: 4 LAYER 324 TEPBGA PGE

TITLE:	PBGA, 324 I/O, 23 X 23 PKG, 1 MM PITCH (OMPAC)	CASE NUMBER: 1158–03	
		STANDARD: JEDEC MS–034 AAJ–1	
		PACKAGE CODE: NOTE 6	SHEET: 2

Figure 54. Mechanical Drawing of MPC5125 PBGA (2 of 3)

7 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com .

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

- *MPC5125 Microprocessor Reference Manual* (document number MPC5125RM)
- *MPC5125 (0M01S) Errata* (document number MSE5125_0M01S)