Renesas Electronics America Inc - R7FS3A6783A01CFM#AA0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 18x14b; D/A 3x8b, 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a6783a01cfm-aa0

Table 1.7 Communication interfaces (2 of 2)

Feature	Functional description
USB 2.0 Full-Speed Module (USBFS)	The USB 2.0 Full-Speed Module (USBFS) can operate as a host controller or device controller. The module supports full-speed and low-speed (only for the host controller) transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on the user system. The MCU supports revision 1.2 of the Battery Charging specification. Because the MCU can be powered at 5 V, the USB LDO regulator provides the internal USB transceiver power supply at 3.3 V. See section 27, USB 2.0 Full-Speed Module (USBFS) in User's Manual.

Table 1.8 Analog

Feature	Functional description
14-bit A/D Converter (ADC14)	A 14-bit successive approximation A/D converter is provided. Up to 25 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 35, 14-Bit A/D Converter (ADC14) in User's Manual.
12-Bit D/A Converter (DAC12)	The 12-Bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 36, 12-Bit D/A Converter (DAC12) in User's Manual.
8-Bit D/A Converter (DAC8) for ACMPLP	The 8-Bit D/A Converter (DAC8) converts data and does not include an output amplifier (DAC8). The DAC8 is used only as the reference voltage for ACMPLP. See section 40, 8-Bit D/A Converter (DAC8) in User's Manual.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC14 for conversion and can be further used by the end application. See section 37, Temperature Sensor (TSN) in User's Manual.
Low-Power Analog Comparator (ACMPLP)	The Low-Power Analog Comparator (ACMPLP) compares the reference input voltage and analog input voltage. The comparison result can be read through software and also be output externally. The reference voltage can be selected from an input to the CMPREFi(i = 0,1) pin, an internal 8-bit D/A converter output, or the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting the high-speed mode decreases the response delay time, but increases current consumption. Setting the low-speed mode increases the response delay time, but decreases current consumption. See section 39, Low-Power Analog Comparator (ACMPLP) in User's Manual.
Operational Amplifier (OPAMP)	The Operational Amplifier (OPAMP) amplifies small analog input voltages and outputs the amplified voltages. A total of four differential operational amplifier units with two input pins and one output pin are provided. See section 38, Operational Amplifier (OPAMP) in User's Manual.

Table 1.9 Human machine interfaces

Feature	Functional description
Segment LCD Controller (SLCDC)	The Segment LCD Controller (SLCDC) provides the following functions: • Waveform A or B selectable • The LCD driver voltage generator can switch between an internal voltage boosting method, a capacitor split method, and an external resistance division method • Automatic output of segment and common signals based on automatic display data register read • The reference voltage generated when operating the voltage boost circuit can be selected in 16 steps (contrast adjustment) • The LCD can be made to blink. See section 45, Segment LCD Controller (SLCDC) in User's Manual.
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed within an electrical insulator so that fingers do not come into direct contact with the electrode. See section 41, Capacitive Touch Sensing Unit (CTSU) in User's Manual.

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

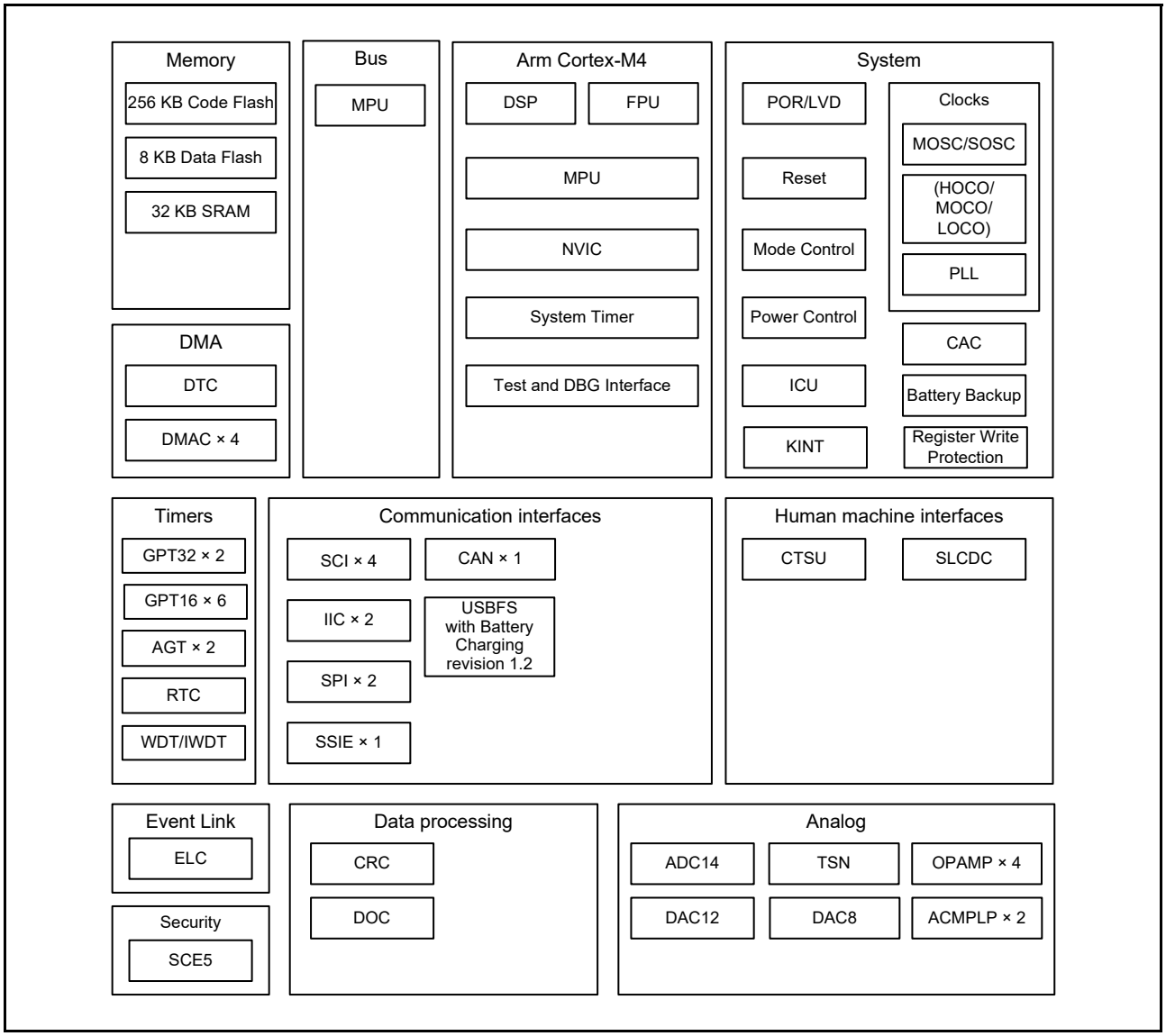


Figure 1.1 Block diagram

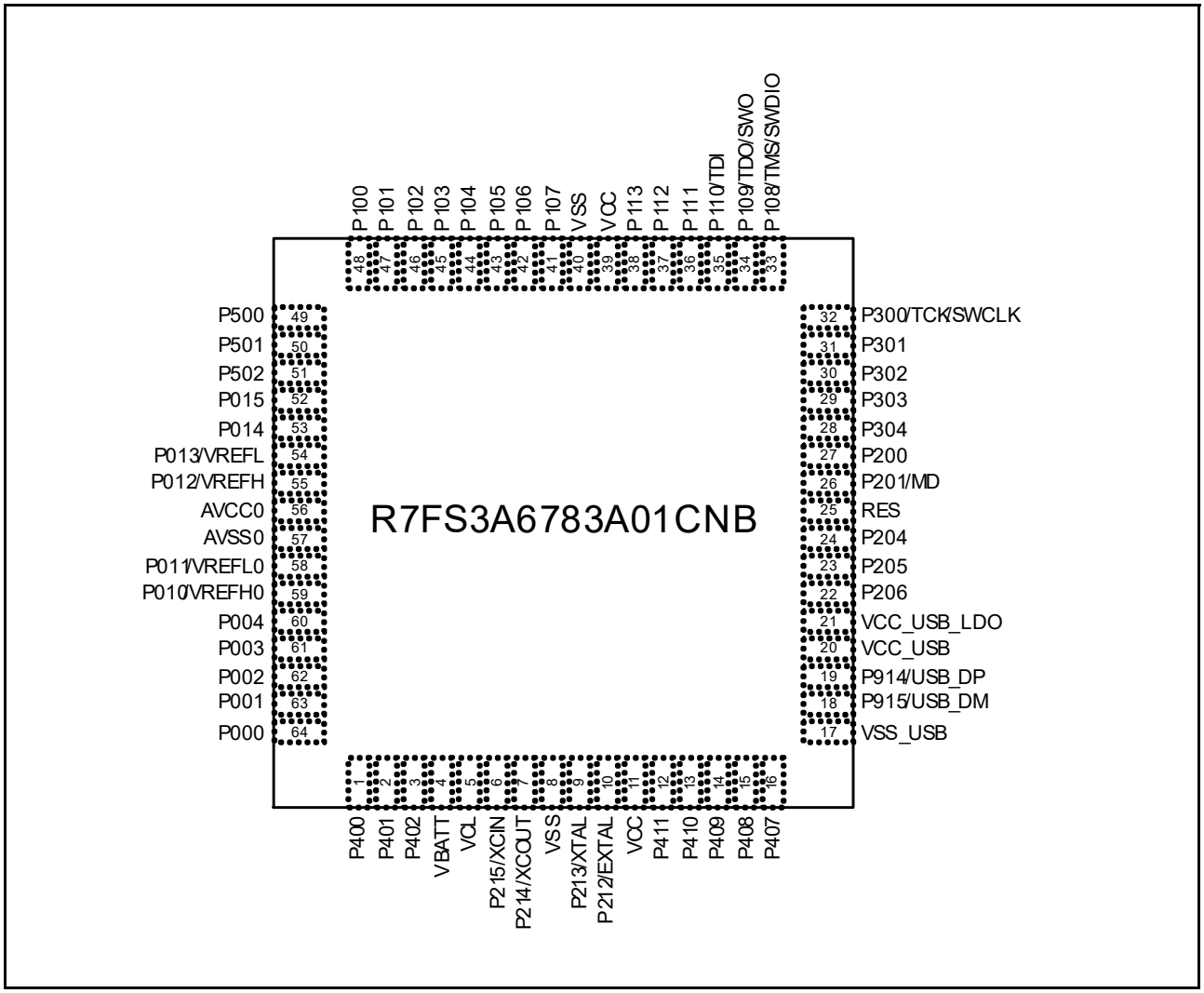


Figure 1.6 Pin assignment for 64-pin QFN (upper perspective view)

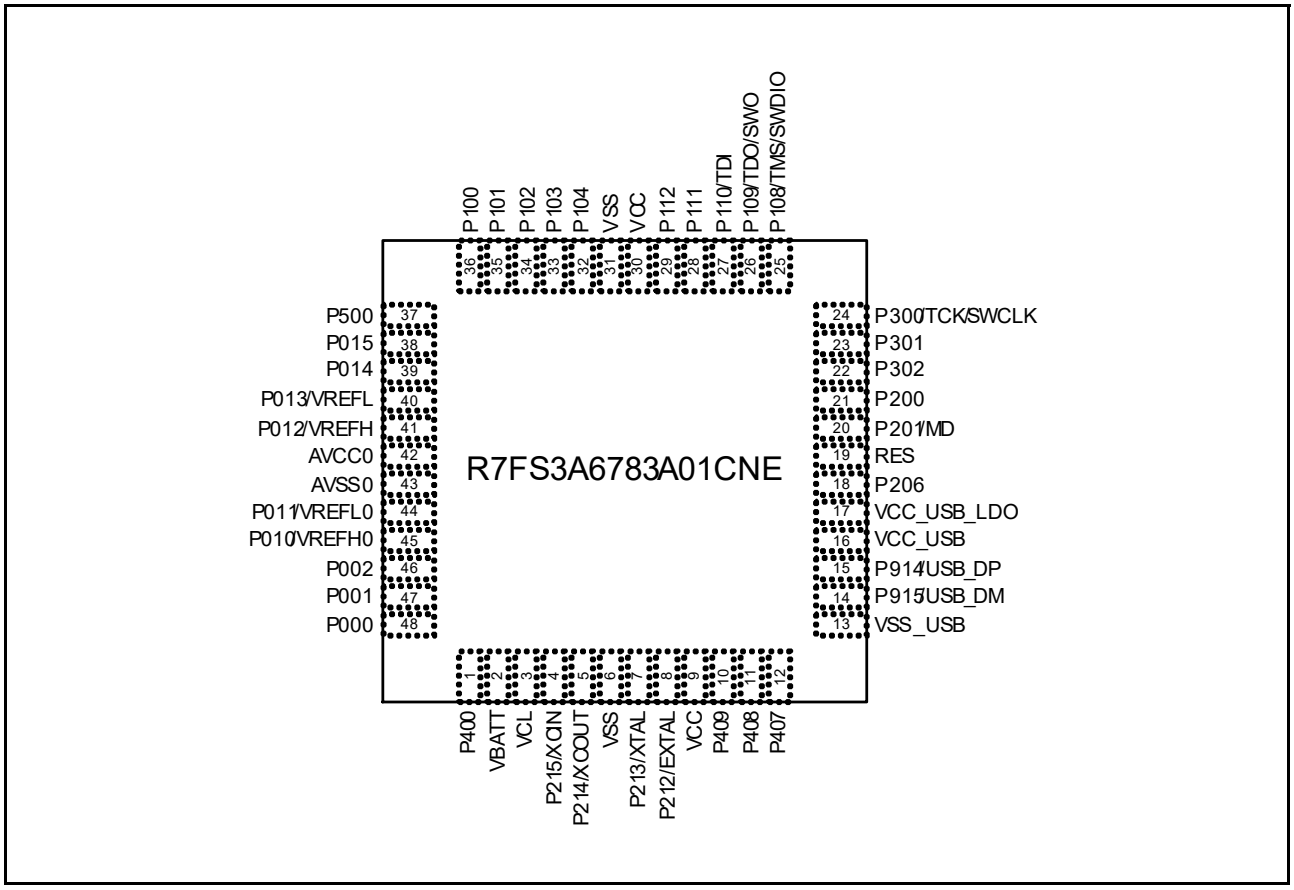


Figure 1.8 Pin assignment for 48-pin QFN (top view)

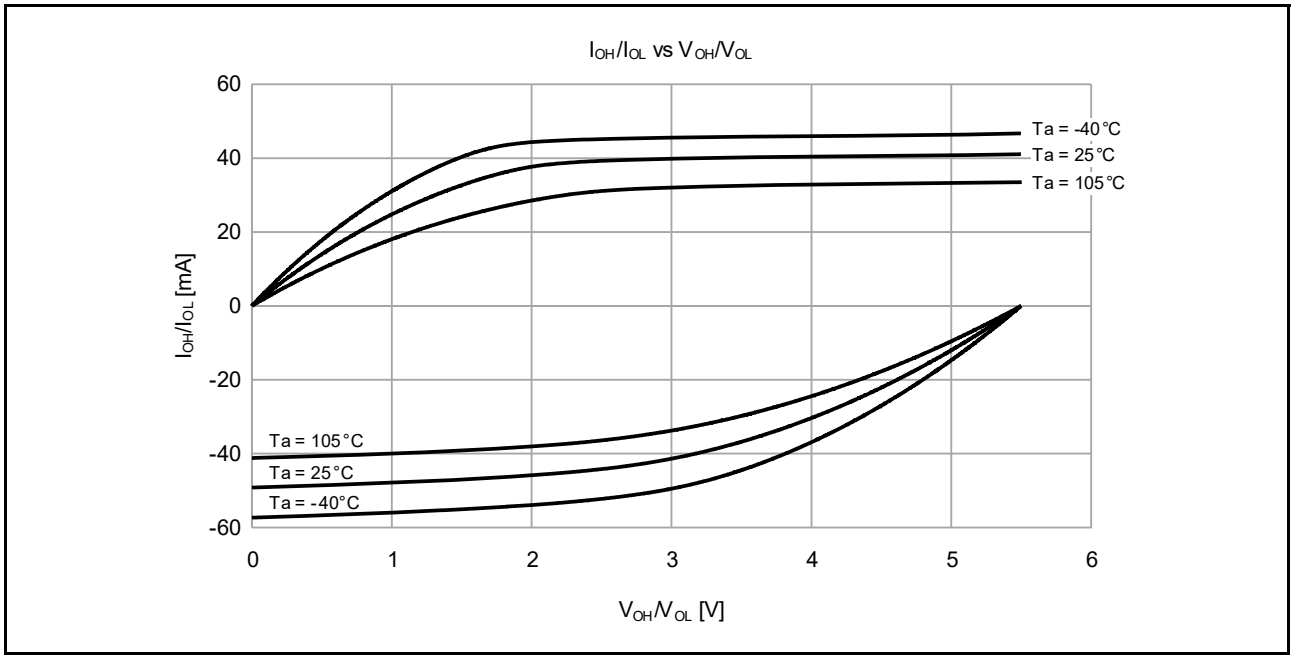


Figure 2.6 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 5.5 V when low drive output is selected (reference data)**

2.2.6 I/O Pin Output Characteristics of Middle Drive Capacity

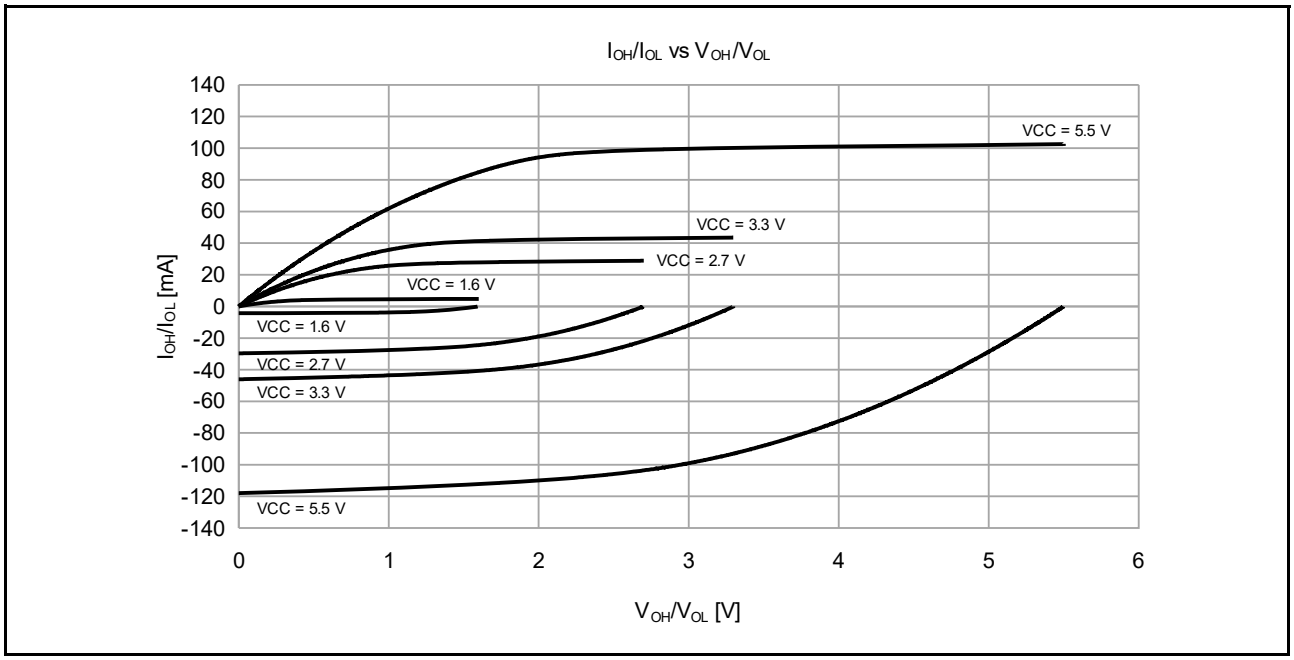
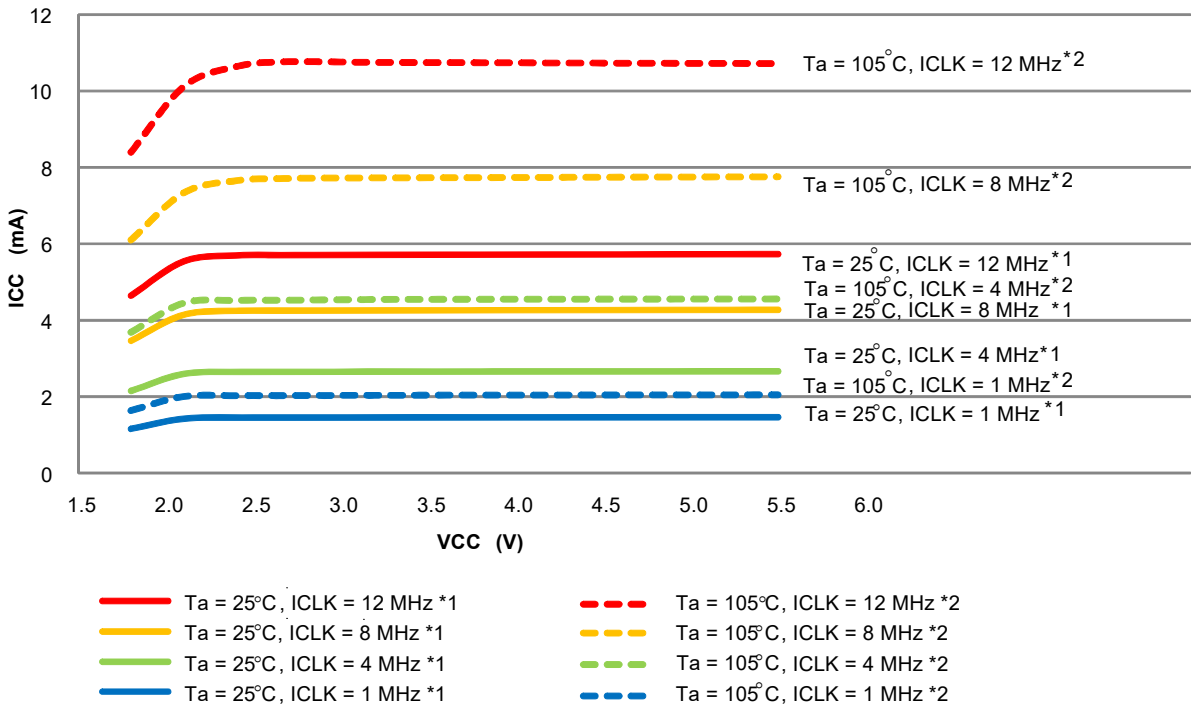


Figure 2.7 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at T_a = 25°C when middle drive output is selected (reference data)**



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

Figure 2.18 Voltage dependency in middle-speed operating mode (reference data)

Table 2.14 Operating and standby current (4)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V, VREFH0 = 2.7 V to AVCC0

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During A/D conversion (at high-speed conversion)		I_{AVCC}	-	-	3.0	mA	-
	During A/D conversion (at low-power conversion)			-	-	1.0	mA	-
	During D/A conversion (per channel)*1			-	0.4	0.8	mA	-
	Waiting for A/D and D/A conversion (all units)*6			-	-	1.0	µA	-
Reference power supply current	During A/D conversion		I_{REFH0}	-	-	150	µA	-
	Waiting for A/D conversion (all units)			-	-	60	nA	-
	During D/A conversion		I_{REFH}	-	50	100	µA	-
	Waiting for D/A conversion (all units)			-	-	100	µA	-
Temperature sensor			I_{TNS}	-	75	-	µA	-
Low-Power Analog Comparator operating current	Window mode		I_{CMPLP}	-	15	-	µA	-
	Comparator High-speed mode			-	10	-	µA	-
	Comparator Low-speed mode			-	2	-	µA	-
	Comparator Low-speed mode using DAC8			-	820	-	µA	-
Operational Amplifier operating current	Low power mode	1 unit operating	I_{AMP}	-	2.5	4.0	µA	-
		2 units operating		-	4.5	8.0	µA	-
		3 units operating		-	6.5	11.0	µA	-
		4 units operating		-	8.5	14.0	µA	-
	High-speed mode	1 unit operating		-	140	220	µA	-
		2 units operating		-	280	410	µA	-
		3 units operating		-	420	600	µA	-
		4 units operating		-	560	780	µA	-
LCD operating current	External resistance division method $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice		I_{LCD1}*5	-	0.34	-	µA	-
	Internal voltage boosting method (VLCD.VLCD = 04) $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice		I_{LCD2}*5	-	0.92	-	µA	-
	Capacitor split method $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice		I_{LCD3}*5	-	0.19	-	µA	-
USB operating current	During USB communication operation under the following settings and conditions: • Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect peripheral devices via a 1-meter USB cable from the USB port.		I_{USBH}*2	-	4.3 (VCC) 0.9 (VCC_USB)*4	-	mA	-
	During USB communication operation under the following settings and conditions: • Device controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect the host device via a 1-meter USB cable from the USB port.		I_{USBF}*2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-
	During suspended state under the following setting and conditions: • Device controller operation is set to full-speed mode (pull up the USB_DP pin) • Software standby mode • Connect the host device via a 1-meter USB cable from the USB port.		I_{SUSP}*3	-	0.35 (VCC) 170 (VCC_USB)*4	-	µA	-

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. Current consumed only by the USBFS.
Note 3. Includes the current supplied from the pull-up resistor of the USB_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU during the suspended state.
Note 4. When VCC = VCC_USB = 3.3 V.
Note 5. Current flowing only to the LCD controller. Not including the current that flows through the LCD panel.
Note 6. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC140 module stop bit) is in the module-stop state.

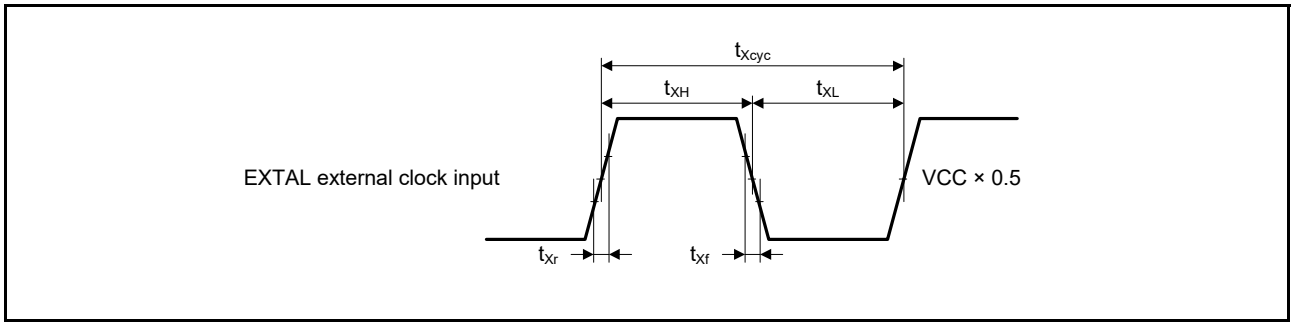


Figure 2.25 EXTAL external clock input timing

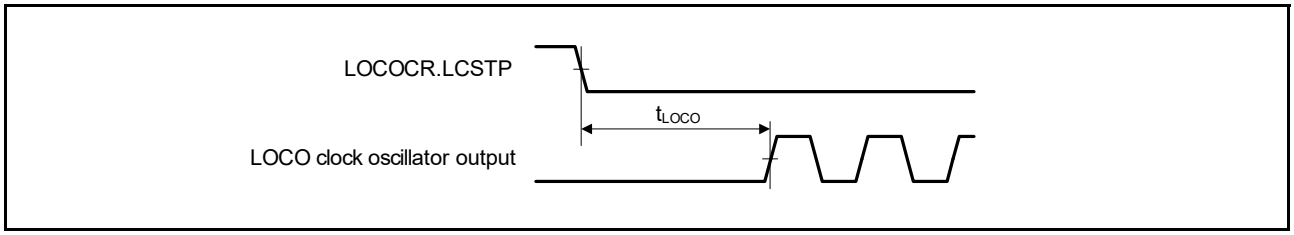


Figure 2.26 LOCO clock oscillation start timing

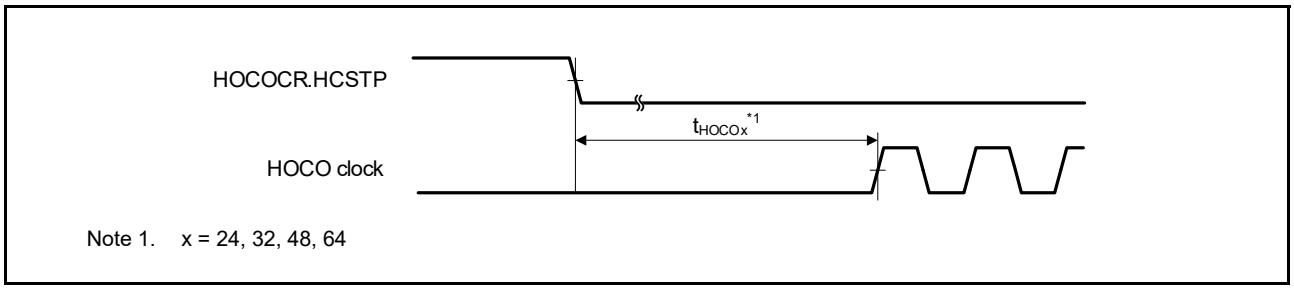


Figure 2.27 HOCO clock oscillation start timing (started by setting HOCOCR.HCSTP bit)

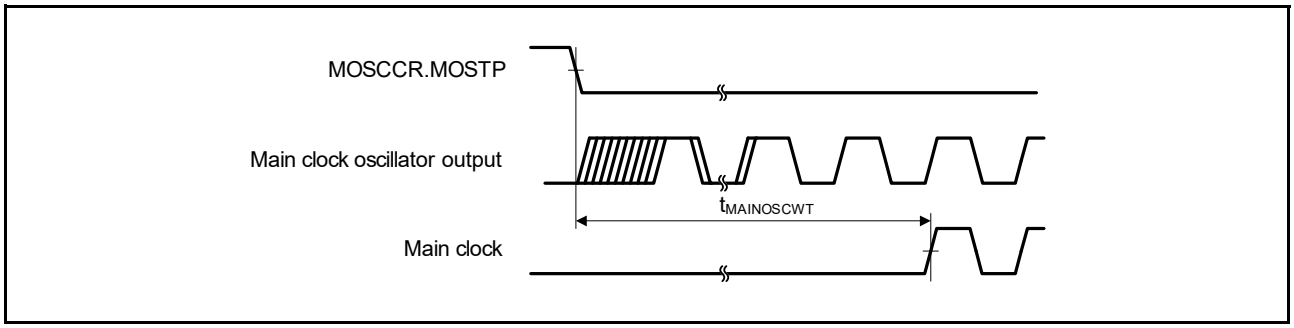


Figure 2.28 Main clock oscillation start timing

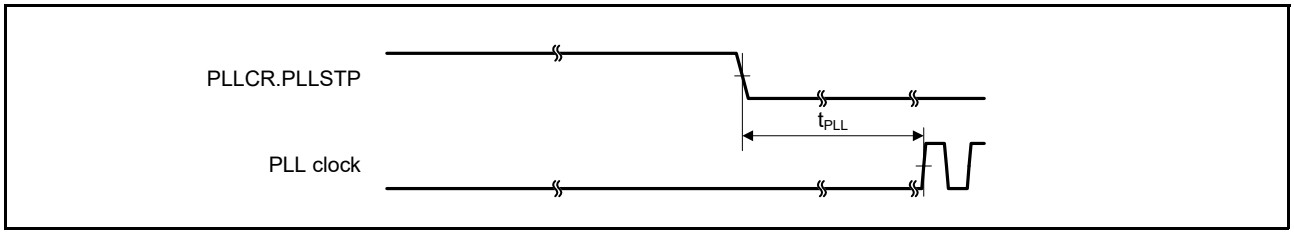


Figure 2.29 PLL clock oscillation start timing (PLL is operated after main clock oscillation has settled)

2.3.4 Wakeup Time

Table 2.24 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 2.34
			System clock source is PLL (48 MHz) with main clock oscillator*2	t_{SBYPC}	-	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t_{SBYEX}	-	14	25	µs	
			System clock source is PLL (48 MHz) with main clock oscillator*3	t_{SBYPE}	-	53	76	µs	
		System clock source is HOCO*4 (HOCO clock is 32 MHz)		t_{SBYHO}	-	43	52	µs	
		System clock source is HOCO*4 (HOCO clock is 48 MHz)		t_{SBYHO}	-	44	52	µs	
		System clock source is HOCO*5 (HOCO clock is 64 MHz)		t_{SBYHO}	-	82	110	µs	
		System clock source is MOCO		t_{SBYMO}	-	16	25	µs	

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
Note 4. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 05h.
Note 5. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 06h.

Table 2.25 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (12 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 2.34
			System clock source is PLL (24 MHz) with main clock oscillator*2	t_{SBYPC}	-	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (12 MHz)*3	t_{SBYEX}	-	2.9	10	µs	
			System clock source is PLL (24 MHz) with main clock oscillator*3	t_{SBYPE}	-	49	76	µs	
		System clock source is HOCO (24 MHz)		t_{SBYHO}	-	38	50	µs	
		System clock source is MOCO		t_{SBYMO}	-	3.5	5.5	µs	

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

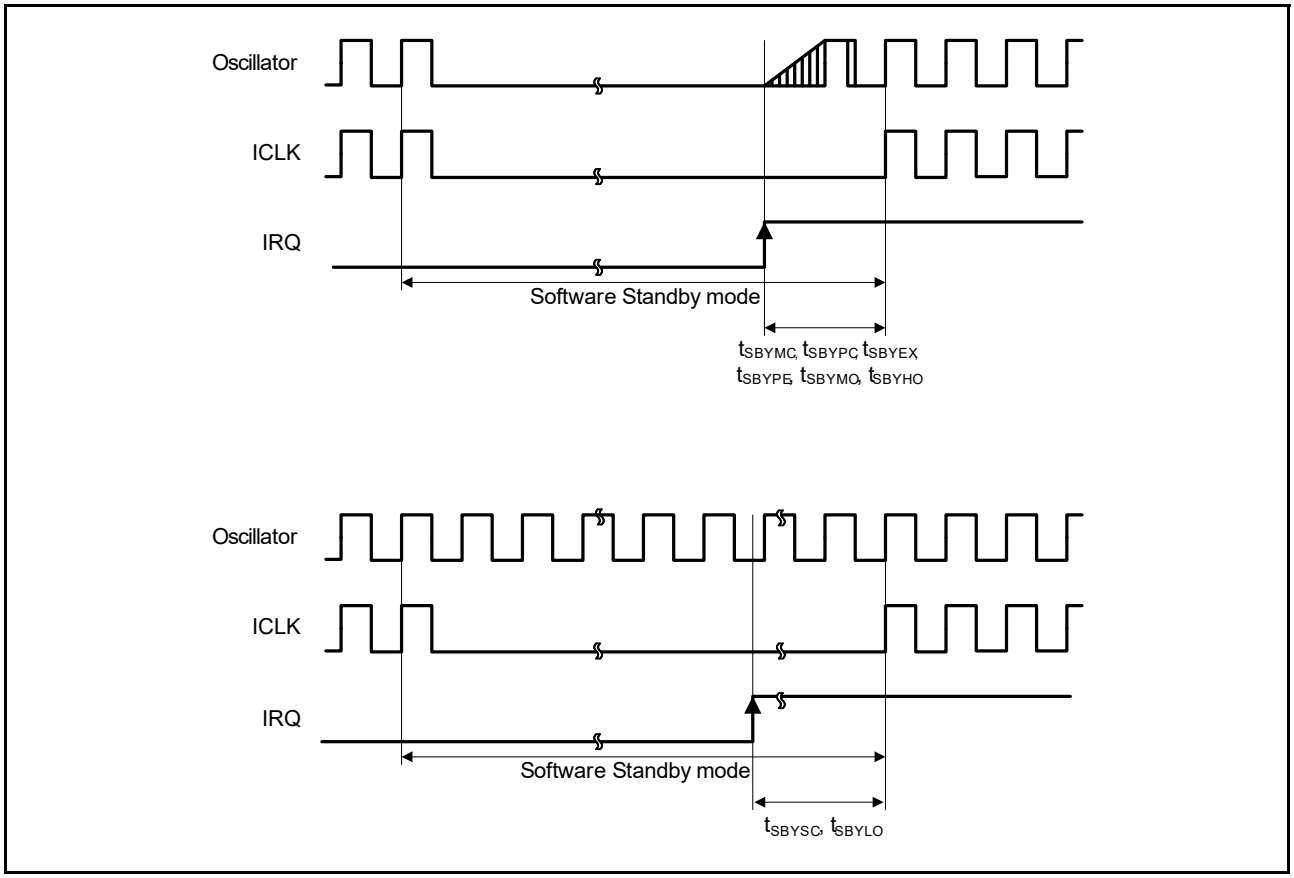


Figure 2.34 Software Standby mode cancellation timing

Table 2.29 Timing of recovery from low power modes (6)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	-	36	45	µs	Figure 2.35
	Middle-speed mode System clock source is MOCO	t_{SNZ}	-	1.3	3.6	µs	
	Low-speed mode System clock source is MOCO	t_{SNZ}	-	10	13	µs	
	Low-voltage mode System clock source is HOCO	t_{SNZ}	-	87	110	µs	

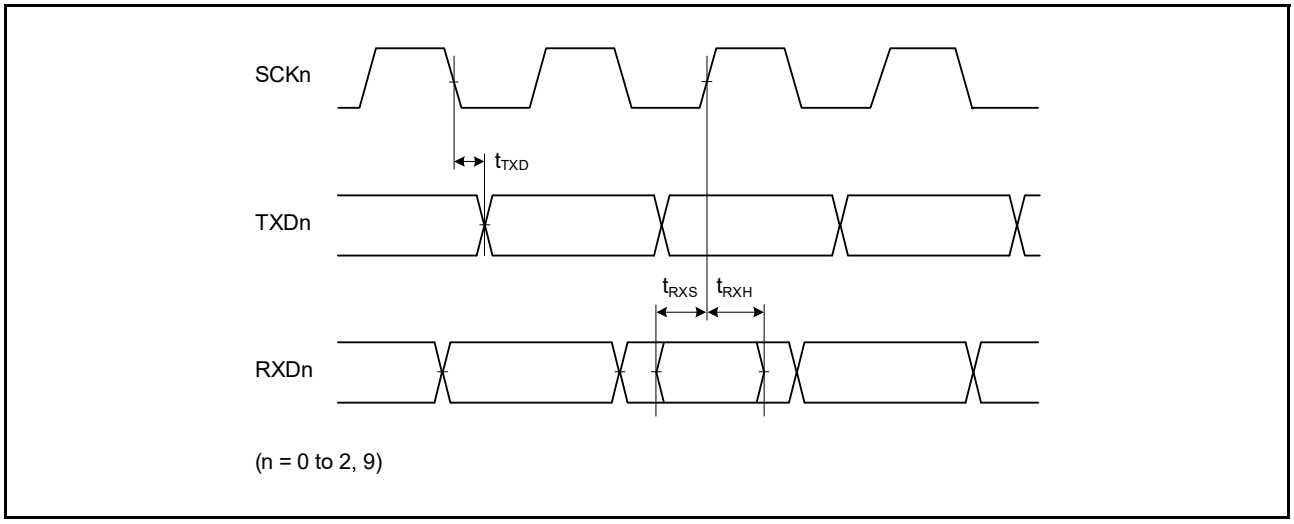


Figure 2.45 SCI input/output timing in clock synchronous mode

Table 2.34 SCI timing (2) (1 of 2)

Parameter				Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)			t_{SPcyc}	4	65,536	t_{Pcyc}	Figure 2.46
	SCK clock cycle input (slave)				6	65,536		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		1.8 V or above	t_{SPCKr}, t_{SPCKf}	-	20	ns	
			1.6 V or above		-	30		
	Data input setup time	Master	2.7 V or above	t_{SU}	45	-	ns	Figure 2.47 to Figure 2.50
			2.4 V or above		55	-		
			1.8 V or above		80	-		
			1.6 V or above		110	-		
		Slave	2.7 V or above		40	-		
			1.6 V or above		45	-		
	Data input hold time	Master		t_H	33.3	-	ns	
		Slave			40	-		
	SS input setup time			t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	Master	1.8 V or above	t_{OD}	-	40	ns	
			1.6 V or above		-	50		
		Slave	2.4 V or above		-	65		
			1.8 V or above		-	100		
			1.6 V or above		-	125		
	Data output hold time	Master	2.7 V or above	t_{OH}	-10	-	ns	
			2.4 V or above		-20	-		
			1.8 V or above		-30	-		
			1.6 V or above		-40	-		
		Slave			-10	-		
	Data rise and fall time	Master	1.8 V or above	t_{Dr}, t_{Df}	-	20	ns	
			1.6 V or above		-	30		
		Slave	1.8 V or above		-	20		
			1.6 V or above		-	30		

Table 2.45 A/D conversion characteristics (4) in low power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.50	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (C_{in}), see section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics.

Table 2.46 A/D conversion characteristics (5) in low power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	16	MHz	-
Analog input capacitance*2		Cs	-	-	8 (reference data)	pF	High-precision channel
			-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance		Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
			-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range		Ain	0	-	VREFH0	V	-
12-bit mode							
Resolution			-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ		3.38	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
			5.06	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error			-	±0.5	±4.5	LSB	High-precision channel
					±6.0	LSB	Other than above

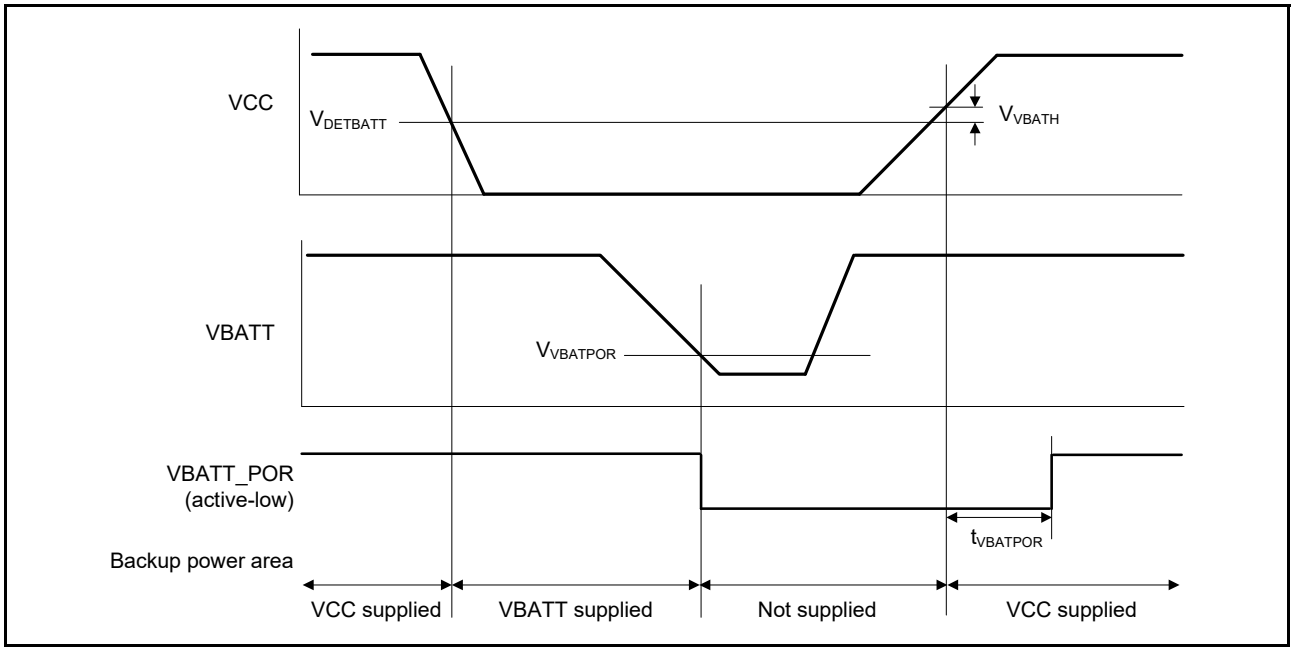


Figure 2.79 VBATT_POR reset timing

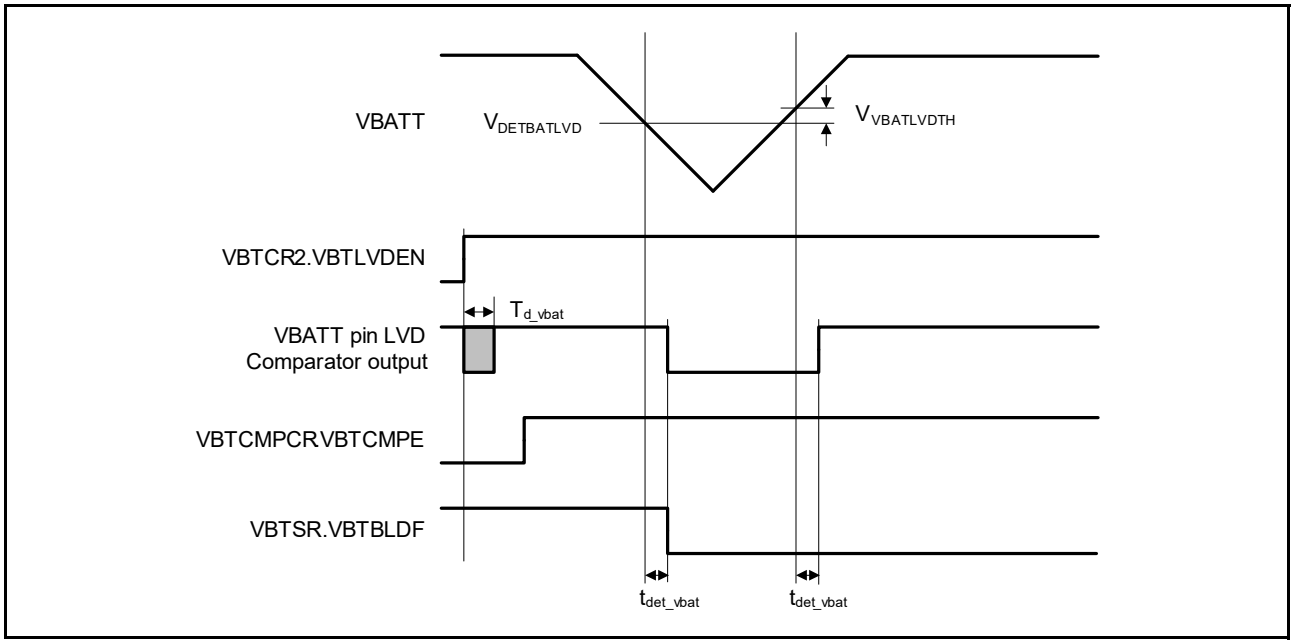


Figure 2.80 VBATT pin voltage detection circuit timing

Table 2.59 VBATT-I/O characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
VBATWIOn I/O output characteristics (n = 0 to 2)	VCC > $V_{DETBATT}$	VCC = 4.0 to 5.5 V	V_{OH}	VCC - 0.8	-	-	V	I_{OH} = -200 µA
			V_{OL}	-	-	0.8		I_{OL} = 200 µA
		VCC = 2.7 to 4.0 V	V_{OH}	VCC - 0.5	-	-		I_{OH} = -100 µA
			V_{OL}	-	-	0.5		I_{OL} = 100 µA
		VCC = $V_{DETBATT}$ to 2.7 V	V_{OH}	VCC - 0.3	-	-		I_{OH} = -50 µA
			V_{OL}	-	-	0.3		I_{OL} = 50 µA
	VCC < $V_{DETBATT}$	VBATT = 2.7 to 3.6 V	V_{OH}	V_{BATT} - 0.5	-	-		I_{OH} = -100 µA
			V_{OL}	-	-	0.5		I_{OL} = 100 µA
		VBATT = 1.6 to 2.7 V	V_{OH}	V_{BATT} - 0.3	-	-		I_{OH} = -50 µA
			V_{OL}	-	-	0.3		I_{OL} = 50 µA

2.11 CTSU Characteristics

Table 2.60 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣIoH	-	-	-24	mA	When the mutual capacitance method is applied

2.12 Segment LCD Controller Characteristics

2.12.1 Resistance Division Method

[Static Display Mode]

Table 2.61 Resistance division method LCD characteristics (1)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.0	-	VCC	V	-

[1/2 Bias Method, 1/4 Bias Method]

Table 2.62 Resistance division method LCD characteristics (2)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.7	-	VCC	V	-

[1/3 Bias Method]

Table 2.63 Resistance division method LCD characteristics (3)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.5	-	VCC	V	-

2.12.2 Internal Voltage Boosting Method

[1/3 Bias Method]

Table 2.64 Internal voltage boosting method LCD characteristics
Conditions: VCC = 1.8 V to 5.5 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C4*1 = 0.47 µF	VLCD = 04h	0.90	1.0	1.08	V	-
			VLCD = 05h	0.95	1.05	1.13	V	-
			VLCD = 06h	1.00	1.10	1.18	V	-
			VLCD = 07h	1.05	1.15	1.23	V	-
			VLCD = 08h	1.10	1.20	1.28	V	-
			VLCD = 09h	1.15	1.25	1.33	V	-
			VLCD = 0Ah	1.20	1.30	1.38	V	-
			VLCD = 0Bh	1.25	1.35	1.43	V	-
			VLCD = 0Ch	1.30	1.40	1.48	V	-
			VLCD = 0Dh	1.35	1.45	1.53	V	-
			VLCD = 0Eh	1.40	1.50	1.58	V	-
			VLCD = 0Fh	1.45	1.55	1.63	V	-
			VLCD = 10h	1.50	1.60	1.68	V	-
			VLCD = 11h	1.55	1.65	1.73	V	-
			VLCD = 12h	1.60	1.70	1.78	V	-
			VLCD = 13h	1.65	1.75	1.83	V	-
Doubler output voltage	V_{L2}	C1 to C4*1 = 0.47 µF		$2 \times V_{L1}$ - 0.1	$2 \times V_{L1}$	$2 \times V_{L1}$	V	-
Tripler output voltage	V_{L4}	C1 to C4*1 = 0.47 µF		$3 \times V_{L1}$ - 0.15	$3 \times V_{L1}$	$3 \times V_{L1}$	V	-
Reference voltage setup time*2	t_{VL1S}			5	-	-	ms	Figure 2.81
LCD output voltage variation range*3	t_{VLWT}	C1 to C4*1 = 0.47 µF		500	-	-	ms	

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

2.15 Flash Memory Characteristics

2.15.1 Code Flash Memory Characteristics

Table 2.69 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	-	-	Times	-
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	-	-	Year	T_a = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be done n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.70 Code flash characteristics (2)
High-speed operating mode
Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P8}	-	116	998	-	54	506	µs
Erasure time	2-KB	t_{E2K}	-	9.03	287	-	5.67	222	ms
Blank check time	8-byte	t_{BC8}	-	-	56.8	-	-	16.6	µs
	2-KB	t_{BC2K}	-	-	1899	-	-	140	µs
Erase suspended time		t_{SED}	-	-	22.5	-	-	10.7	µs
Startup area switching setting time		t_{SAS}	-	21.7	585	-	12.1	447	ms
Access window time		t_{AWS}	-	21.7	585	-	12.1	447	ms
OCD/serial programmer ID setting time		t_{OSIS}	-	21.7	585	-	12.1	447	ms
Flash memory mode transition wait time 1		t_{DIS}	2	-	-	2	-	-	µs
Flash memory mode transition wait time 2		t_{MS}	5	-	-	5	-	-	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

Table 2.74 Data flash characteristics (3)
Middle-speed operating mode
Conditions: VCC = 1.8 to 5.5 V, T_a = -40 to +85°C

Parameter		Symbol	FCLK = 4 MHz			FCLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	-	94.7	886	-	89.3	849	µs
Erasure time	1-KB	t_{DE1K}	-	9.59	299	-	8.29	273	ms
Blank check time	1-byte	t_{DBC1}	-	-	56.2	-	-	52.5	µs
	1-KB	t_{DBC1K}	-	-	2.17	-	-	1.51	ms
Suspended time during erasing		t_{DSED}	-	-	23.0	-	-	21.7	µs
Data flash STOP recovery time		t_{DSTOP}	720	-	-	720	-	-	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

2.16 Boundary Scan

Table 2.75 Boundary scan
Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	-	-	ns	Figure 2.82
TCK clock high pulse width	t_{TCKH}	45	-	-	ns	
TCK clock low pulse width	t_{TCKL}	45	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	20	-	-	ns	Figure 2.83
TMS hold time	t_{TMSH}	20	-	-	ns	
TDI setup time	t_{TDIS}	20	-	-	ns	
TDI hold time	t_{TDIH}	20	-	-	ns	
TDO data delay	t_{TDOD}	-	-	70	ns	
Boundary Scan circuit start up time*1	t_{BSSTUP}	t_{RESWP}	-	-	-	Figure 2.84

Note 1. Boundary scan does not function until power-on-reset becomes negative.

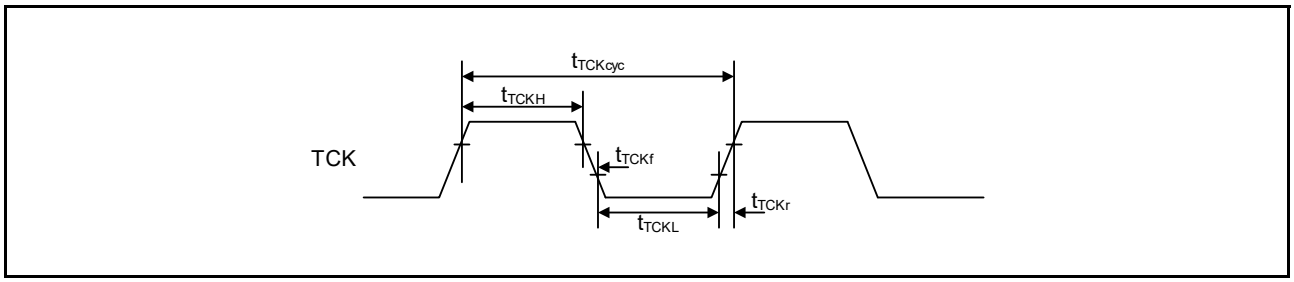


Figure 2.82 Boundary scan TCK timing

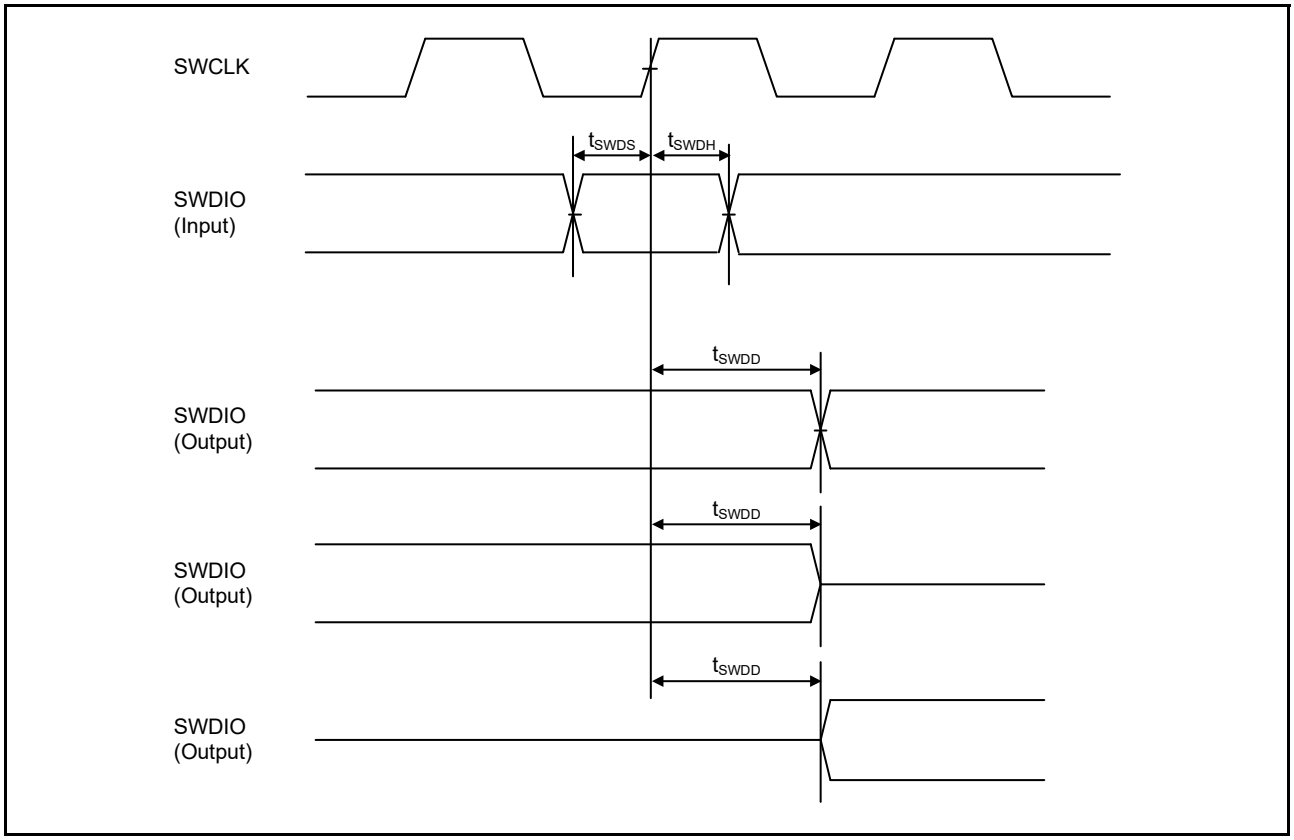
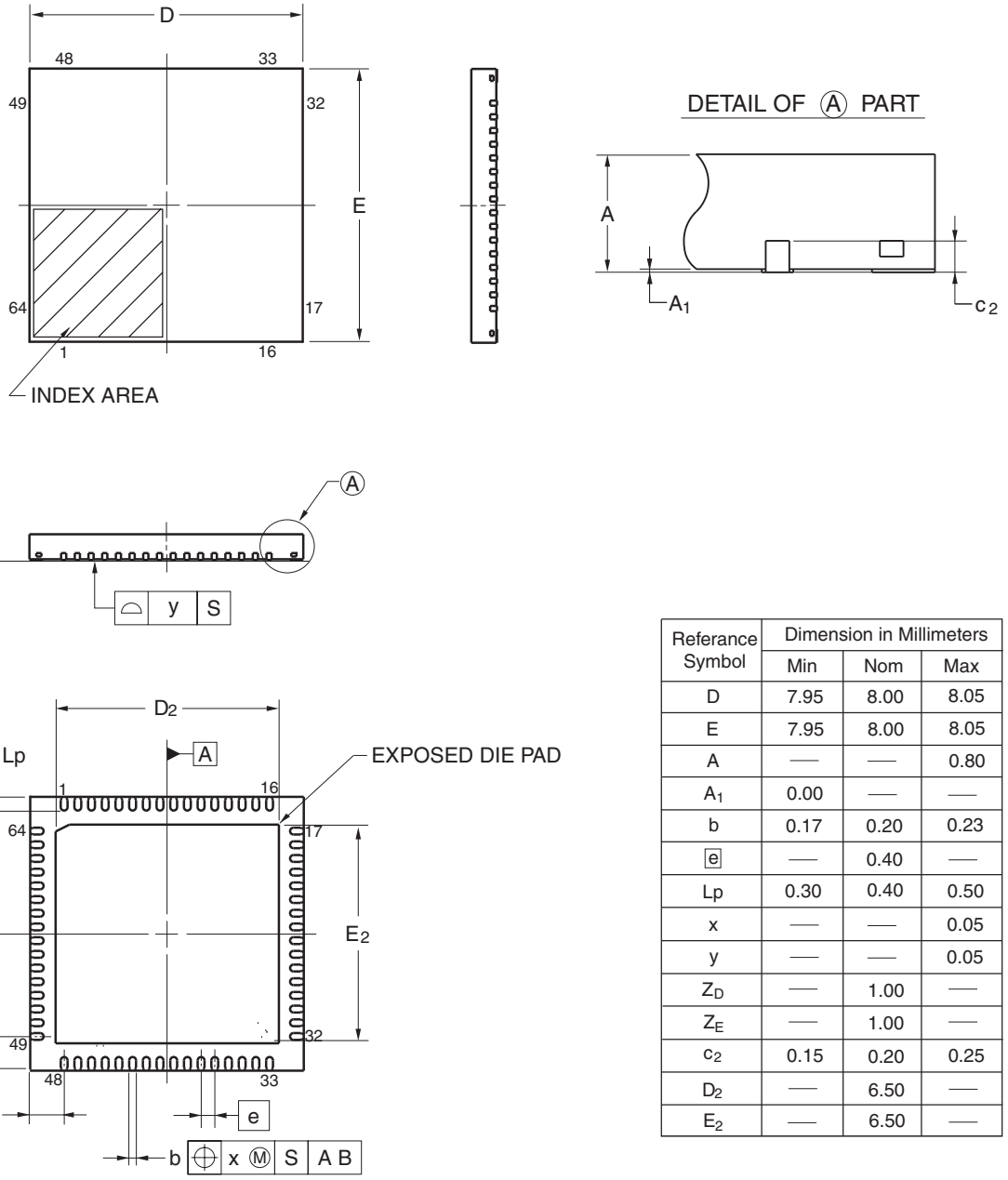


Figure 2.88 SWD input/output timing

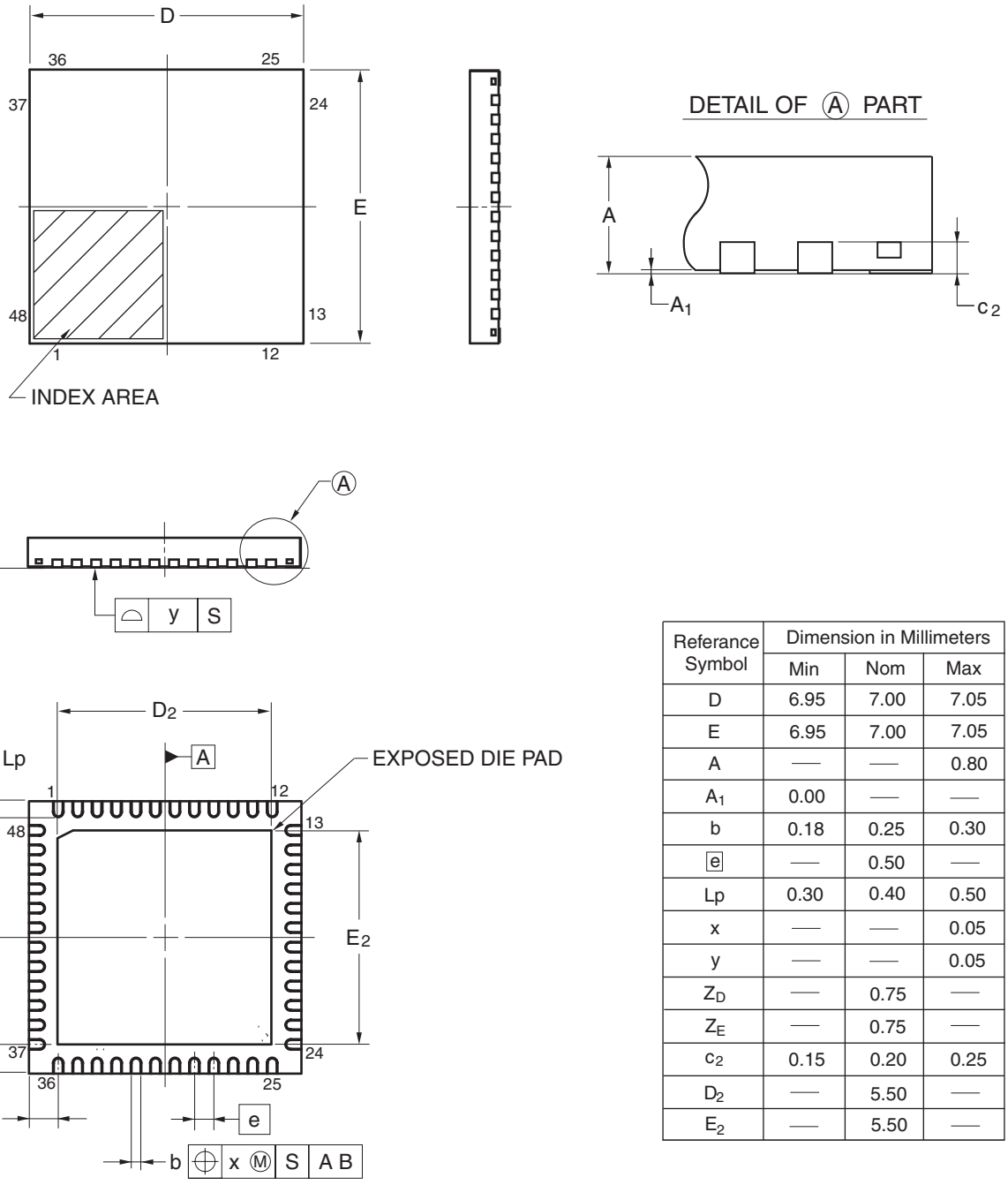
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN64-8x8-0.40	PWQN0064LA-A	P64K8-40-9B5-3	0.16



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	7.95	8.00	8.05
E	7.95	8.00	8.05
A	—	—	0.80
A_1	0.00	—	—
b	0.17	0.20	0.23
e	—	0.40	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	1.00	—
Z_E	—	1.00	—
c_2	0.15	0.20	0.25
D_2	—	6.50	—
E_2	—	6.50	—

Figure 1.4 64-pin QFN

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—

Figure 1.6 48-pin QFN