Renesas Electronics America Inc - R7FS3A6783A01CFP#AA0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 25x14b; D/A 3x8b, 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a6783a01cfp-aa0

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU provides an optimal combination of low-power, high-performance Arm Cortex®-M4 core running up to 48 MHz with the following features:

- 256-KB code flash memory
- 32-KB SRAM
- Segment LCD Controller (SLCDC)
- Capacitive Touch Sensing Unit (CTSU)
- USB 2.0 Full-Speed Module (USBFS)
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- Security features.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M4 core	• Maximum operating frequency: up to 48 MHz • Arm Cortex-M4 core - Revision: r0p1-01rel0 - Armv7E-M architecture profile - Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008. • Arm Memory Protection Unit (Arm MPU) - Armv7 Protected Memory System Architecture - 8 protected regions. • SysTick timer - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256-KB code flash memory. See section 44, Flash Memory in User's Manual.
Data flash memory	8-KB data flash memory. See section 44, Flash Memory in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). An area in SRAM0 provides error correction capability using ECC. See section 43, SRAM in User's Manual.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI/USB boot mode. See section 3, Operating Modes in User's Manual.
Resets	14 resets: • RES pin reset • Power-on reset • VBATT-selected voltage power-on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • CPU stack pointer error reset • Software reset. See section 5, Resets in User's Manual.
Low Voltage Detection (LVD)	Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 7, Low Voltage Detection (LVD) in User's Manual.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • IWDT-dedicated on-chip oscillator • Clock out support. See section 8, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 9, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 13, Interrupt Controller Unit (ICU) in User's Manual.
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 20, Key Interrupt Function (KINT) in User's Manual.
Low power modes	Power consumption can be reduced in multiple ways, such as by setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 10, Low Power Modes in User's Manual.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery powered area includes RTC, SOSC, LOCO, wakeup control, backup memory, VBATT_R low voltage detection, and switches between VCC and VBATT. During normal operation, the battery powered area is powered by the main power supply, which is the VCC pin. When a VCC voltage drop is detected, the power source is switched to the dedicated battery backup power pin, the VBATT pin. When the voltage rises again, the power source is switched from the VBATT pin to the VCC pin. See section 11, Battery Backup Function in User's Manual.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 12, Register Write Protection in User's Manual.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 32, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 42, Data Operation Circuit (DOC) in User's Manual.

Table 1.11 Security

Feature	Functional description
Secure Crypto Engine 5 (SCE5)	• Security algorithm - Symmetric algorithm: AES. • Other support features - TRNG (True Random Number Generator) - Hash-value generation: GHASH.

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

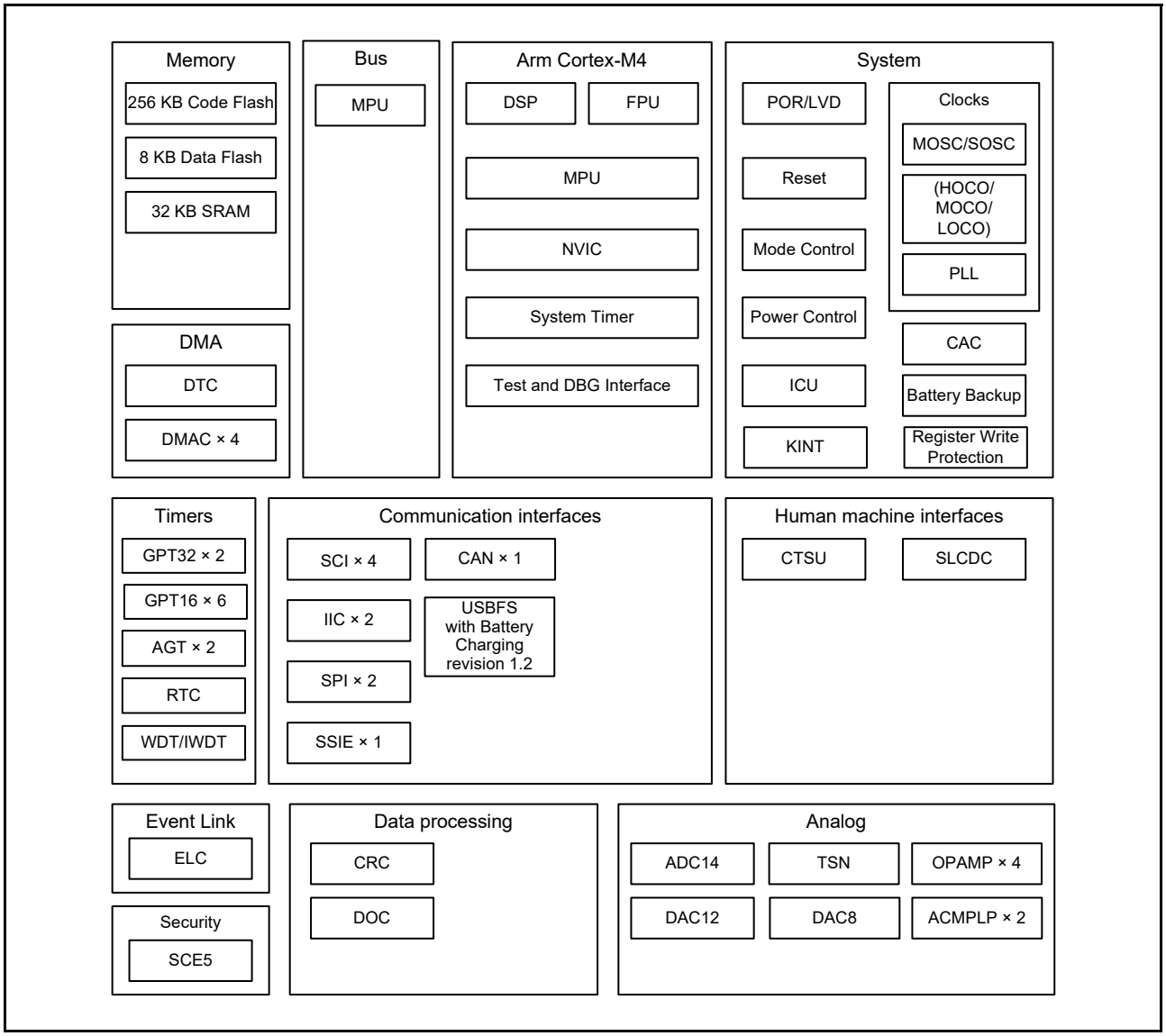


Figure 1.1 Block diagram

1.6 Pin Assignments

Figure 1.3 to Figure 1.6 show the pin assignments.

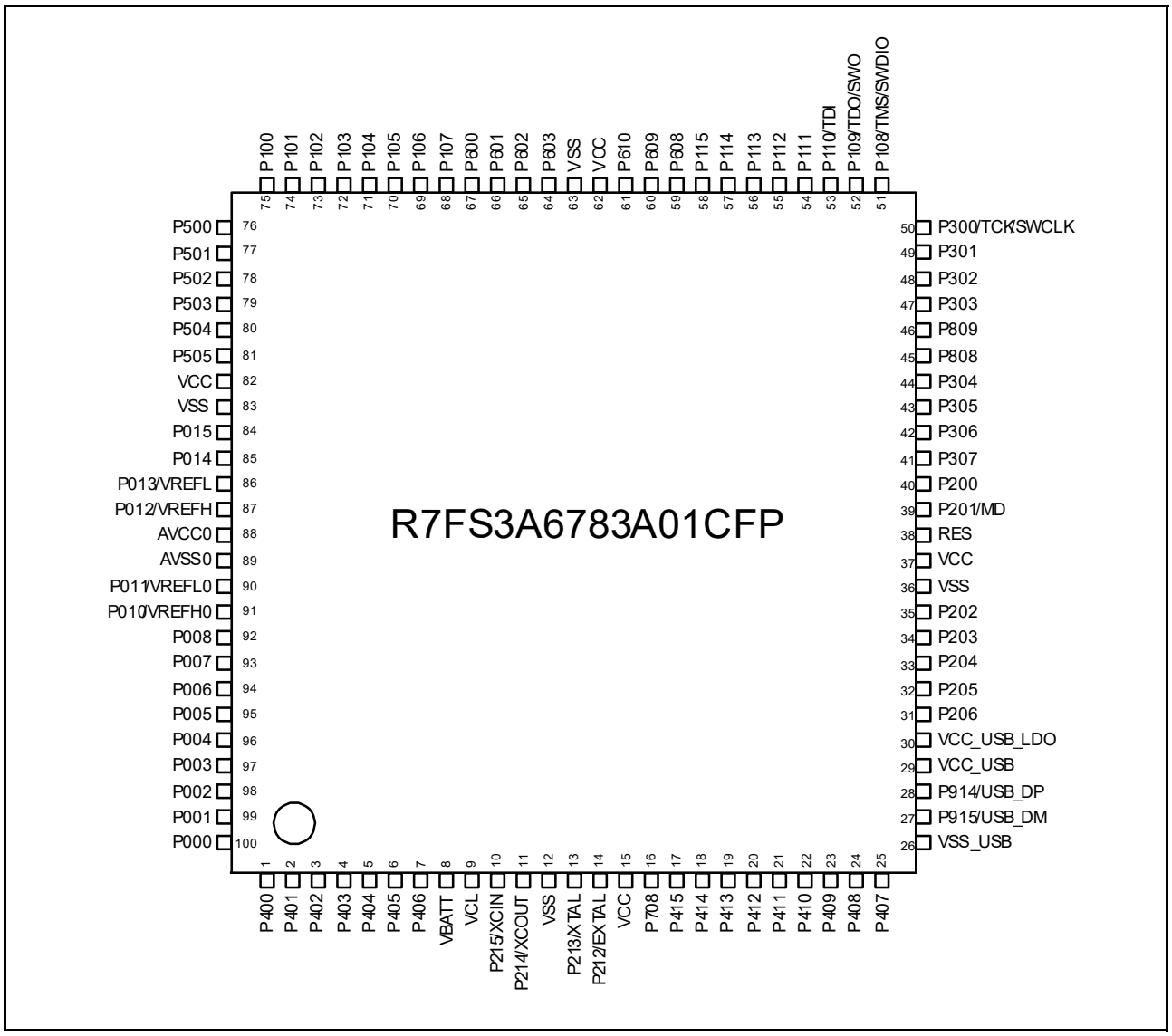


Figure 1.3 Pin assignment for 100-pin LQFP (top view)

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
Input voltage	5 V-tolerant ports*1	V_{in}	-0.3 to +6.5	V
	P000 to P008, P010 to P015	V_{in}	-0.3 to AVCC0 + 0.3	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +6.5	V
		VREFH		V
VBATT power supply voltage		VBATT	-0.5 to +6.5	V
Analog power supply voltage		AVCC0	-0.5 to +6.5	V
USB power supply voltage		VCC_USB	-0.5 to +6.5	V
		VCC_USB_LDO	-0.5 to +6.5	V
Analog input voltage	When AN000 to AN014 are used	V_{AN}	-0.3 to AVCC0 + 0.3	V
	When AN016 to AN025 are used		-0.3 to VCC + 0.3	V
LCD voltage	VL1 voltage	V_{L1}	-0.3 to +2.8	V
	VL2 voltage	V_{L2}	-0.3 to +6.5	V
	VL3 voltage	V_{L3}	-0.3 to +6.5	V
	VL4 voltage	V_{L4}	-0.3 to +6.5	V
Operating temperature*2,*3,*4		T_{opr}	-40 to +105	°C
			-40 to +85	
Storage temperature		T_{stg}	-55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, and between the VREFH and VREFL pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.
Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. The capacitor must be placed close to the pin.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

Note 1. Ports P205, P206, P400 to P404, P407, P408 are 5 V tolerant.
Note 2. See section 2.2.1, Tj/Ta Definition.
Note 3. Contact a Renesas Electronics sales office for information on derating operation under T_a = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
Note 4. The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section 1.3, Part Numbering.

2.2 DC Characteristics

2.2.1 Tj/T_a Definition

Table 2.3 DC Characteristics

Conditions: Products with operating temperature (T_a) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that Tj = T_a + θja × total power consumption (W),
where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

Note 1. The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section 1.3, Part Numbering. If the part number shows the operation temperature at 85°C, then the maximum value of T_j is +105°C, otherwise, it is +125°C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1)

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 5.5V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

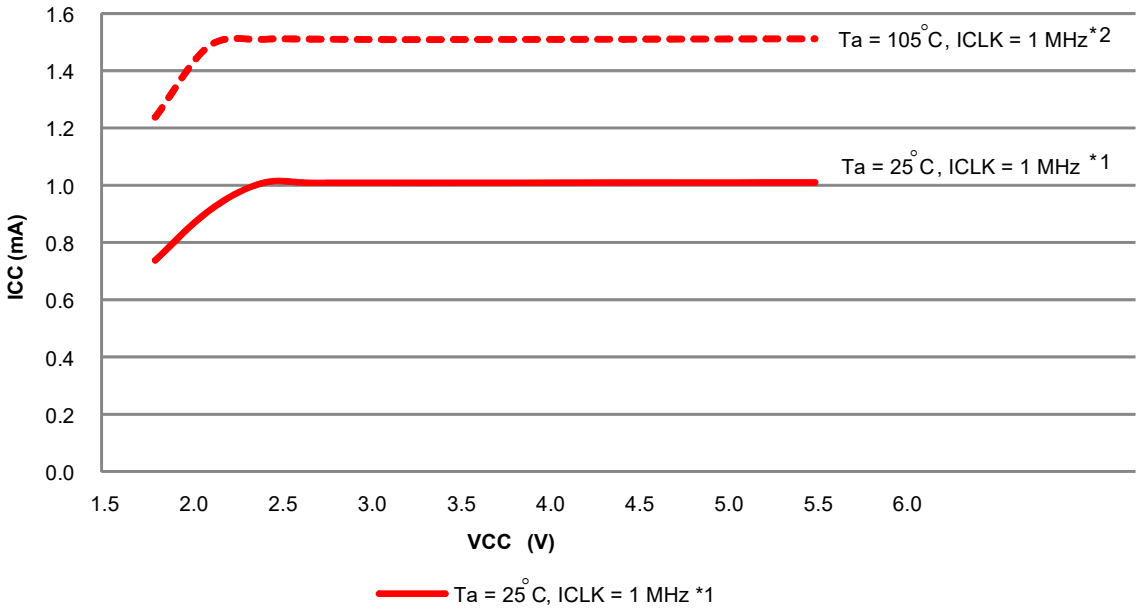
Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Schmitt trigger input voltage	IIC*1 (except for SMBus)	V_{IH}	VCC × 0.7	-	5.8	V	-
		V_{IL}	-	-	VCC × 0.3		
		ΔV_T	VCC × 0.05	-	-		
	RES, NMI Other peripheral input pins excluding IIC	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.1	-	-		
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	V_{IH}	2.2	-	-		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	-	-		VCC = 2.7 to 3.6 V
		V_{IL}	-	-	0.8		-
	5 V-tolerant ports*3	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	P000 to P008, P010 to P015	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	EXTAL Input ports pins except for P000 to P008, P010 to P015, P914, P915	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
When V_{BATT} power supply is selected	P402, P403, P404	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3		
		V_{IL}	-	-	V_{BATT} × 0.2		
		ΔV_T	V_{BATT} × 0.05	-	-		

Note 1. P205, P206, P400, P401, P407, P408 (total 6 pins).
Note 2. P100, P101, P204, P205, P206, P400, P401, P407, P408 (total 9 pins).
Note 3. P205, P206, P400 to P404, P407, P408 (total 9 pins).

2.2.3 I/O I_{OH}, I_{OL}

Table 2.6 I/O I_{OH}, I_{OL} (1 of 2)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LCO = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P212, P213	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Port P408	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive for IIC Fast-mode*4 VCC = 2.7 to 5.5 V	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Port P409	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P100 to P115, P201 to P204, P300 to P307, P500 to P503, P600 to P603, P608 to P610, P808, P809 (total 41 pins)	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P914, P915	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Other output pin*3	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

Figure 2.19 Voltage dependency in Low-speed mode (reference data)

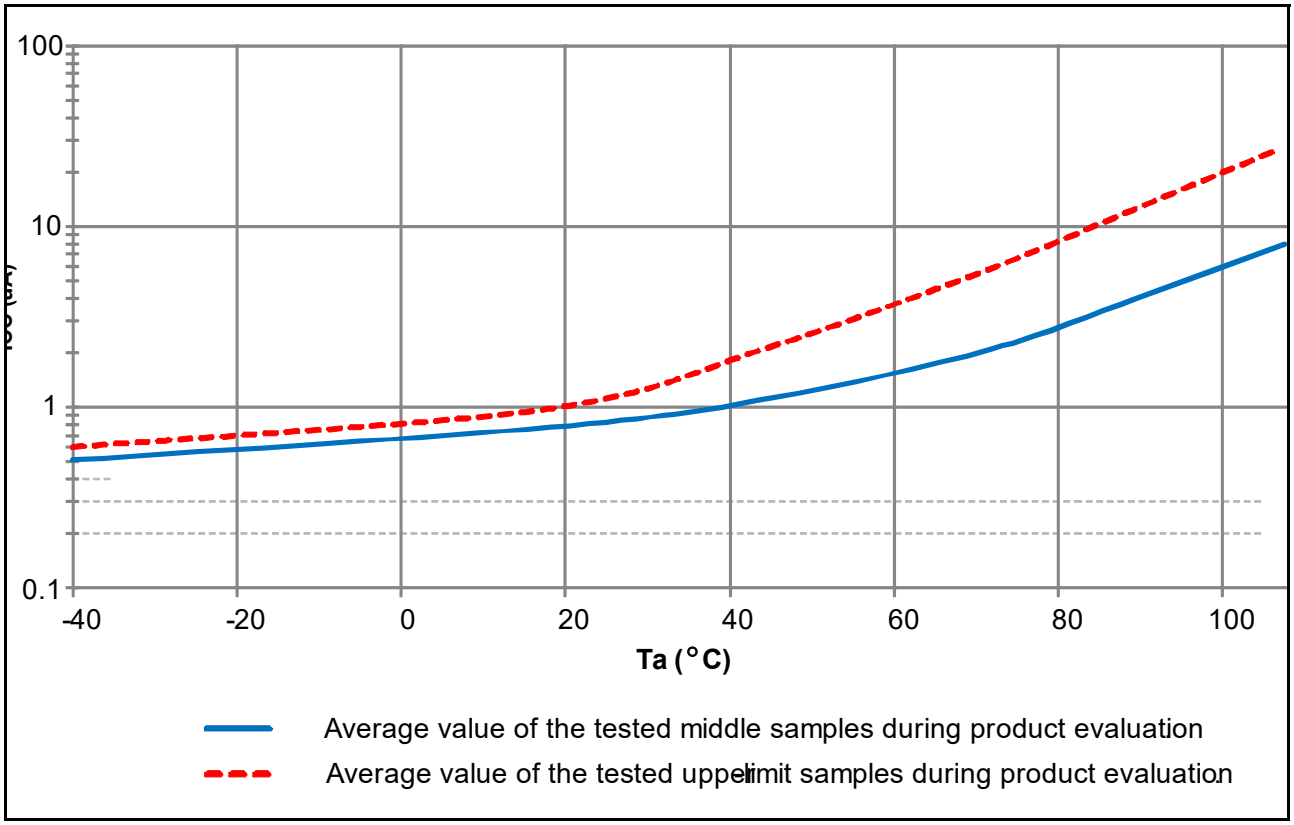


Figure 2.22 Temperature dependency in Software Standby mode all SRAM (reference data)

Table 2.13 Operating and standby current (3)

Conditions: VCC = AVCC0 = 0V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0V

Parameter			Symbol	Typ	Max	Unit	Test conditions
Supply current*1	RTC operation when VCC is off	T_a = 25°C	I_{CC}	0.8	-	µA	VBATT = 2.0 V SOMCR.SORDRV[1:0] = 11b (Low power mode 3)
		T_a = 55°C		0.9	-		
		T_a = 85°C		1.0	-		
		T_a = 105°C		1.1	-		
		T_a = 25°C		0.9	-		VBATT = 3.3 V SOMCR.SORDRV[1:0] = 11b (Low power mode 3)
		T_a = 55°C		1.0	-		
		T_a = 85°C		1.1	-		
		T_a = 105°C		1.2	-		
		T_a = 25°C		1.5	-		VBATT = 2.0 V SOMCR.SORDRV[1:0] = 00b (Normal mode)
		T_a = 55°C		1.7	-		
		T_a = 85°C		2.0	-		
		T_a = 105°C		2.2	-		
		T_a = 25°C		1.6	-		VBATT = 3.3 V SOMCR.SORDRV[1:0] = 00b (Normal mode)
		T_a = 55°C		1.8	-		
		T_a = 85°C		2.1	-		
		T_a = 105°C		2.3	-		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Table 2.21 Operation frequency value in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*3	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Flash interface clock (FCLK)*1, *3	1.8 to 5.5 V		27.8528	32.768	37.6832	
	Peripheral module clock (PCLKA)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKC)*2, *3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		-	-	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The 14-bit A/D converter cannot be used.
Note 3. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK.

2.3.2 Clock Timing

Table 2.22 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	-	-	ns	Figure 2.25
EXTAL external clock input high pulse width	t_{XH}	20	-	-	ns	
EXTAL external clock input low pulse width	t_{XL}	20	-	-	ns	
EXTAL external clock rising time	t_{Xr}	-	-	5	ns	
EXTAL external clock falling time	t_{Xf}	-	-	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	0.3	-	-	μs	-
EXTAL external clock input frequency	f_{EXTAL}	-	-	20	MHz	2.4 ≤ VCC ≤ 5.5
		-	-	8		1.8 ≤ VCC < 2.4
		-	-	1		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency	f_{MAIN}	1	-	20	MHz	2.4 ≤ VCC ≤ 5.5
		1	-	8		1.8 ≤ VCC < 2.4
		1	-	4		1.6 ≤ VCC < 1.8
Main clock oscillation stabilization wait time (crystal)*9	$t_{MAINOSCWT}$	-	-	-*9	ms	-
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization time	t_{LOCO}	-	-	100	μs	Figure 2.26
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization time	t_{MOCO}	-	-	1	μs	-

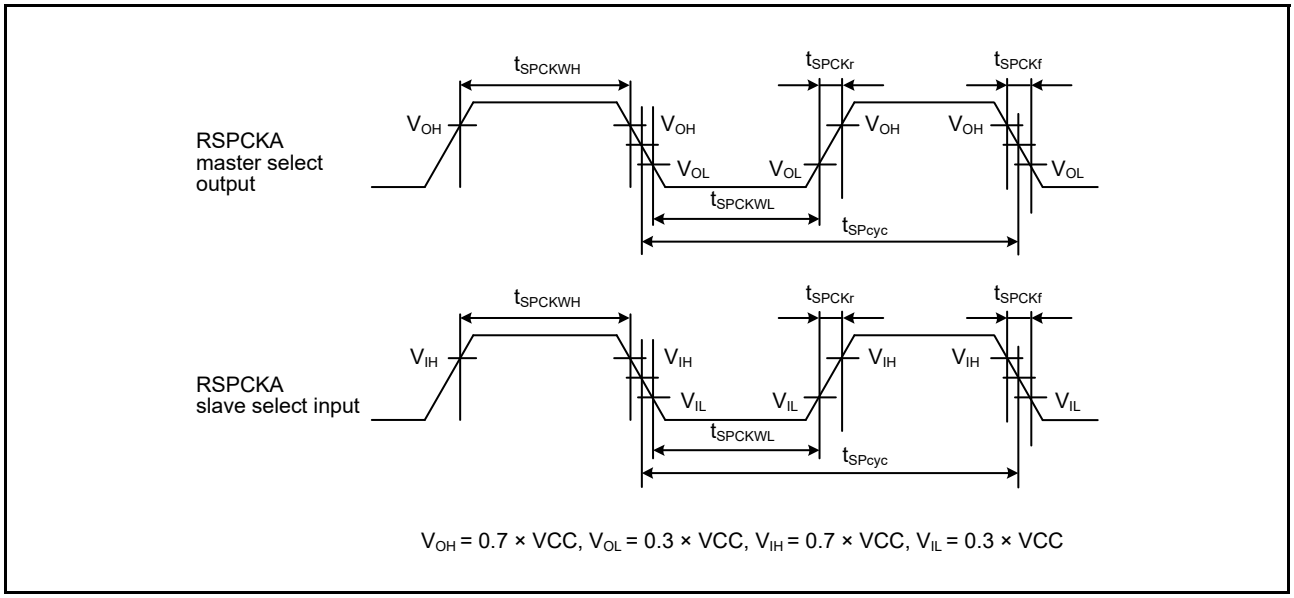


Figure 2.52 SPI clock timing

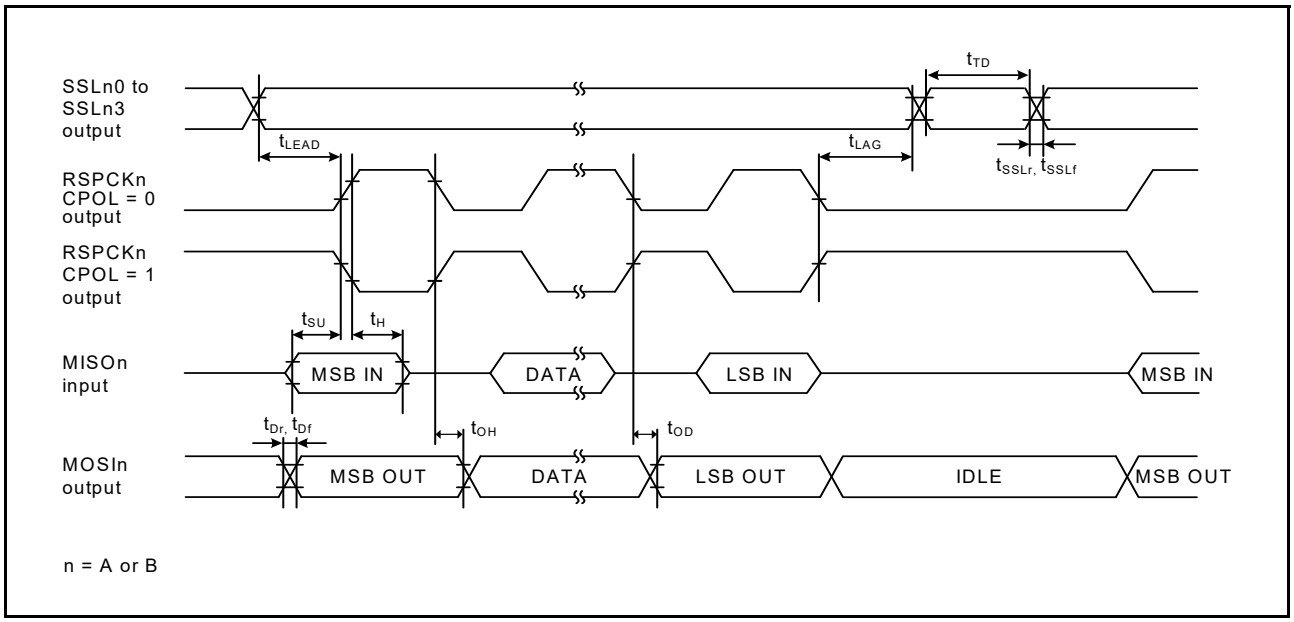


Figure 2.53 SPI timing for master when CPHA = 0 and the bit rate is set to any value other than PCLKA/2

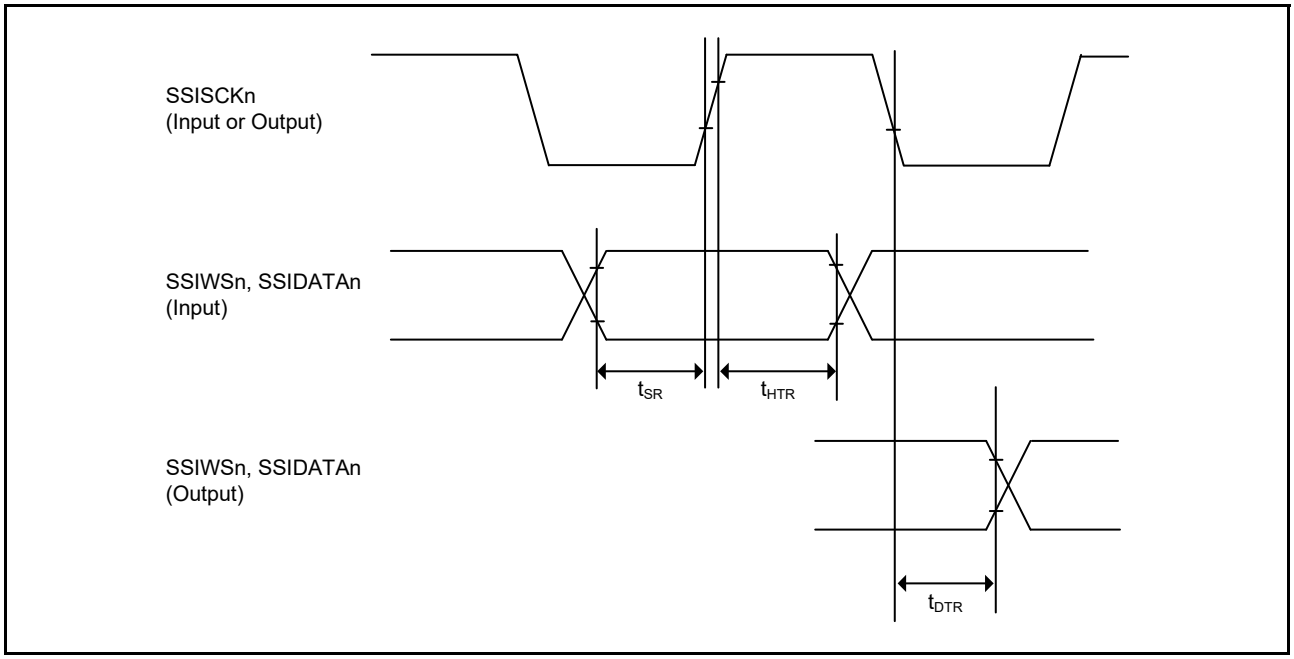


Figure 2.61 SSIE data transmit/receive timing (SSICR.BCKP = 0)

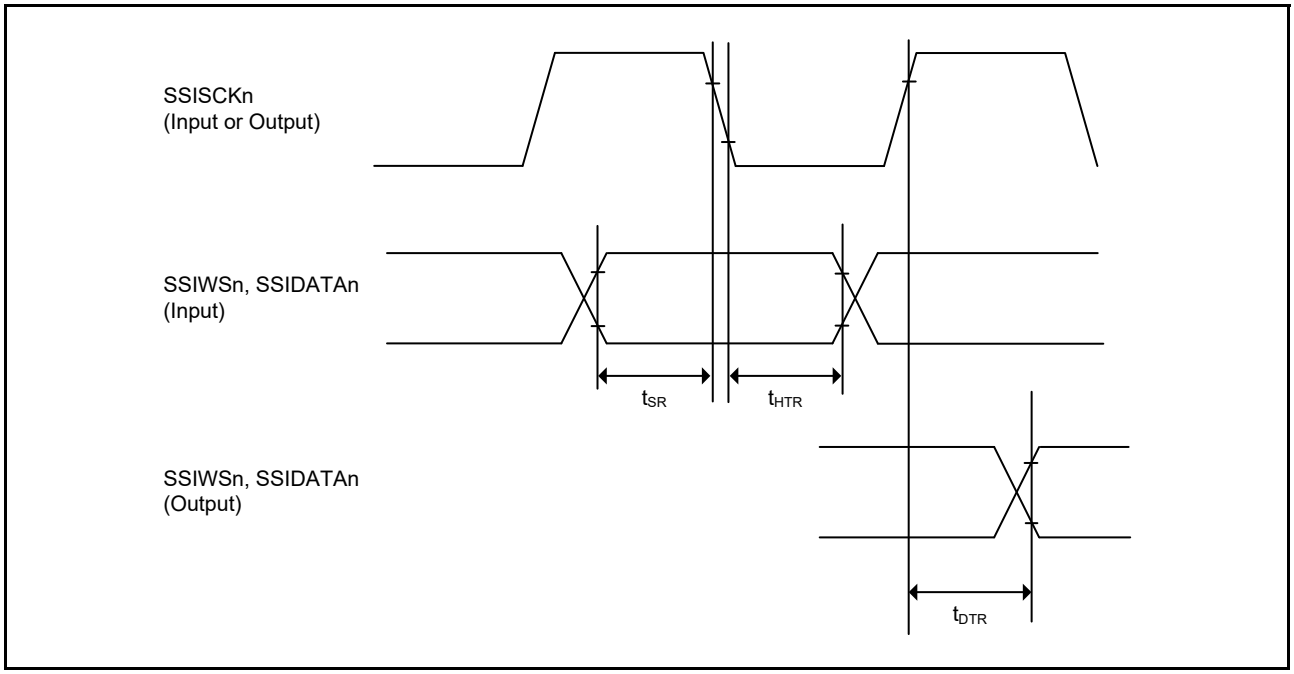


Figure 2.62 SSIE data transmit/receive timing (SSICR.BCKP = 1)

Table 2.44 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.59	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.44	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (C_{in}), see section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics.

Table 2.45 A/D conversion characteristics (4) in low power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	24	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.25	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.38	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-

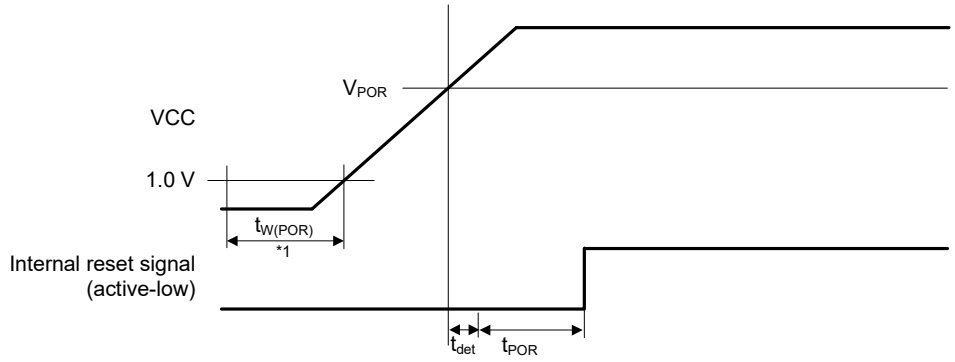
Table 2.46 A/D conversion characteristics (5) in low power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.75	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.44	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (C_{in}), see section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics.

Table 2.47 A/D conversion characteristics (6) in low power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	8	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	3.8 (reference data)	kΩ	High-precision channel
		-	-	8.2 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	6.75	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.13	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h



Note: $t_{W(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{W(POR)}$ for 1.0 ms or more.

Figure 2.74 Power-on reset timing

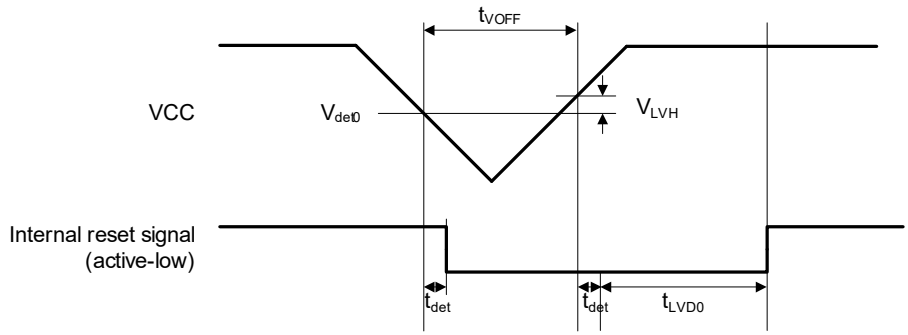


Figure 2.75 Voltage detection circuit timing (V_{det0})

2.12 Segment LCD Controller Characteristics

2.12.1 Resistance Division Method

[Static Display Mode]

Table 2.61 Resistance division method LCD characteristics (1)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.0	-	VCC	V	-

[1/2 Bias Method, 1/4 Bias Method]

Table 2.62 Resistance division method LCD characteristics (2)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.7	-	VCC	V	-

[1/3 Bias Method]

Table 2.63 Resistance division method LCD characteristics (3)
Conditions: VL4 ≤ VCC ≤ 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.5	-	VCC	V	-

2.12.2 Internal Voltage Boosting Method

[1/3 Bias Method]

Table 2.64 Internal voltage boosting method LCD characteristics
Conditions: VCC = 1.8 V to 5.5 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C4*1 = 0.47 µF	VLCD = 04h	0.90	1.0	1.08	V	-
			VLCD = 05h	0.95	1.05	1.13	V	-
			VLCD = 06h	1.00	1.10	1.18	V	-
			VLCD = 07h	1.05	1.15	1.23	V	-
			VLCD = 08h	1.10	1.20	1.28	V	-
			VLCD = 09h	1.15	1.25	1.33	V	-
			VLCD = 0Ah	1.20	1.30	1.38	V	-
			VLCD = 0Bh	1.25	1.35	1.43	V	-
			VLCD = 0Ch	1.30	1.40	1.48	V	-
			VLCD = 0Dh	1.35	1.45	1.53	V	-
			VLCD = 0Eh	1.40	1.50	1.58	V	-
			VLCD = 0Fh	1.45	1.55	1.63	V	-
			VLCD = 10h	1.50	1.60	1.68	V	-
			VLCD = 11h	1.55	1.65	1.73	V	-
			VLCD = 12h	1.60	1.70	1.78	V	-
			VLCD = 13h	1.65	1.75	1.83	V	-
Doubler output voltage	V_{L2}	C1 to C4*1 = 0.47 µF		$2 \times V_{L1}$ - 0.1	$2 \times V_{L1}$	$2 \times V_{L1}$	V	-
Tripler output voltage	V_{L4}	C1 to C4*1 = 0.47 µF		$3 \times V_{L1}$ - 0.15	$3 \times V_{L1}$	$3 \times V_{L1}$	V	-
Reference voltage setup time*2	t_{VL1S}			5	-	-	ms	Figure 2.81
LCD output voltage variation range*3	t_{VLWT}	C1 to C4*1 = 0.47 µF		500	-	-	ms	

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

2.15 Flash Memory Characteristics

2.15.1 Code Flash Memory Characteristics

Table 2.69 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	-	-	Times	-
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	-	-	Year	T_a = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be done n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.70 Code flash characteristics (2)
High-speed operating mode
Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P8}	-	116	998	-	54	506	µs
Erasure time	2-KB	t_{E2K}	-	9.03	287	-	5.67	222	ms
Blank check time	8-byte	t_{BC8}	-	-	56.8	-	-	16.6	µs
	2-KB	t_{BC2K}	-	-	1899	-	-	140	µs
Erase suspended time		t_{SED}	-	-	22.5	-	-	10.7	µs
Startup area switching setting time		t_{SAS}	-	21.7	585	-	12.1	447	ms
Access window time		t_{AWS}	-	21.7	585	-	12.1	447	ms
OCD/serial programmer ID setting time		t_{OSIS}	-	21.7	585	-	12.1	447	ms
Flash memory mode transition wait time 1		t_{DIS}	2	-	-	2	-	-	µs
Flash memory mode transition wait time 2		t_{MS}	5	-	-	5	-	-	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

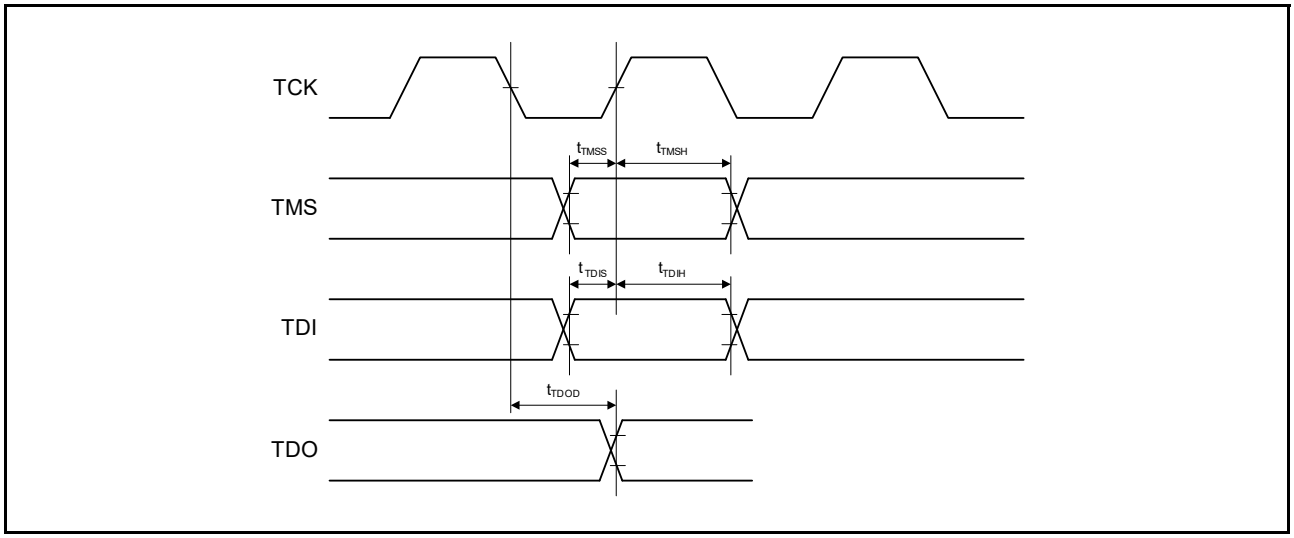


Figure 2.83 Boundary scan input/output timing

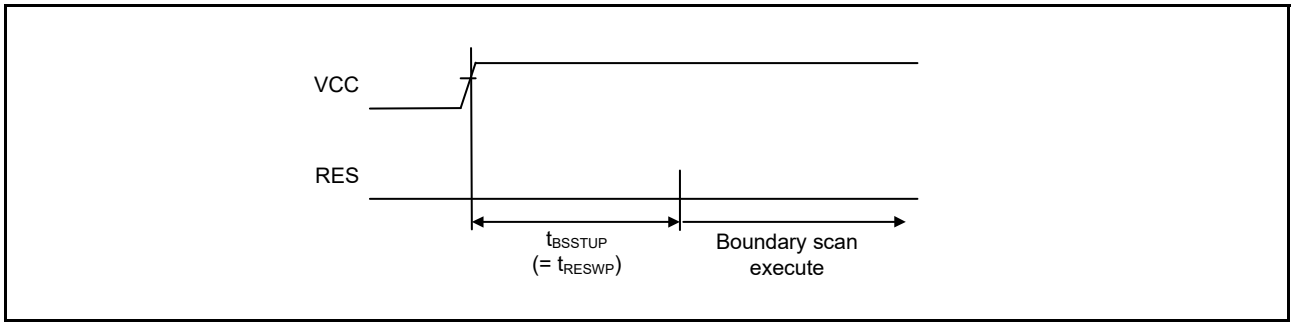


Figure 2.84 Boundary scan circuit start up timing

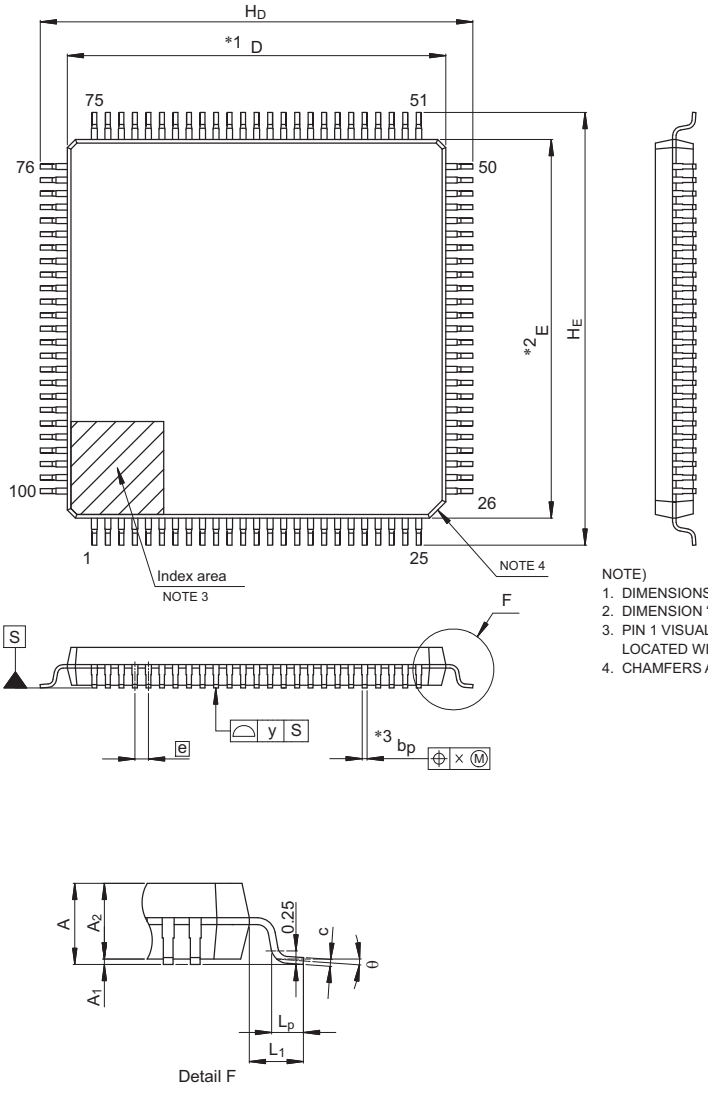
2.17 Joint Test Action Group (JTAG)

Table 2.76 JTAG (debug) characteristics (1)
Conditions: VCC = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	80	-	-	ns	Figure 2.85
TCK clock high pulse width	t_{TCKH}	35	-	-	ns	
TCK clock low pulse width	t_{TCKL}	35	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	16	-	-	ns	Figure 2.86
TMS hold time	t_{TMSH}	16	-	-	ns	
TDI setup time	t_{TDIS}	16	-	-	ns	
TDI hold time	t_{TDIH}	16	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	70	ns	

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.2 100-pin LQFP