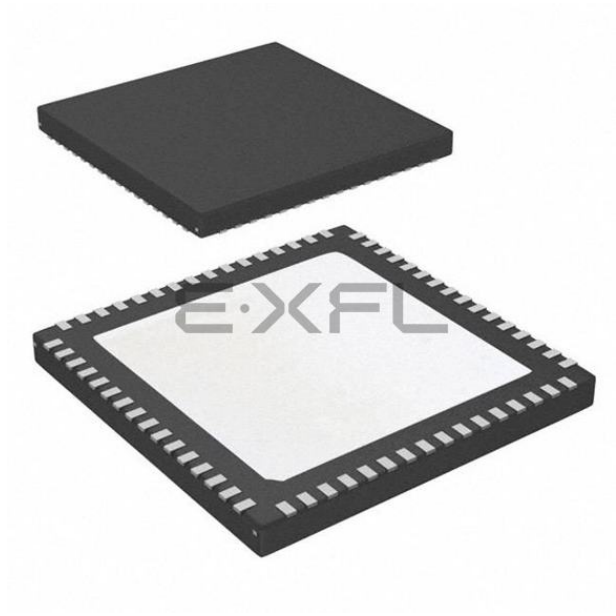
Renesas Electronics America Inc - R7FS3A6783A01CNB#AC0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 18x14b; D/A 3x8b, 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a6783a01cnb-ac0

Table 1.3 System (2 of 2)

Feature	Functional description
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 15, Memory Protection Unit (MPU) in User's Manual.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter. It can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and used as the condition to detect when the system runs out of control. See section 25, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. It can be used to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 26, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 18, Event Link Controller (ELC) in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 17, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	A 4-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 16, DMA Controller (DMAC) in User's Manual.

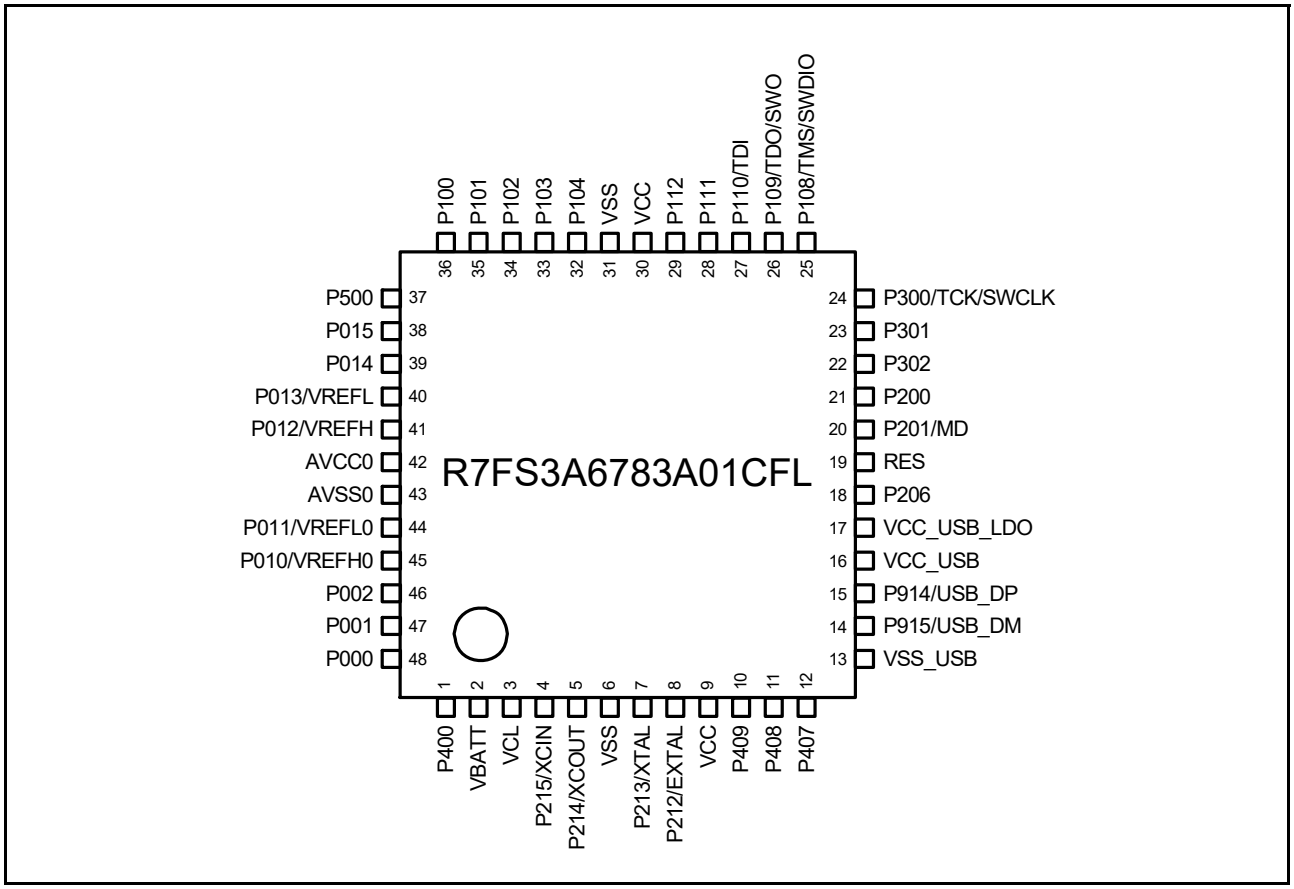


Figure 1.7 Pin assignment for 48-pin LQFP (top view)

2.2 DC Characteristics

2.2.1 Tj/T_a Definition

Table 2.3 DC Characteristics

Conditions: Products with operating temperature (T_a) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that Tj = T_a + θja × total power consumption (W),
where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

Note 1. The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section 1.3, Part Numbering. If the part number shows the operation temperature at 85°C, then the maximum value of T_j is +105°C, otherwise, it is +125°C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1)

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 5.5V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Schmitt trigger input voltage	IIC*1 (except for SMBus)	V_{IH}	VCC × 0.7	-	5.8	V	-
		V_{IL}	-	-	VCC × 0.3		
		ΔV_T	VCC × 0.05	-	-		
	RES, NMI Other peripheral input pins excluding IIC	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.1	-	-		
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	V_{IH}	2.2	-	-		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	-	-		VCC = 2.7 to 3.6 V
		V_{IL}	-	-	0.8		-
	5 V-tolerant ports*3	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	P000 to P008, P010 to P015	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	EXTAL Input ports pins except for P000 to P008, P010 to P015, P914, P915	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
When V_{BATT} power supply is selected	P402, P403, P404	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3		
		V_{IL}	-	-	V_{BATT} × 0.2		
		ΔV_T	V_{BATT} × 0.05	-	-		

Note 1. P205, P206, P400, P401, P407, P408 (total 6 pins).
Note 2. P100, P101, P204, P205, P206, P400, P401, P407, P408 (total 9 pins).
Note 3. P205, P206, P400 to P404, P407, P408 (total 9 pins).

Table 2.5 I/O V_{IH}, V_{IL} (2)

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6 to 2.7 V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Schmitt trigger input voltage	RES, NMI Peripheral input pins	V_{IH}	VCC × 0.8	-	-	V	-
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.01	-	-		
Input voltage (except for Schmitt trigger input pin)	5 V-tolerant ports*1	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	P000 to P008, P010 to P015	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	EXTAL Input ports pins except for P000 to P008, P010 to P015, P914, P915	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
When V_{BATT} power supply is selected	P402, P403, P404	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3		
		V_{IL}	-	-	V_{BATT} × 0.2		
		ΔV_T	V_{BATT} × 0.01	-	-		

Note 1. P205, P206, P400 to P404, P407, P408 (total 9 pins)

2.2.8 IIC I/O Pin Output Characteristics

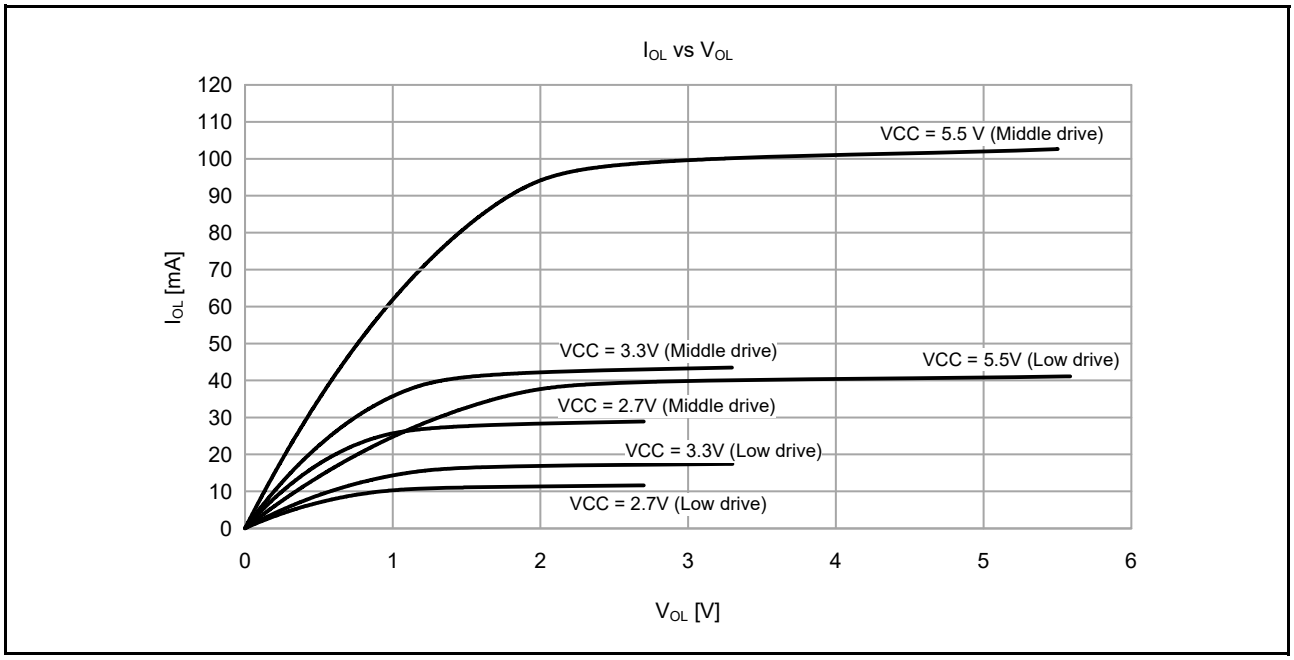


Figure 2.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C

Table 2.11 Operating and standby current (1) (2 of 2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test conditions
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 1 MHz	I_{CC}	0.4	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 1 MHz		0.6	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 1 MHz		1.0	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 1 MHz		-	2.2		
		Sleep mode	All peripheral clock disabled*5	ICLK = 1 MHz		0.3	-		*7
			All peripheral clock enabled*5	ICLK = 1 MHz		0.9	-		*8
	Low-voltage mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 4 MHz	I_{CC}	1.7	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 4 MHz		2.8	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 4 MHz		3.0	-		*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 4 MHz		-	8.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 4 MHz		1.3	-		*7
			All peripheral clock enabled*5	ICLK = 4 MHz		2.5	-		*8
	Subosc-speed mode*4	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 32.768 kHz	I_{CC}	8.5	-	µA	*8
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 32.768 kHz		14.9	-		
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 32.768 kHz		-	83.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32.768 kHz		5.0	-		
			All peripheral clock enabled*5	ICLK = 32.768 kHz		11.4	-		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64.
Note 8. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are the same frequency as that of ICLK.
Note 9. FCLK and PCLKB are set to divided by 2 and PCLKA, PCLKC, and PCLKD are the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.

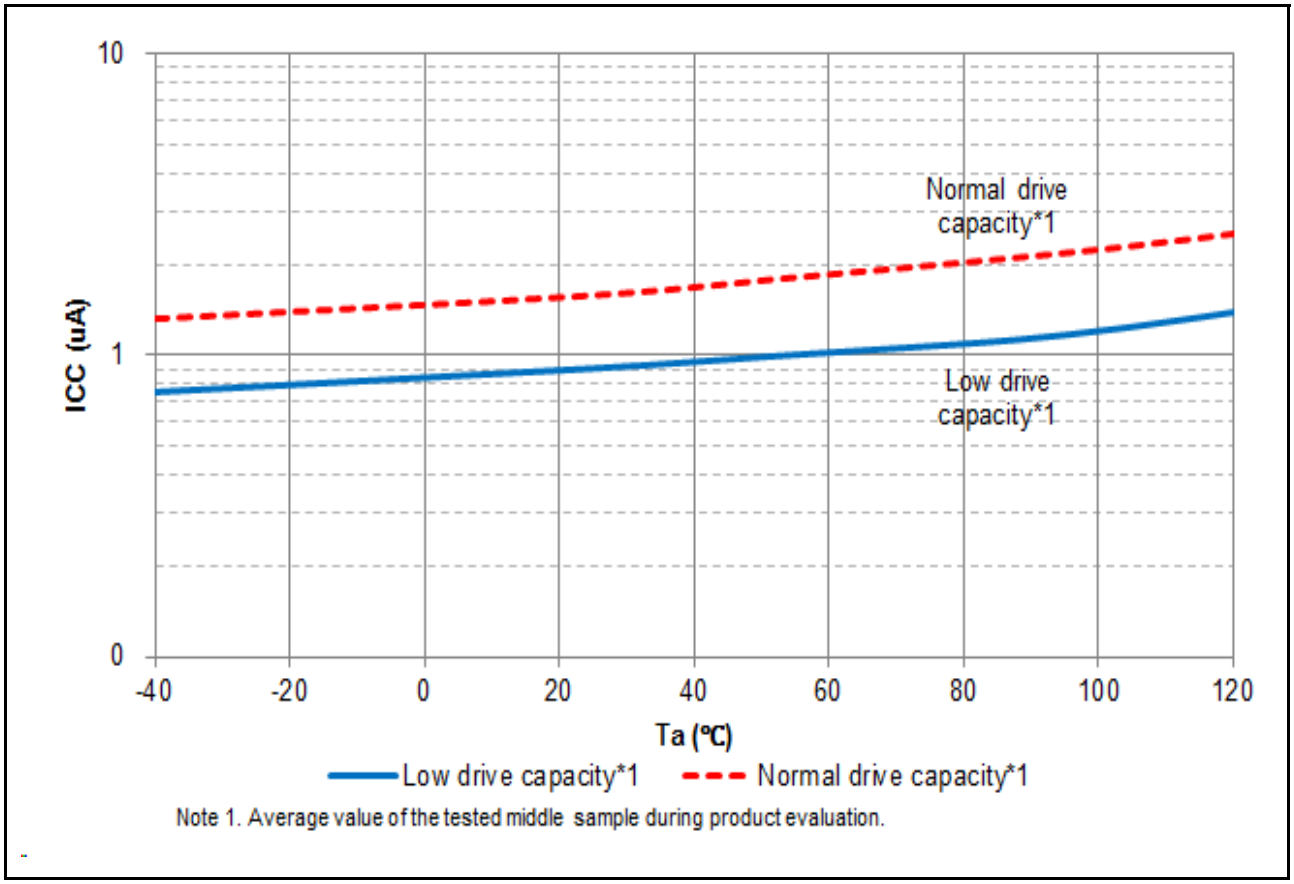


Figure 2.23 Temperature dependency of RTC operation with VCC off (reference data)

Table 2.14 Operating and standby current (4)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V, VREFH0 = 2.7 V to AVCC0

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During A/D conversion (at high-speed conversion)		I_{AVCC}	-	-	3.0	mA	-
	During A/D conversion (at low-power conversion)			-	-	1.0	mA	-
	During D/A conversion (per channel)*1			-	0.4	0.8	mA	-
	Waiting for A/D and D/A conversion (all units)*6			-	-	1.0	µA	-
Reference power supply current	During A/D conversion		I_{REFH0}	-	-	150	µA	-
	Waiting for A/D conversion (all units)			-	-	60	nA	-
	During D/A conversion		I_{REFH}	-	50	100	µA	-
	Waiting for D/A conversion (all units)			-	-	100	µA	-
Temperature sensor			I_{TNS}	-	75	-	µA	-
Low-Power Analog Comparator operating current	Window mode		I_{CMPLP}	-	15	-	µA	-
	Comparator High-speed mode			-	10	-	µA	-
	Comparator Low-speed mode			-	2	-	µA	-
	Comparator Low-speed mode using DAC8			-	820	-	µA	-
Operational Amplifier operating current	Low power mode	1 unit operating	I_{AMP}	-	2.5	4.0	µA	-
		2 units operating		-	4.5	8.0	µA	-
		3 units operating		-	6.5	11.0	µA	-
		4 units operating		-	8.5	14.0	µA	-
	High-speed mode	1 unit operating		-	140	220	µA	-
		2 units operating		-	280	410	µA	-
		3 units operating		-	420	600	µA	-
		4 units operating		-	560	780	µA	-
LCD operating current	External resistance division method $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice		I_{LCD1}*5	-	0.34	-	µA	-
	Internal voltage boosting method (VLCD.VLCD = 04) $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice		I_{LCD2}*5	-	0.92	-	µA	-
	Capacitor split method $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice		I_{LCD3}*5	-	0.19	-	µA	-
USB operating current	During USB communication operation under the following settings and conditions: • Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect peripheral devices via a 1-meter USB cable from the USB port.		I_{USBH}*2	-	4.3 (VCC) 0.9 (VCC_USB)*4	-	mA	-
	During USB communication operation under the following settings and conditions: • Device controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect the host device via a 1-meter USB cable from the USB port.		I_{USBF}*2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-
	During suspended state under the following setting and conditions: • Device controller operation is set to full-speed mode (pull up the USB_DP pin) • Software standby mode • Connect the host device via a 1-meter USB cable from the USB port.		I_{SUSP}*3	-	0.35 (VCC) 170 (VCC_USB)*4	-	µA	-

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. Current consumed only by the USBFS.
Note 3. Includes the current supplied from the pull-up resistor of the USB_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU during the suspended state.
Note 4. When VCC = VCC_USB = 3.3 V.
Note 5. Current flowing only to the LCD controller. Not including the current that flows through the LCD panel.
Note 6. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC140 module stop bit) is in the module-stop state.

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.22, Clock timing.

Table 2.19 Operation frequency value in Low-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*3	1.8 to 5.5 V	f	0.032768	-	1	MHz
	Flash interface clock (FCLK)*1, *3	1.8 to 5.5 V		0.032768	-	1	
	Peripheral module clock (PCLKA)*3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKC)*2, *3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory.
Note 2. The lower-limit frequency of PCLKC is 1 MHz when the A/D converter is in use.
Note 3. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.22, Clock timing.

Table 2.20 Operation frequency value in low-voltage mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*4	1.6 to 5.5 V	f	0.032768	-	4	MHz
	Flash interface clock (FCLK)*1, *2, *4	1.6 to 5.5 V		0.032768	-	4	
	Peripheral module clock (PCLKA)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKB)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKC)*3, *4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKD)*4	1.6 to 5.5 V		-	-	4	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-Bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.22, Clock timing.

2.3.5 NMI and IRQ Noise Filter

Table 2.30 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 12, 14, 15).

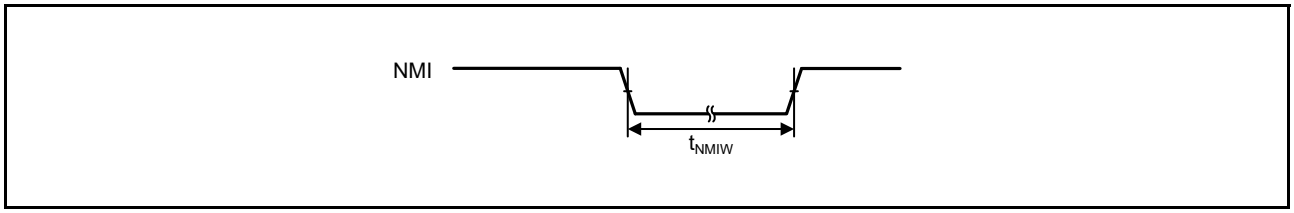


Figure 2.36 NMI interrupt input timing

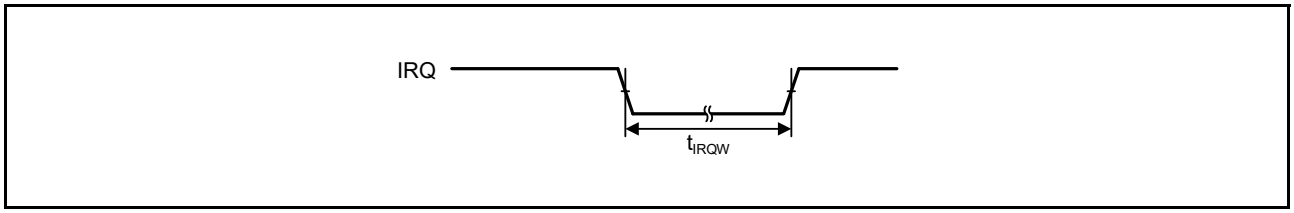


Figure 2.37 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 Trigger Timing

Table 2.31 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.38
	Input/output data cycle (P002, P003, P004, P007)		t_{POcyc}	10	-	us	
POEG	POEG input trigger pulse width		t_{POEW}	3	-	t_{Pcyc}	Figure 2.39
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.40
		Dual edge		2.5	-		
AGT	AGTIO, AGTEE input cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	-	ns	Figure 2.41
		2.4 V ≤ VCC < 2.7 V		500	-	ns	
		1.8 V ≤ VCC < 2.4 V		1000	-	ns	
		1.6 V ≤ VCC < 1.8 V		2000	-	ns	
	AGTIO, AGTEE input high level width, low-level width	2.7 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	-	ns	
		2.4 V ≤ VCC < 2.7 V		200	-	ns	
		1.8 V ≤ VCC < 2.4 V		400	-	ns	
		1.6 V ≤ VCC < 1.8 V		800	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	-	ns	Figure 2.41
		2.4 V ≤ VCC < 2.7 V		125	-	ns	
		1.8 V ≤ VCC < 2.4 V		250	-	ns	
		1.6 V ≤ VCC < 1.8 V		500	-	ns	
ADC14	14-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.42
KINT	KRn (n = 00 to 07) pulse width		t_{KR}	250	-	ns	Figure 2.43

Note 1. Constraints on AGTIO input: $t_{Pcyc} \times 2 < t_{ACYC}$

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle

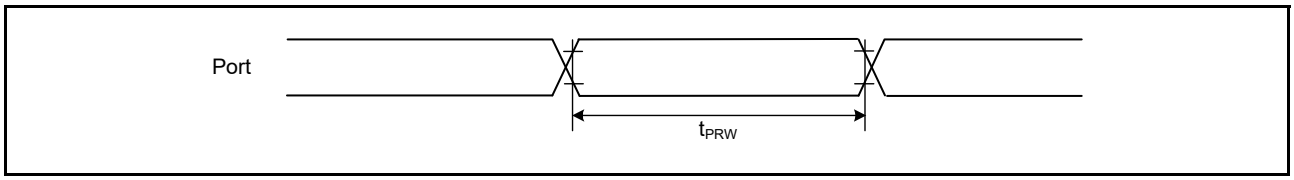


Figure 2.38 I/O ports input timing

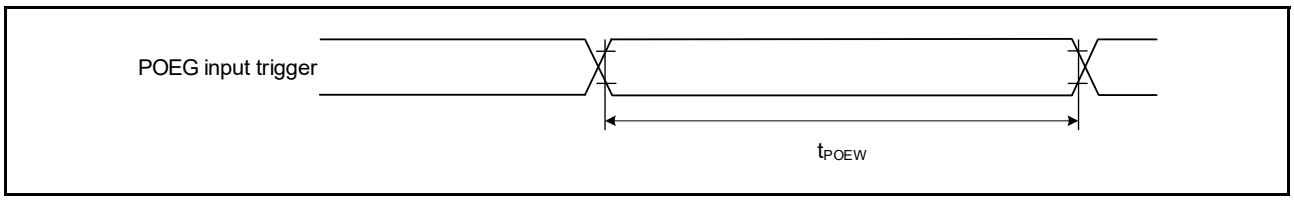


Figure 2.39 POEG input trigger timing

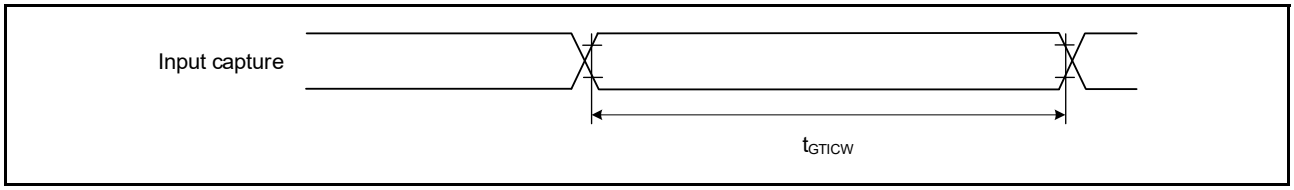


Figure 2.40 GPT input capture timing

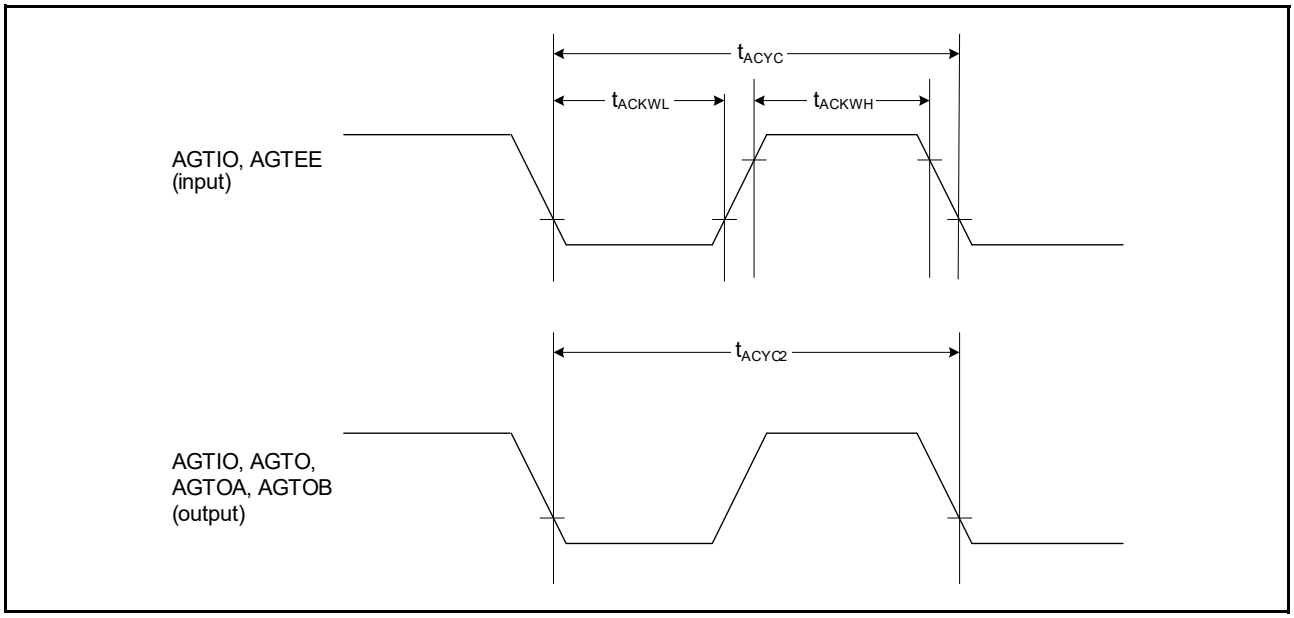


Figure 2.41 AGT I/O timing

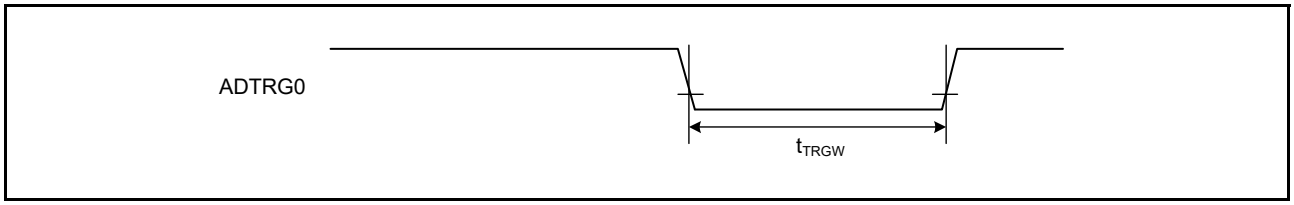


Figure 2.42 ADC14 trigger input timing

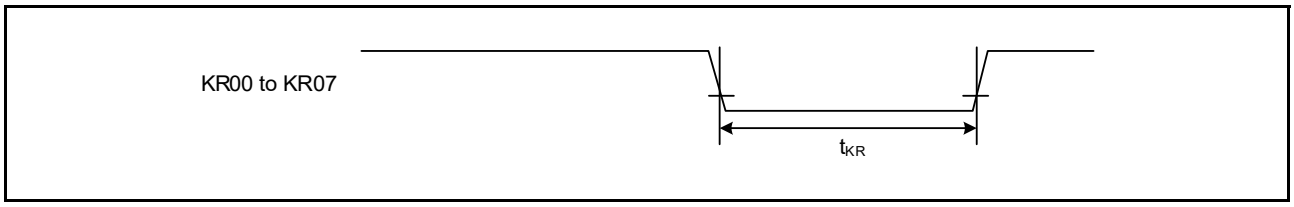


Figure 2.43 Key interrupt input timing

2.3.7 CAC Timing

Table 2.32 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{PBcyc}*1 ≤ t_{cac}*2	t_{CACREF}	4.5 × t_{cac} + 3 × t_{PBcyc}*1	-	-	ns	-
		t_{PBcyc}*1 > t_{cac}*2		5 × t_{cac} + 6.5 × t_{PBcyc}*1	-	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. t_{cac}: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.33 SCI timing (1)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous		t_{Scyc}	4	-	t_{Pcyc}	Figure 2.44
		Clock synchronous			6	-		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	-	20	ns	
	Input clock fall time			t_{SCKf}	-	20	ns	
	Output clock cycle	Asynchronous		t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous			4	-		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V or above	t_{SCKr}	-	20	ns	
			1.6 V or above		-	30		
	Output clock fall time		1.8 V or above	t_{SCKf}	-	20	ns	
			1.6 V or above		-	30		
	Transmit data delay (master)	Clock synchronous	1.8 V or above	t_{TXD}	-	40	ns	Figure 2.45
			1.6 V or above		-	45		
	Transmit data delay (slave)	Clock synchronous	2.7 V or above		-	55	ns	
			2.4 V or above		-	60		
			1.8 V or above		-	100		
			1.6 V or above		-	125		
	Receive data setup time (master)	Clock synchronous	2.7 V or above	t_{RXS}	45	-	ns	
			2.4 V or above		55	-		
			1.8 V or above		90	-		
			1.6 V or above		110	-		
	Receive data setup time (slave)	Clock synchronous	2.7 V or above		40	-	ns	
			1.6 V or above		45	-		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	-	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

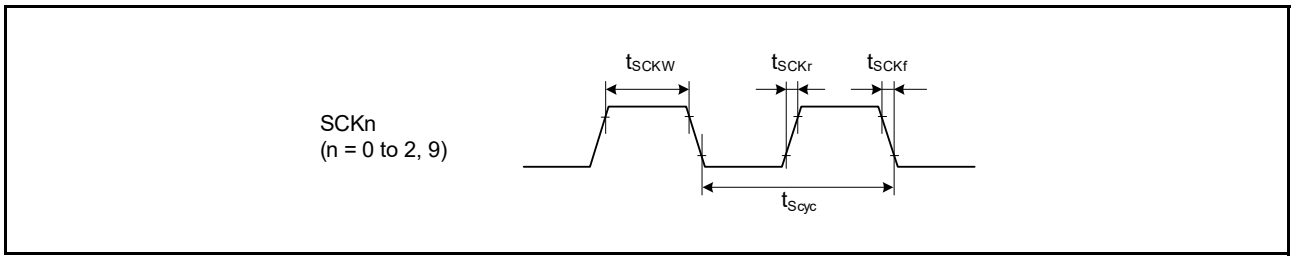


Figure 2.44 SCK clock input timing

Table 2.36 SPI timing (2 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in PmnPFS register

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	Data output delay	Master	2.7 V or above	t_{OD}	-	14	ns	Figure 2.53 to Figure 2.58
			2.4 V or above		-	20		
			1.8 V or above		-	25		
			1.6 V or above		-	30		
		Slave	2.7 V or above		-	50		
			2.4 V or above		-	60		
			1.8 V or above		-	85		
			1.6 V or above		-	110		
	Data output hold time	Master		t_{OH}	0	-	ns	
		Slave			0	-		
	Successive transmission delay	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			6 × t_{Pcyc}	-		
	MOSI and MISO rise and fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	-	10	ns	
			2.4 V or above		-	15		
			1.8 V or above		-	20		
			1.6 V or above		-	30		
		Input			-	1	µs	
	SSL rise and fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	-	10	ns	
			2.4 V or above		-	15		
			1.8 V or above		-	20		
			1.6 V or above		-	30		
		Input			-	1	µs	
	Slave access time		2.4 V or above	t_{SA}	-	2 × t_{Pcyc} + 100	ns	Figure 2.57 and Figure 2.58
			1.8 V or above		-	2 × t_{Pcyc} + 140		
			1.6 V or above		-	2 × t_{Pcyc} + 180		
	Slave output release time		2.4 V or above	t_{REL}	-	2 × t_{Pcyc} + 100	ns	
			1.8 V or above		-	2 × t_{Pcyc} + 140		
			1.6 V or above		-	2 × t_{Pcyc} + 180		

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.
Note 4. The upper limit of RSPCK is 16 MHz.

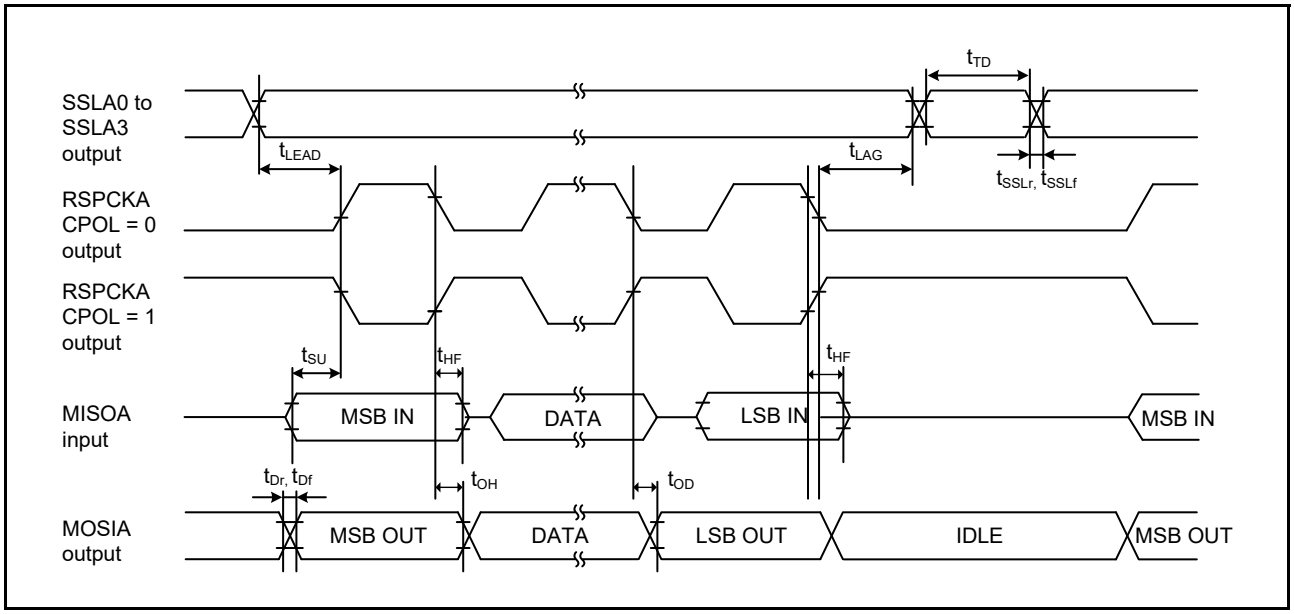


Figure 2.54 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

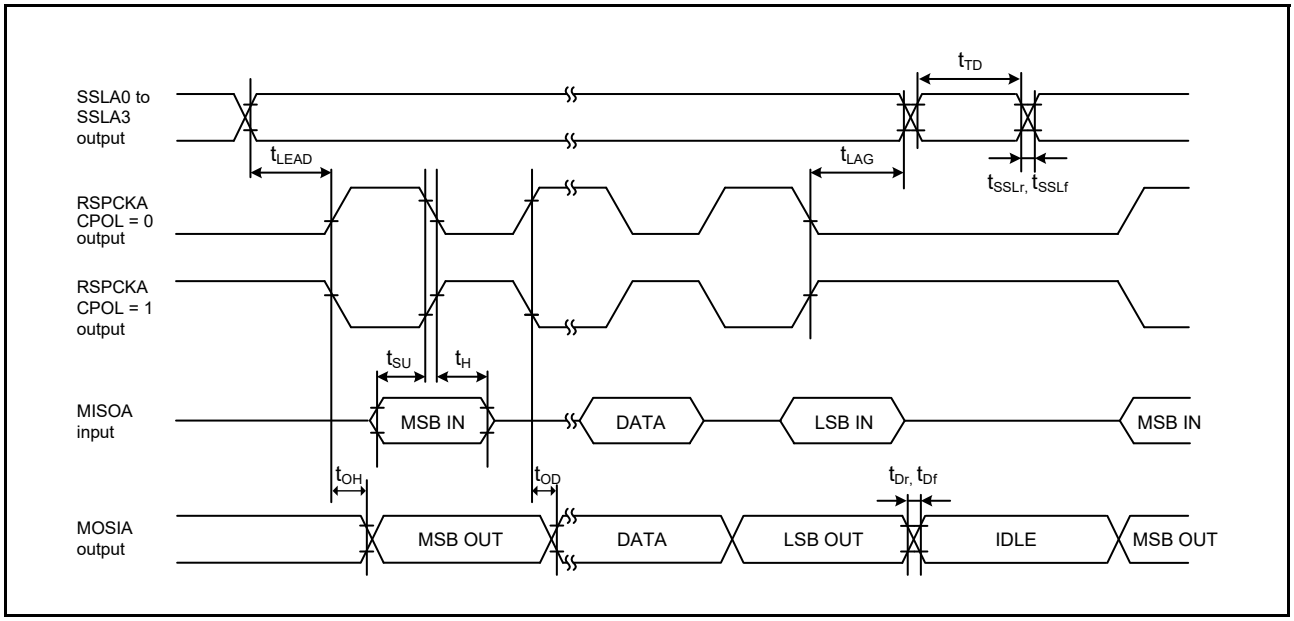
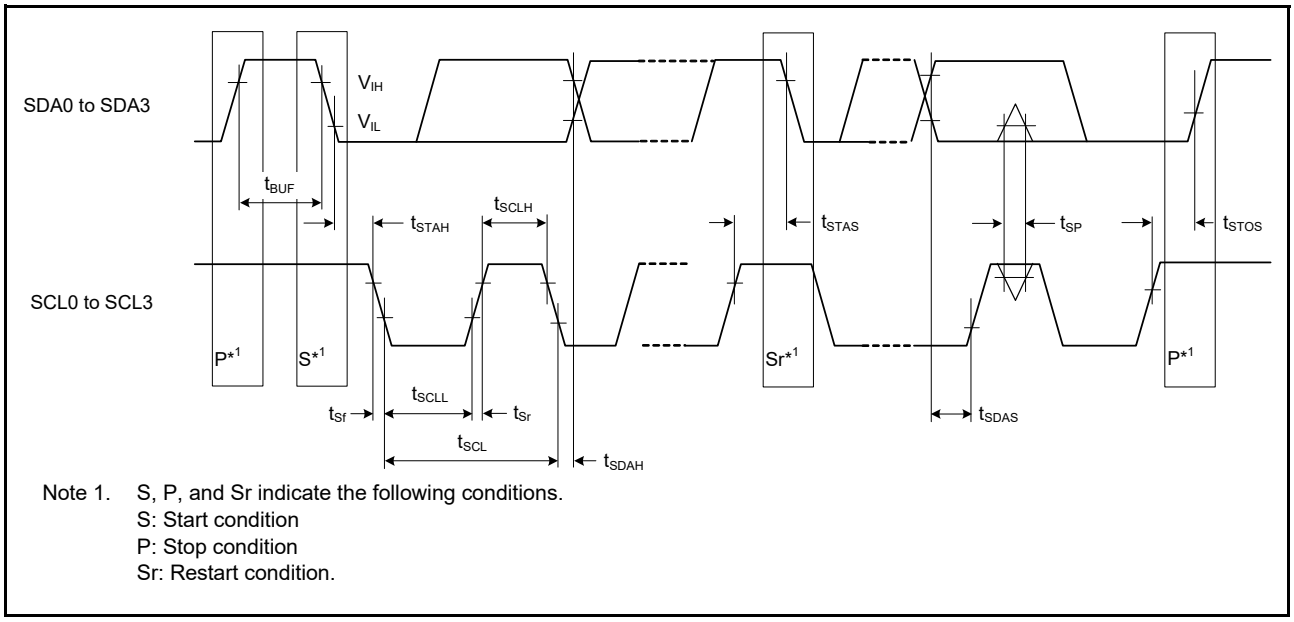


Figure 2.55 SPI timing for master when CPHA = 1 and the bit rate is set to any value other than PCLKA/2

Table 2.37 IIC timing (2 of 2)
Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.59 For all ports except P408, use PmnPFS.DSCR of middle drive. For port P408, use PmnPFS.DSCR1/DSCR of middle drive for IIC fast-mode.
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	300	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle
Note 1. The value in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition.

Figure 2.59 IIC bus interface input/output timing

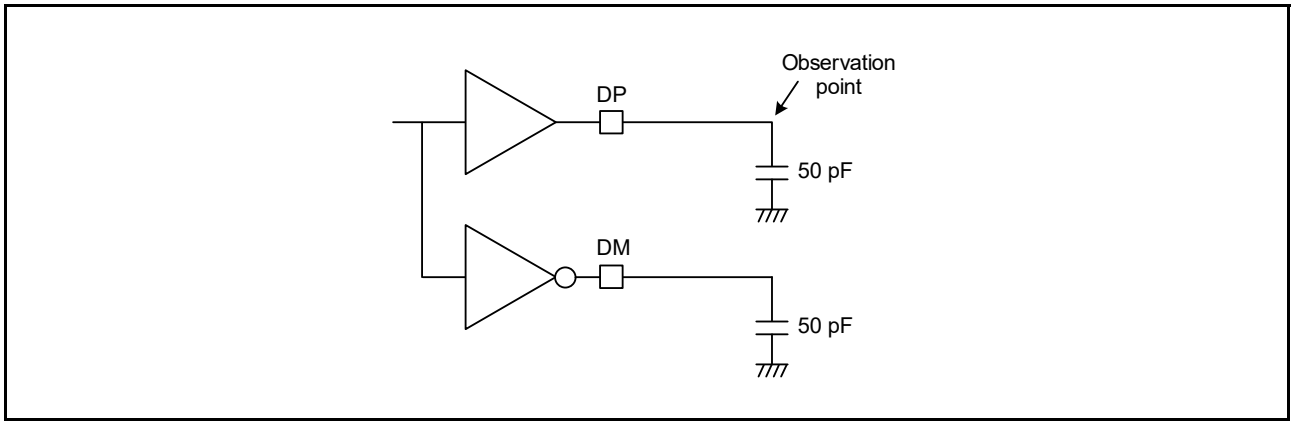


Figure 2.66 Test circuit for Full-Speed (FS) connection

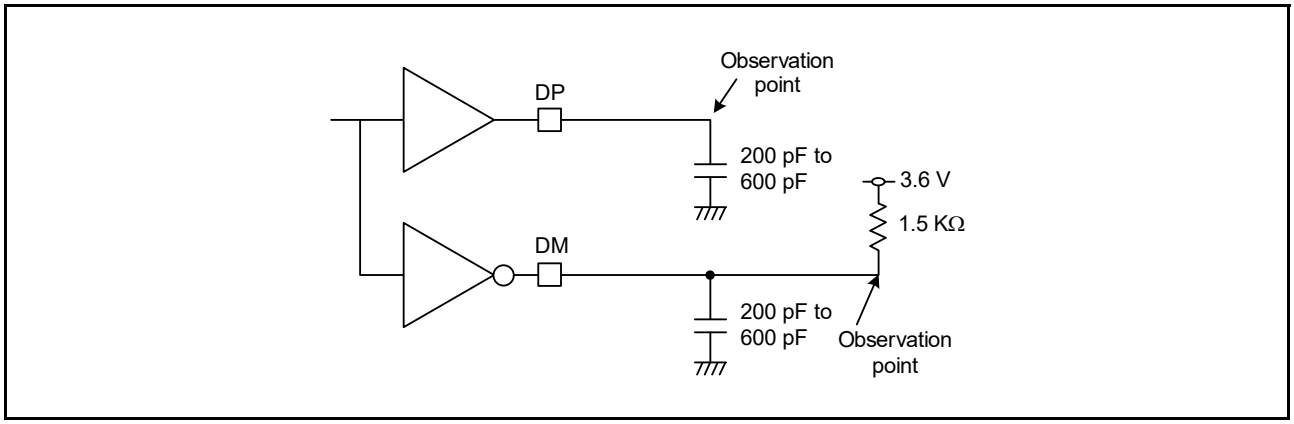


Figure 2.67 Test circuit for Low-Speed (LS) connection

2.4.2 USB External Supply

Table 2.41 USB regulator

Parameter		Min	Typ	Max	Unit	Test conditions
VCC_USB supply current	VCC_USB_LDO ≥ 3.8V	-	-	50	mA	-
	VCC_USB_LDO ≥ 4.5V	-	-	100	mA	-
VCC_USB supply voltage		3.0	-	3.6	V	-

Table 2.42 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time*1 (Operation at PCLKC = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.80	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.22	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (C_{in}), see section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics.

Table 2.43 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	48	MHz	-
Analog input capacitance*2		Cs	-	-	8 (reference data)	pF	High-precision channel
			-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance		Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
			-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range		Ain	0	-	VREFH0	V	-
12-bit mode							
Resolution			-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ		0.94	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
			1.50	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error			-	±0.5	±4.5	LSB	High-precision channel
					±6.0	LSB	Other than above
Full-scale error			-	±0.75	±4.5	LSB	High-precision channel
					±6.0	LSB	Other than above
Quantization error			-	±0.5	-	LSB	-
Absolute accuracy			-	±1.25	±5.0	LSB	High-precision channel
					±8.0	LSB	Other than above
DNL differential nonlinearity error			-	±1.0	-	LSB	-
INL integral nonlinearity error			-	±1.0	±3.0	LSB	-

Table 2.46 A/D conversion characteristics (5) in low power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.75	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.44	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (C_{in}), see section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics.

Table 2.47 A/D conversion characteristics (6) in low power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	8	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	3.8 (reference data)	kΩ	High-precision channel
		-	-	8.2 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	6.75	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.13	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h

2.14 OPAMP Characteristics

Table 2.68 OPAMP characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Common mode input range	Vicm1	Low power mode		0.2	-	AVCC0 - 0.5	V
	Vicm2	High-speed mode		0.3	-	AVCC0 - 0.6	V
Output voltage range	Vo1	Low power mode		0.1	-	AVCC0 - 0.1	V
	Vo2	High-speed mode		0.1	-	AVCC0 - 0.1	V
Input offset voltage	Vioff	3σ		-10	-	10	mV
Open gain	Av			60	120	-	dB
Gain-bandwidth (GB) product	GBW1	Low power mode		-	0.04	-	MHz
	GBW2	High-speed mode		-	1.7	-	MHz
Phase margin	PM	CL = 20 pF		50	-	-	deg
Gain margin	GM	CL = 20 pF		10	-	-	dB
Equivalent input noise	Vnoise1	f = 1 kHz	Low power mode	-	230	-	nV/√Hz
	Vnoise2	f = 10 kHz		-	200	-	nV/√Hz
	Vnoise3	f = 1 kHz	High-speed mode	-	90	-	nV/√Hz
	Vnoise4	f = 2 kHz		-	70	-	nV/√Hz
Power supply reduction ratio	PSRR			-	90	-	dB
Common mode signal reduction ratio	CMRR			-	90	-	dB
Stabilization wait time	Tstd1	CL = 20 pF Only operational amplifier is activated *1	Low power mode	650	-	-	µs
	Tstd2		High-speed mode	13	-	-	µs
	Tstd3	CL = 20 pF Operational amplifier and reference current circuit are activated simultaneously	Low power mode	650	-	-	µs
	Tstd4		High-speed mode	13	-	-	µs
Settling time	Tset1	CL = 20 pF	Low power mode	-	-	750	µs
	Tset2		High-speed mode	-	-	13	µs
Slew rate	Tslew1	CL = 20 pF	Low power mode	-	0.02	-	V/µs
	Tslew2		High-speed mode	-	1.1	-	V/µs
Load current	Iload1	Low-power mode		-100	-	100	µA
	Iload2	High-speed mode		-100	-	100	µA
Load capacitance	CL			-	-	20	pF

Note 1. When the operational amplifier reference current circuit is activated in advance.