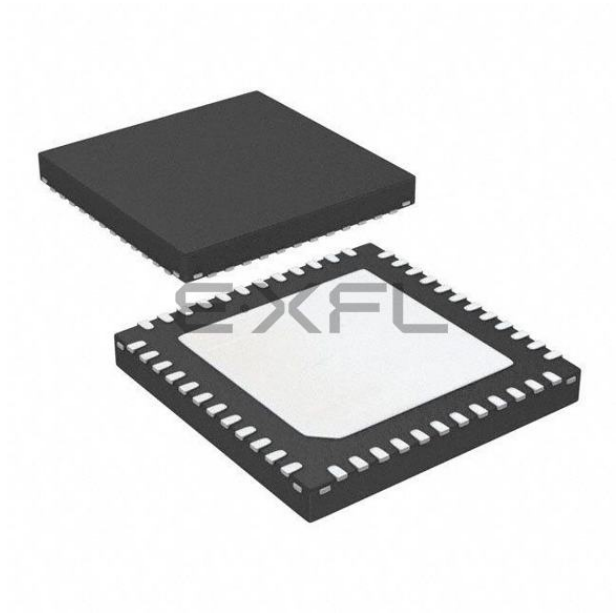
Renesas Electronics America Inc - R7FS3A6783A01CNE#AC0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 14x14b; D/A 3x8b, 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a6783a01cne-ac0

High efficiency 48-MHz Arm® Cortex®-M4 core, 256-KB code flash memory, 32-KB SRAM, Segment LCD Controller, Capacitive Touch Sensing Unit, USB 2.0 Full-Speed Module, 14-bit A/D Converter, 12-bit D/A Converter, security and safety features

Features

■ Arm Cortex-M4 Core with Floating Point Unit (FPU)
- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 48 MHz
- Support for 4-GB address space
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: ITM, DWT, FPB, TPIU, ETB
- CoreSight™ Debug Port: JTAG-DP and SW-DP

■ Memory
- 256-KB code flash memory
- 8-KB data flash memory (100,000 program/erase (P/E) cycles)
- 32-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Unit (MPU)
- 128-bit unique ID

■ Connectivity
- USB 2.0 Full-Speed Module (USBFS)
  - On-chip transceiver with voltage regulator
  - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 4
  - UART
  - Simple IIC
  - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 2
- Controller Area Network (CAN) module
- Serial Sound Interface Enhanced (SSIE)

■ Analog
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- 8-bit D/A Converter (DAC8) ×2 (for ACMPLP)
- Low-Power Analog Comparator (ACMPLP) × 2
- Operational Amplifier (OPAMP) × 4
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-Bit (GPT32) × 2
- General PWM Timer 16-Bit (GPT16) × 6
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management
- Low power modes
- Realtime Clock (RTC) with calendar and Battery Backup support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 4
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption
- AES128/256
- GHASH
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)
- Segment LCD Controller (SLCDC)
  - Up to 38 segments × 4 commons
  - Up to 34 segments × 8 commons
- Capacitive Touch Sensing Unit (CTSU)

■ Multiple Clock Sources
- Main clock oscillator (MOSC)
  (1 to 20 MHz when VCC = 2.4 to 5.5 V)
  (1 to 8 MHz when VCC = 1.8 to 2.4 V)
  (1 to 4 MHz when VCC = 1.6 to 1.8 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
  (24, 32, 48, 64 MHz when VCC = 2.4 to 5.5 V)
  (24, 32, 48 MHz when VCC = 1.8 to 5.5 V)
  (24, 32 MHz when VCC = 1.6 to 5.5 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General Purpose I/O Ports
- Up to 84 input/output pins
  - Up to 3 CMOS input
  - Up to 81 CMOS input/output
    - Up to 9 input/output 5-V tolerant
    - Up to 2 high current (20 mA)

■ Operating Voltage
- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages
- Ta = -40°C to +85°C
  - 100-pin LGA (7 mm × 7 mm, 0.65 mm pitch)
- Ta = -40°C to +105°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 40-pin QFN (6 mm × 6 mm, 0.5 mm pitch)

Table 1.3 System (2 of 2)

Feature	Functional description
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 15, Memory Protection Unit (MPU) in User's Manual.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter. It can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and used as the condition to detect when the system runs out of control. See section 25, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. It can be used to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 26, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 18, Event Link Controller (ELC) in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 17, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	A 4-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 16, DMA Controller (DMAC) in User's Manual.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 32, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 42, Data Operation Circuit (DOC) in User's Manual.

Table 1.11 Security

Feature	Functional description
Secure Crypto Engine 5 (SCE5)	• Security algorithm - Symmetric algorithm: AES. • Other support features - TRNG (True Random Number Generator) - Hash-value generation: GHASH.

1.4 Function Comparison

Table 1.13 Function comparison

Part numbers		R7FS3A6783A01CFP	R7FS3A6782A01CLJ	R7FS3A6783A01CFM/ R7FS3A6783A01CNB	R7FS3A6783A01CFL/ R7FS3A6783A01CNE	R7FS3A6783A01CNF
Pin count		100	100	64	48	40
Package		LQFP	LGA	LQFP/QFN	LQFP/QFN	QFN
Code flash memory		256 KB				
Data flash memory		8 KB				
SRAM		32 KB				
	Parity	16 KB				
	ECC	16 KB				
System	CPU clock	48 MHz				
	Backup registers	512 bytes				
	ICU	Yes				
	KINT	8			5	3
Event control	ELC	Yes				
DMA	DTC	Yes				
	DMAC	4				
Bus	External bus	No				
Timers	GPT32	2				
	GPT16	6			4	2
	AGT	2			No	
	RTC	Yes				
	WDT/IWDT	Yes				
Communication	SCI	4				
	IIC	2				
	SPI	2				1
	SSIE	1		No		
	QSPI	No				
	SDHI	No				
	CAN	1				
	USBFS	Yes				
Analog	ADC14	25		18	14	11
	DAC12	1				
	DAC8	2				
	ACMPLP	2				1
	OPAMP	4	4	3	1	No
	TSN	Yes				
HMI	SLCDC	4 com × 38 seg or 8 com × 34 seg		4 com × 21 seg or 8 com × 17 seg	No	
	CTSU	27		24	15	10
Data processing	CRC	Yes				
	DOC	Yes				
Security		SCE5				

Table 1.14 Pin functions (4 of 4)

Function	Signal	I/O	Description
I/O ports	P000 to P008, P010 to P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201 to P206, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P307	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P505	I/O	General-purpose input/output pins
	P600 to P603, P608 to P610	I/O	General-purpose input/output pins
	P708	I/O	General-purpose input/output pins
	P808, P809	I/O	General-purpose input/output pins
	P914, P915	I/O	General-purpose input/output pins
SLCDC	VL1, VL2, VL3, VL4	I/O	Voltage pin for driving the LCD
	CAPH, CAPL	I/O	Capacitor connection pin for the LCD controller/driver
	COM0 to COM7	Output	Common signal output pins for the LCD controller/driver
	SEG00 to SEG37	Output	Segment signal output pins for the LCD controller/driver

R7FS3A6782A01CLJ

	A	B	C	D	E	F	G	H	J	K	
10	P407	P409	P412	VCC	P212/ EXTAL	P215/ XCIN	VCL	P403	P400	P000	10
9	P915/ USB_DM	P914/ USB_DP	P413	VSS	P213/ XTAL	P214/ XCOUT	VBATT	P405	P401	P001	9
8	VCC_ USB	VSS_ USB	VCC_USB_LDO	P411	P415	P708	P404	P003	P004	P002	8
7	P205	P204	P206	P408	P414	P406	P006	P007	P008	P005	7
6	VSS	VCC	P202	P203	P410	P402	P505	AVSS 0	P011/ VREFL0	P010/ VREFH0	6
5	P200	P201/MD	P307	RES	P113	P600	P504	AVCC0	P013/ VREFL	P012/ VREFH	5
4	P305	P304	P808	P306	P115	P601	P503	P100	P015	P014	4
3	P809	P303	P110/TDI	P111	P609	P602	P107	P103	VSS	VCC	3
2	P300/ TCK/ SWCLK	P302	P301	P114	P610	P603	P106	P101	P501	P502	2
1	P108/ TMS/ SWDIO	P109/ TDO/ SWO	P112	P608	VCC	VSS	P105	P104	P102	P500	1
	A	B	C	D	E	F	G	H	J	K	

Figure 1.4 Pin assignment for 100-pin LGA (upper perspective view)

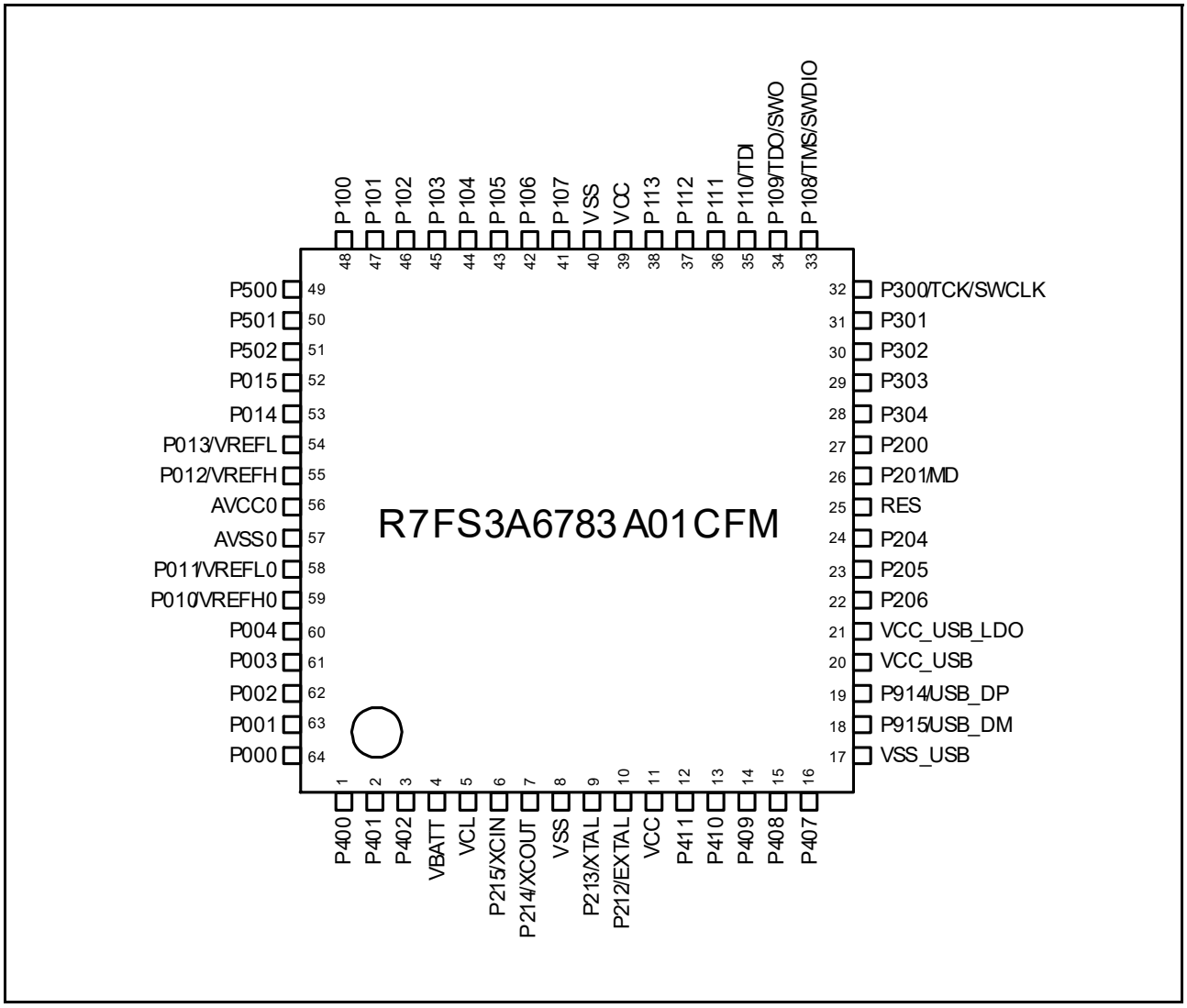


Figure 1.5 Pin assignment for 64-pin LQFP (top view)

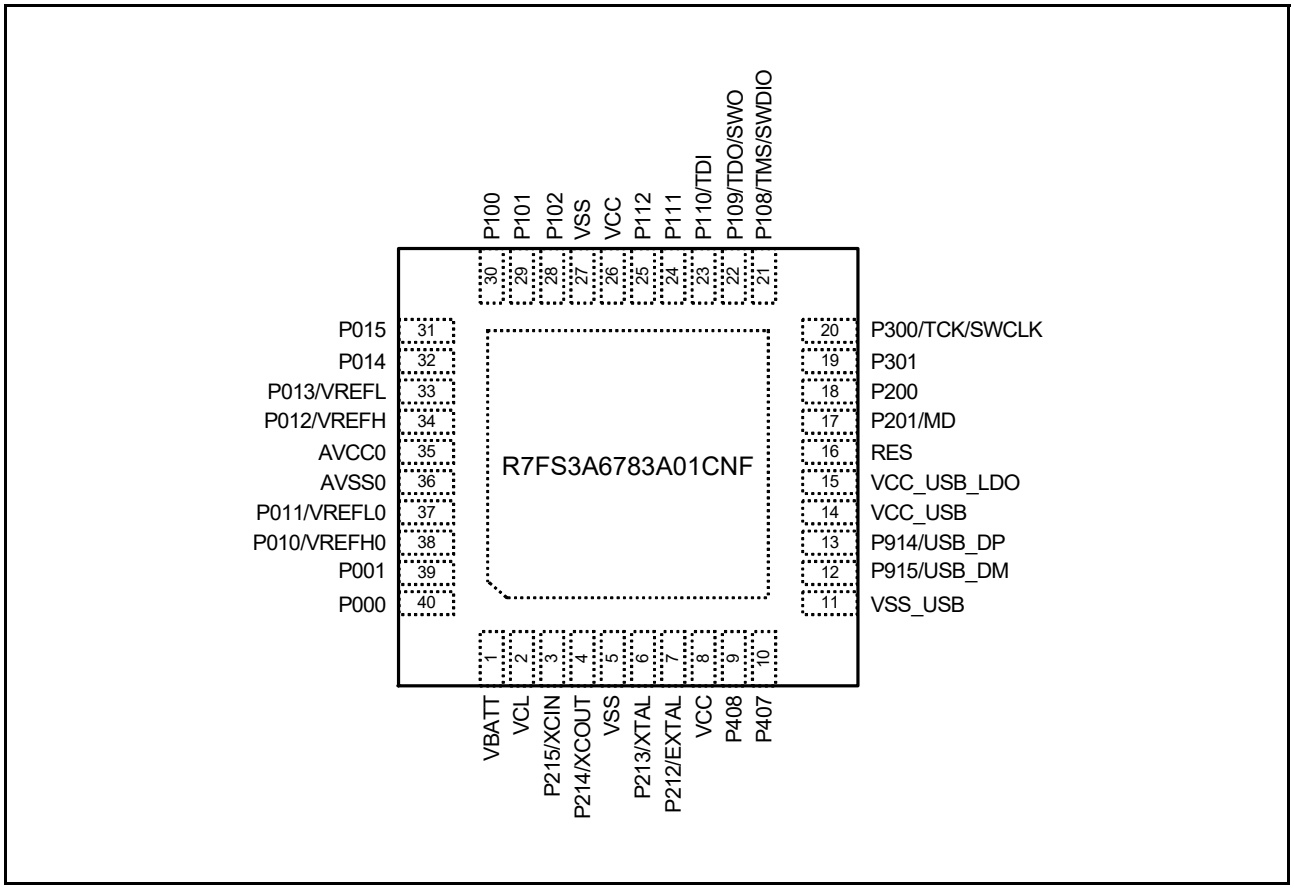


Figure 1.9 Pin assignment for 40-pin QFN (top view)

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
Input voltage	5 V-tolerant ports*1	V_{in}	-0.3 to +6.5	V
	P000 to P008, P010 to P015	V_{in}	-0.3 to AVCC0 + 0.3	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +6.5	V
		VREFH		V
VBATT power supply voltage		VBATT	-0.5 to +6.5	V
Analog power supply voltage		AVCC0	-0.5 to +6.5	V
USB power supply voltage		VCC_USB	-0.5 to +6.5	V
		VCC_USB_LDO	-0.5 to +6.5	V
Analog input voltage	When AN000 to AN014 are used	V_{AN}	-0.3 to AVCC0 + 0.3	V
	When AN016 to AN025 are used		-0.3 to VCC + 0.3	V
LCD voltage	VL1 voltage	V_{L1}	-0.3 to +2.8	V
	VL2 voltage	V_{L2}	-0.3 to +6.5	V
	VL3 voltage	V_{L3}	-0.3 to +6.5	V
	VL4 voltage	V_{L4}	-0.3 to +6.5	V
Operating temperature*2,*3,*4		T_{opr}	-40 to +105	°C
			-40 to +85	
Storage temperature		T_{stg}	-55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, and between the VREFH and VREFL pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.
Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. The capacitor must be placed close to the pin.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

Note 1. Ports P205, P206, P400 to P404, P407, P408 are 5 V tolerant.
Note 2. See section 2.2.1, Tj/Ta Definition.
Note 3. Contact a Renesas Electronics sales office for information on derating operation under T_a = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
Note 4. The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section 1.3, Part Numbering.

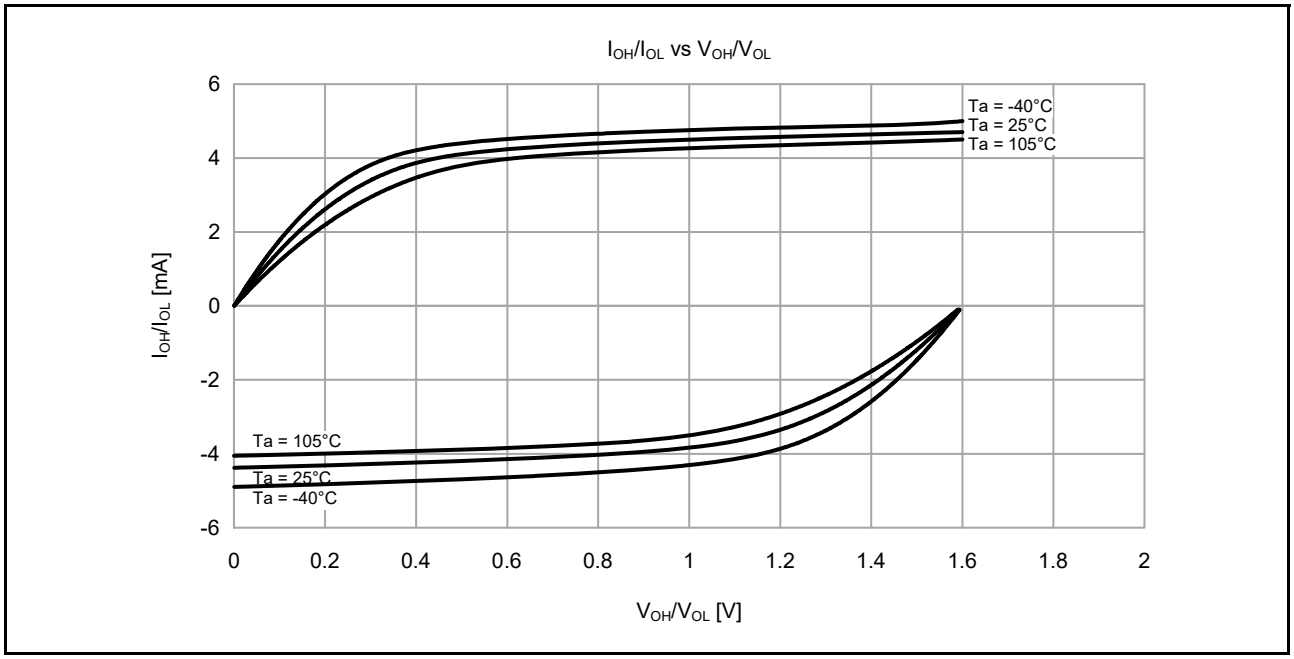


Figure 2.8 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.6 V when middle drive output is selected (reference data)**

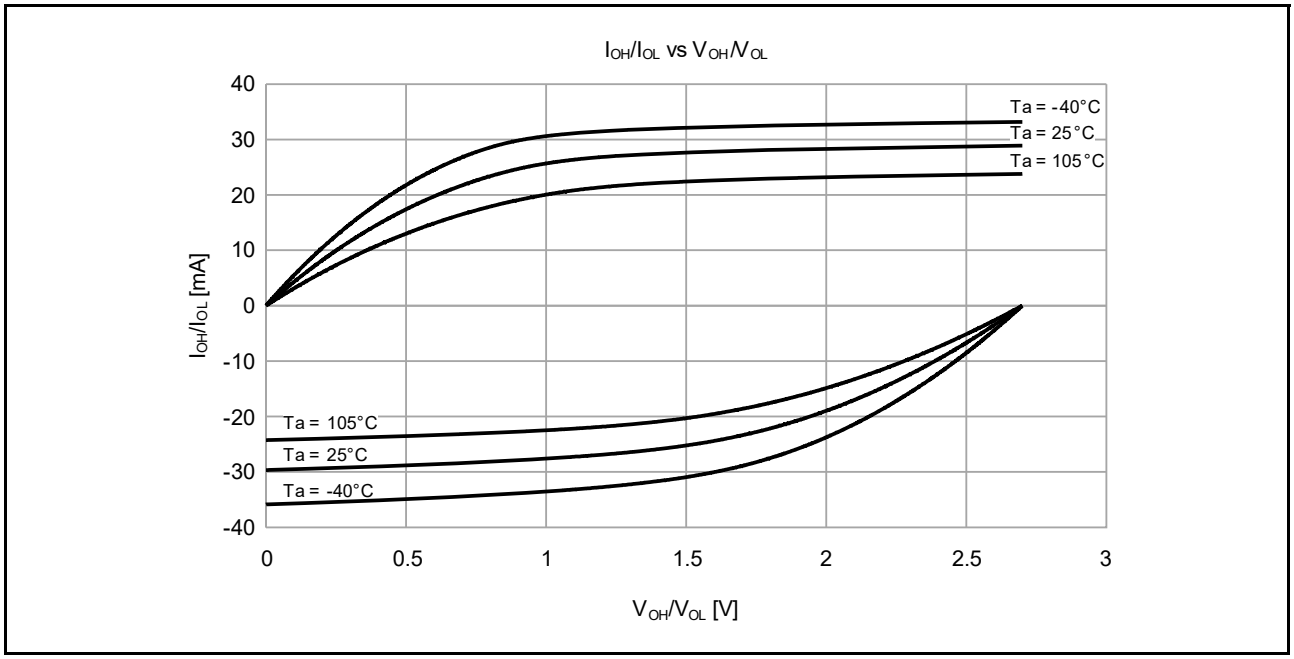
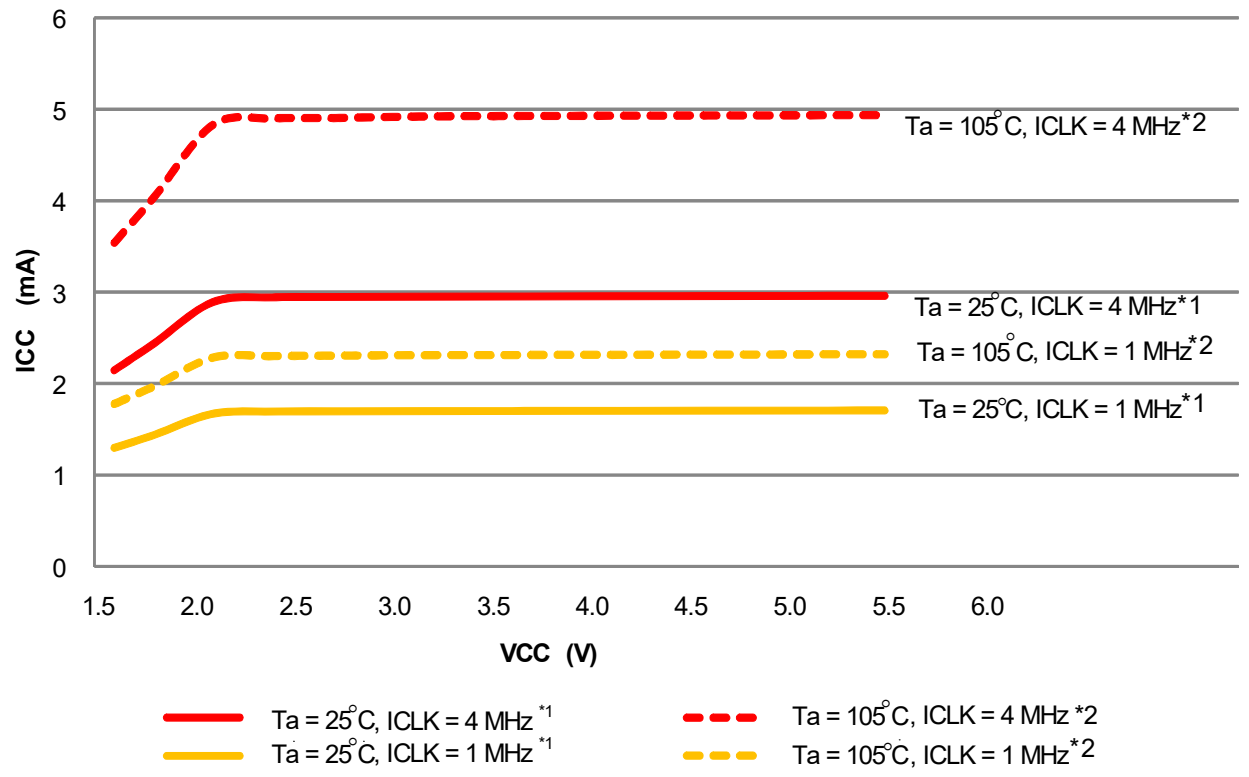


Figure 2.9 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)**



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

Figure 2.20 Voltage dependency in low-voltage mode (reference data)

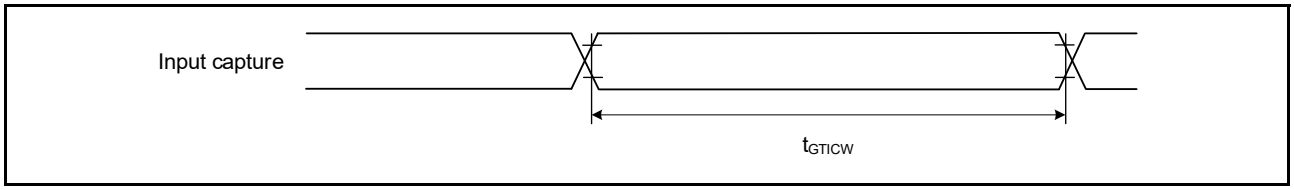


Figure 2.40 GPT input capture timing

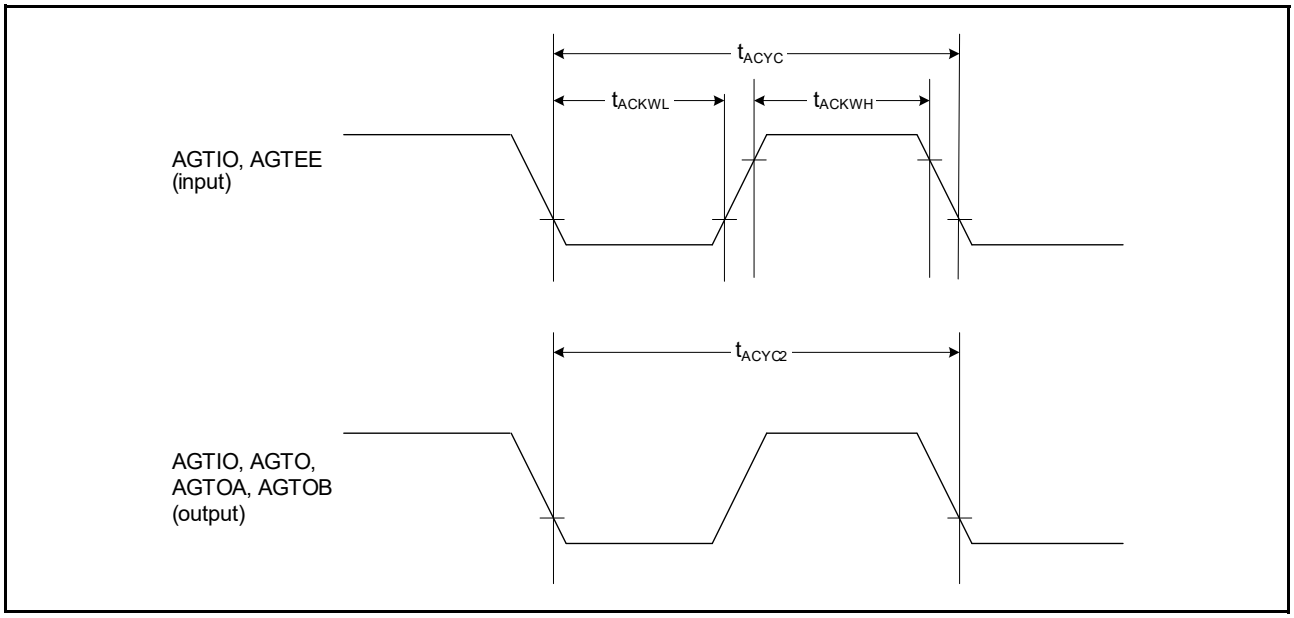


Figure 2.41 AGT I/O timing

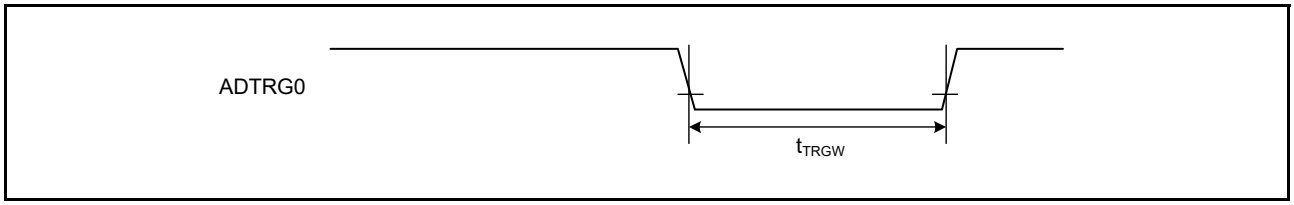


Figure 2.42 ADC14 trigger input timing

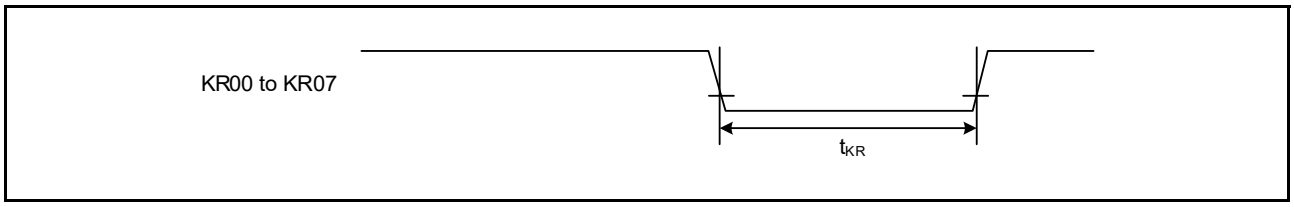
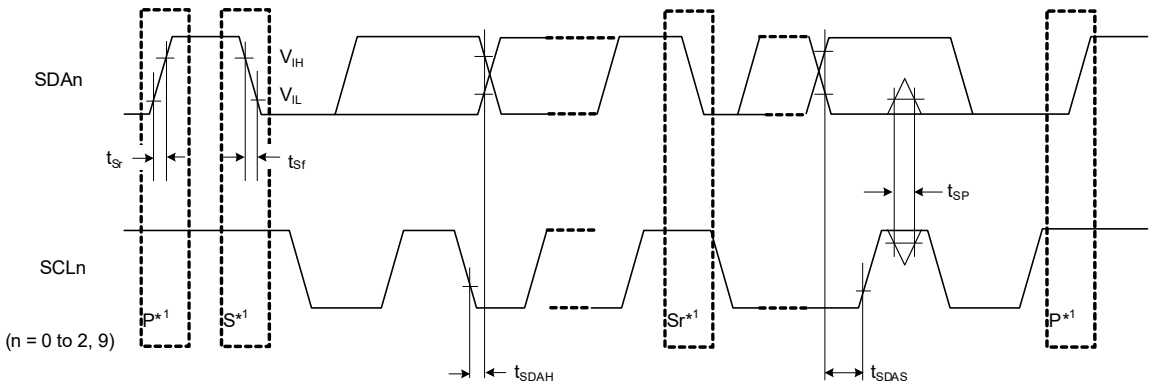


Figure 2.43 Key interrupt input timing

2.3.7 CAC Timing

Table 2.32 CAC timing

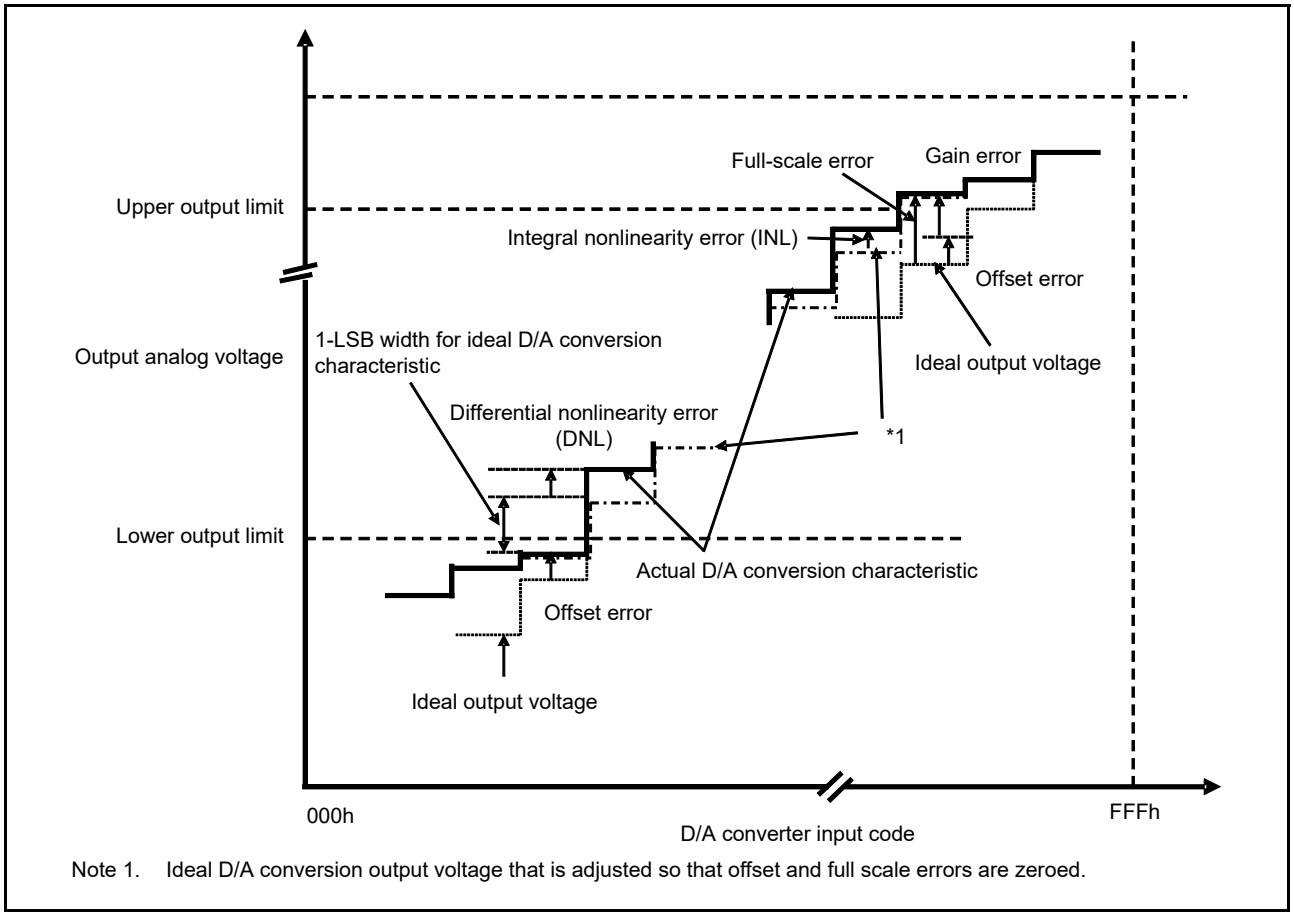
Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{PBcyc}*1 ≤ t_{cac}*2	t_{CACREF}	4.5 × t_{cac} + 3 × t_{PBcyc}*1	-	-	ns	-
		t_{PBcyc}*1 > t_{cac}*2		5 × t_{cac} + 6.5 × t_{PBcyc}*1	-	-	ns	



Note 1. S, P, and Sr indicate the following:
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Figure 2.51 SCI simple IIC mode timing



Note 1. Ideal D/A conversion output voltage that is adjusted so that offset and full scale errors are zeroed.

Figure 2.71 Illustration of D/A converter characteristic terms

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal output voltage based on the ideal conversion characteristic when the measured offset and full-scale errors are zeroed, and the actual output voltage.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB voltage width based on the ideal D/A conversion characteristics and the width of the actual output voltage.

Offset error

Offset error is the difference between the highest actual output voltage that falls below the lower output limit and the ideal output voltage based on the input code.

Full-scale error

Full-scale error is the difference between the lowest actual output voltage that exceeds the upper output limit and the ideal output voltage based on the input code.

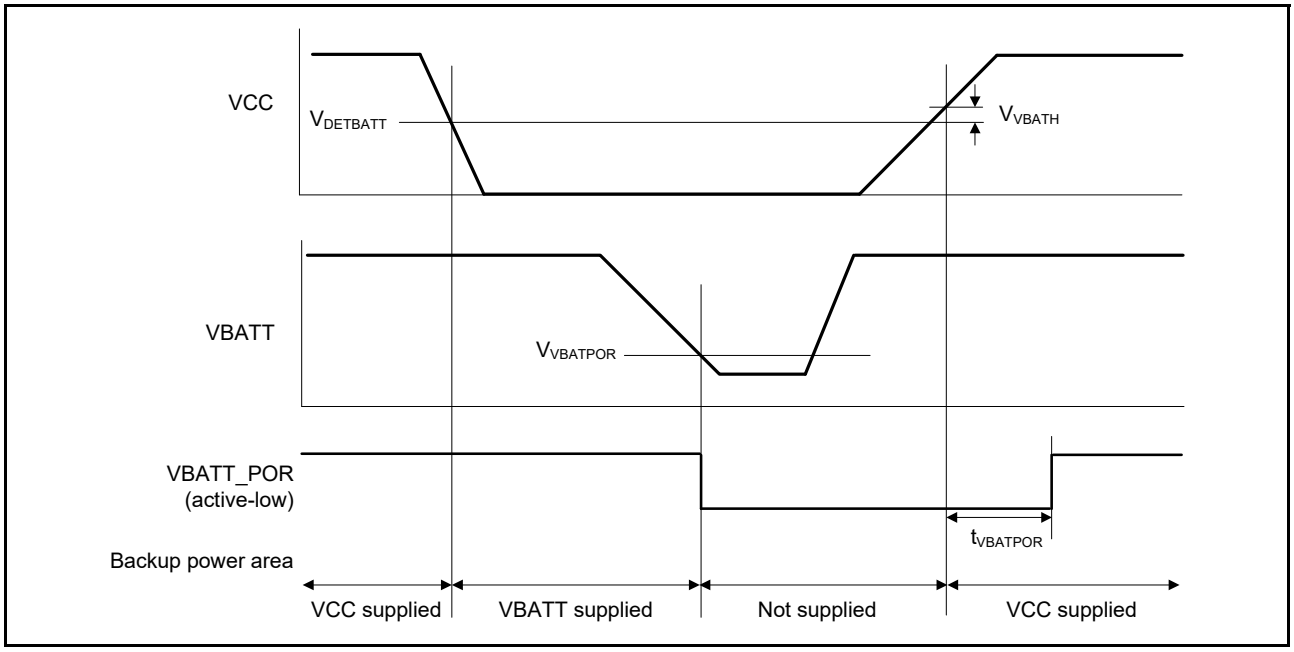


Figure 2.79 VBATT_POR reset timing

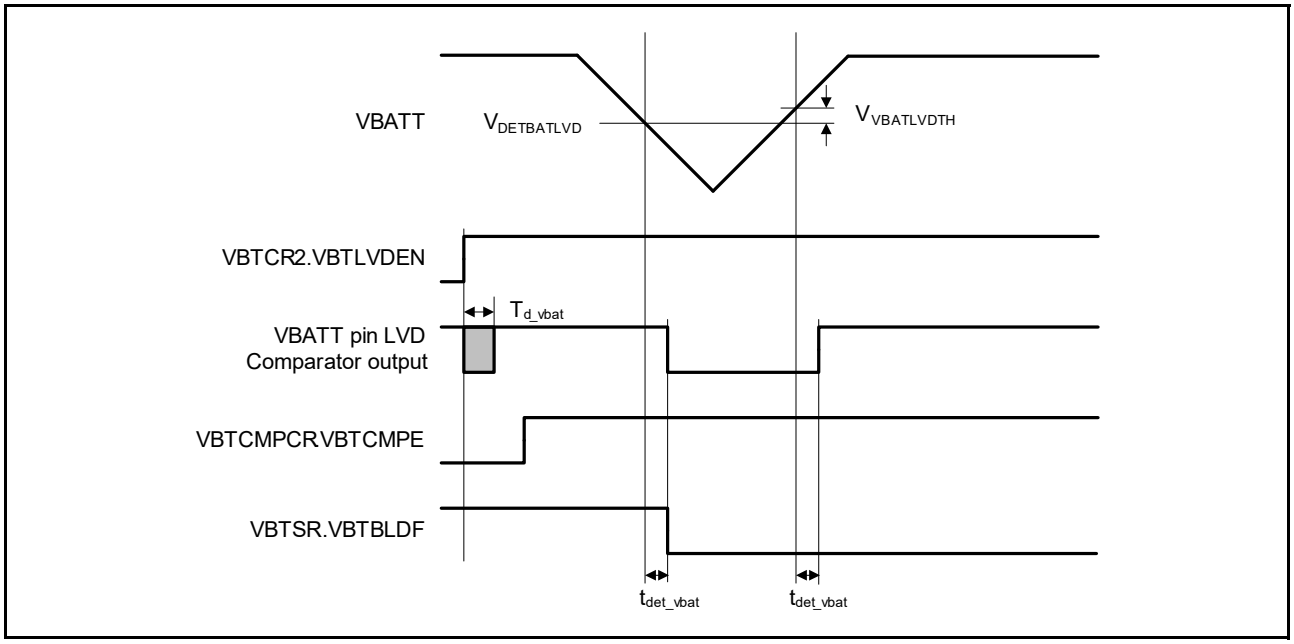


Figure 2.80 VBATT pin voltage detection circuit timing

C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between VL1 and GND
C3: A capacitor connected between VL2 and GND
C4: A capacitor connected between VL4 and GND
C1 = C2 = C3 = C4 = 0.47 µF ±30%.

Note 2. This is the time required to wait from when the reference voltage is specified using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits in the LCDM0 register to 01b) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

[1/4 Bias Method]

Table 2.65 Internal voltage boosting method LCD characteristics

Conditions: VCC = 1.8 V to 5.5 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C5*1 = 0.47 µF	VLCD = 04h	0.90	1.0	1.08	V	-
			VLCD = 05h	0.95	1.05	1.13	V	-
			VLCD = 06h	1.00	1.10	1.18	V	-
			VLCD = 07h	1.05	1.15	1.23	V	-
			VLCD = 08h	1.10	1.20	1.28	V	-
			VLCD = 09h	1.15	1.25	1.33	V	-
			VLCD = 0Ah	1.20	1.30	1.38	V	-
			VLCD = 0Bh	1.25	1.35	1.43	V	-
			VLCD = 0Ch	1.30	1.40	1.48	V	-
Doubler output voltage	V_{L2}	C1 to C5*1 = 0.47 µF		$2V_{L1}$ - 0.08	$2V_{L1}$	$2V_{L1}$	V	-
Tripler output voltage	V_{L3}	C1 to C5*1 = 0.47 µF		$3V_{L1}$ - 0.12	$3V_{L1}$	$3V_{L1}$	V	-
Quadruply output voltage	V_{L4}*4	C1 to C5*1 = 0.47 µF		$4V_{L1}$ - 0.16	$4V_{L1}$	$4V_{L1}$	V	-
Reference voltage setup time*2	t_{VL1S}			5	-	-	ms	Figure 2.81
LCD output voltage variation range*3	t_{VLWT}	C1 to C5*1 = 0.47 µF		500	-	-	ms	

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 µF ± 30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits in the LCDM0 register to 01b) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 4. V_{L4} must be 5.5 V or lower.

2.12.3 Capacitor Split Method

[1/3 Bias Method]

Table 2.66 Internal voltage boosting method LCD characteristics
Conditions: VCC = 2.2 V to 5.5 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
VL4 voltage*1	V_{L4}	C1 to C4 = 0.47 µF*2	-	VCC	-	V	-
VL2 voltage*1	V_{L2}	C1 to C4 = 0.47 µF*2	2/3 × V_{L4} - 0.07	2/3 × V_{L4}	2/3 × V_{L4} + 0.07	V	-
VL1 voltage*1	V_{L1}	C1 to C4 = 0.47 µF*2	1/3 × V_{L4} - 0.08	1/3 × V_{L4}	1/3 × V_{L4} + 0.08	V	-
Capacitor split wait time*1	t_{WAIT}		100	-	-	ms	Figure 2.81

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).
Note 2. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 µF ± 30%.

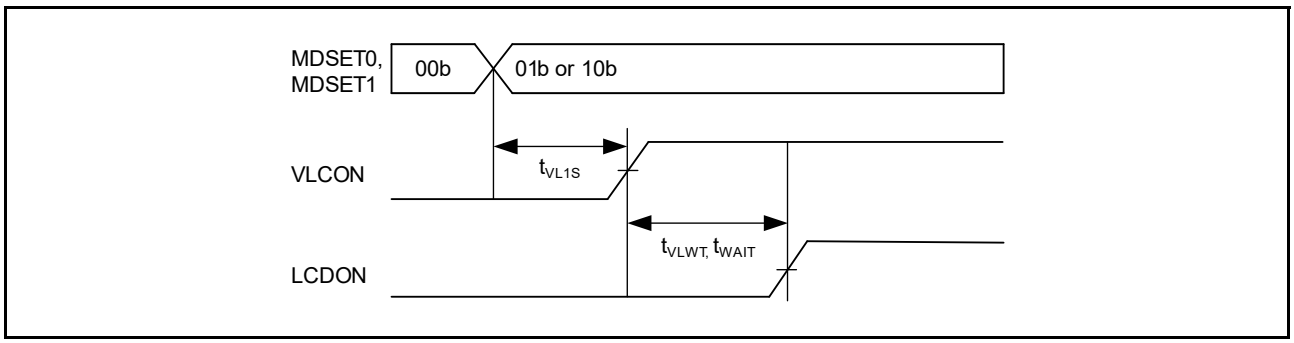


Figure 2.81 LCD reference voltage setup time, voltage boosting wait time, and capacitor split wait time

Table 2.77 JTAG (debug) characteristics (2)
Conditions: VCC = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	250	-	-	ns	Figure 2.85
TCK clock high pulse width	t_{TCKH}	120	-	-	ns	
TCK clock low pulse width	t_{TCKL}	120	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	50	-	-	ns	Figure 2.86
TMS hold time	t_{TMSH}	50	-	-	ns	
TDI setup time	t_{TDIS}	50	-	-	ns	
TDI hold time	t_{TDIH}	50	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	150	ns	

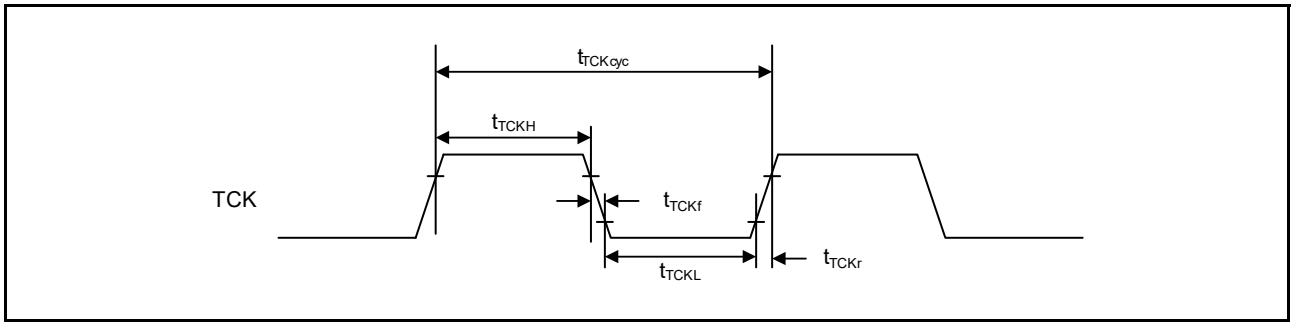


Figure 2.85 JTAG TCK timing

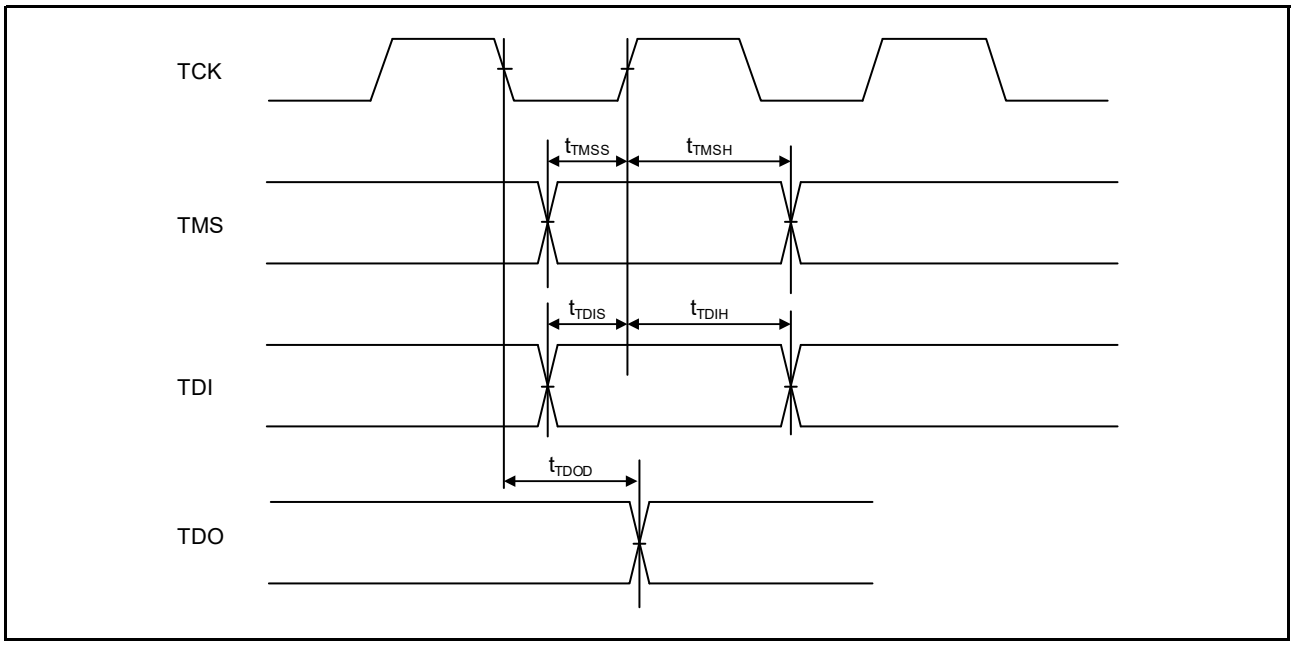
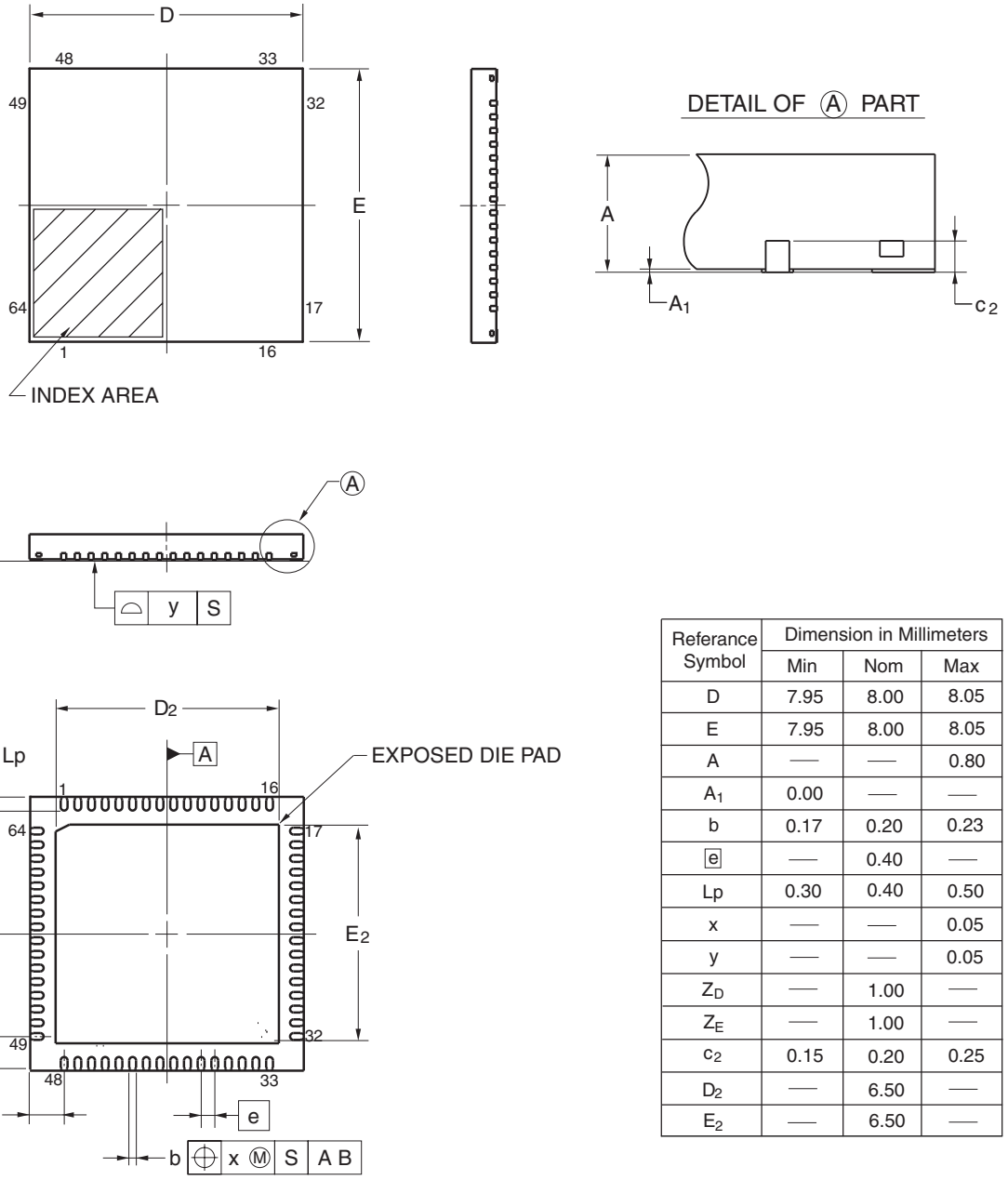


Figure 2.86 JTAG input/output timing

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN64-8x8-0.40	PWQN0064LA-A	P64K8-40-9B5-3	0.16

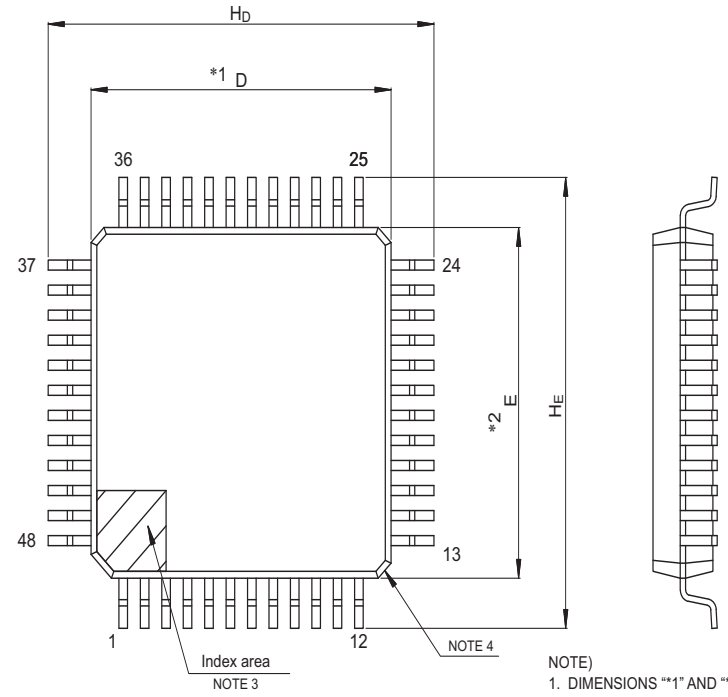


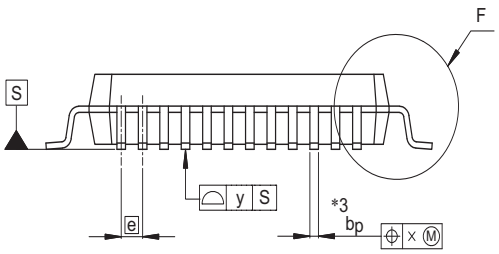
Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	7.95	8.00	8.05
E	7.95	8.00	8.05
A	—	—	0.80
A_1	0.00	—	—
b	0.17	0.20	0.23
e	—	0.40	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	1.00	—
Z_E	—	1.00	—
c_2	0.15	0.20	0.25
D_2	—	6.50	—
E_2	—	6.50	—

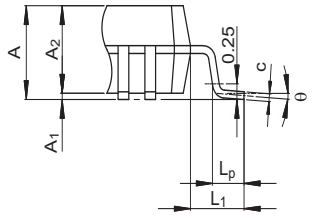
Figure 1.4 64-pin QFN

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.5 48-pin LQFP