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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674ff3mvv3

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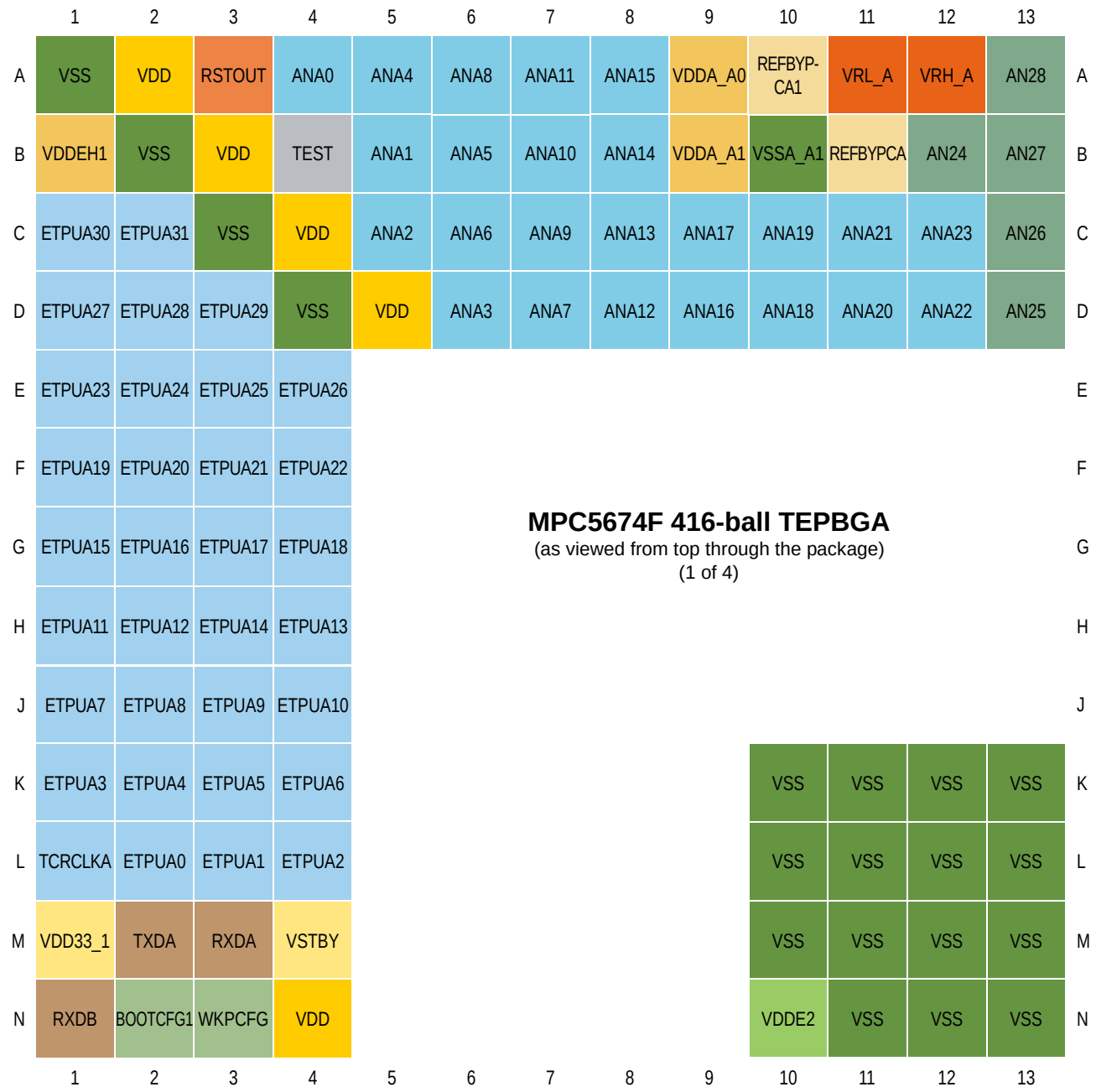
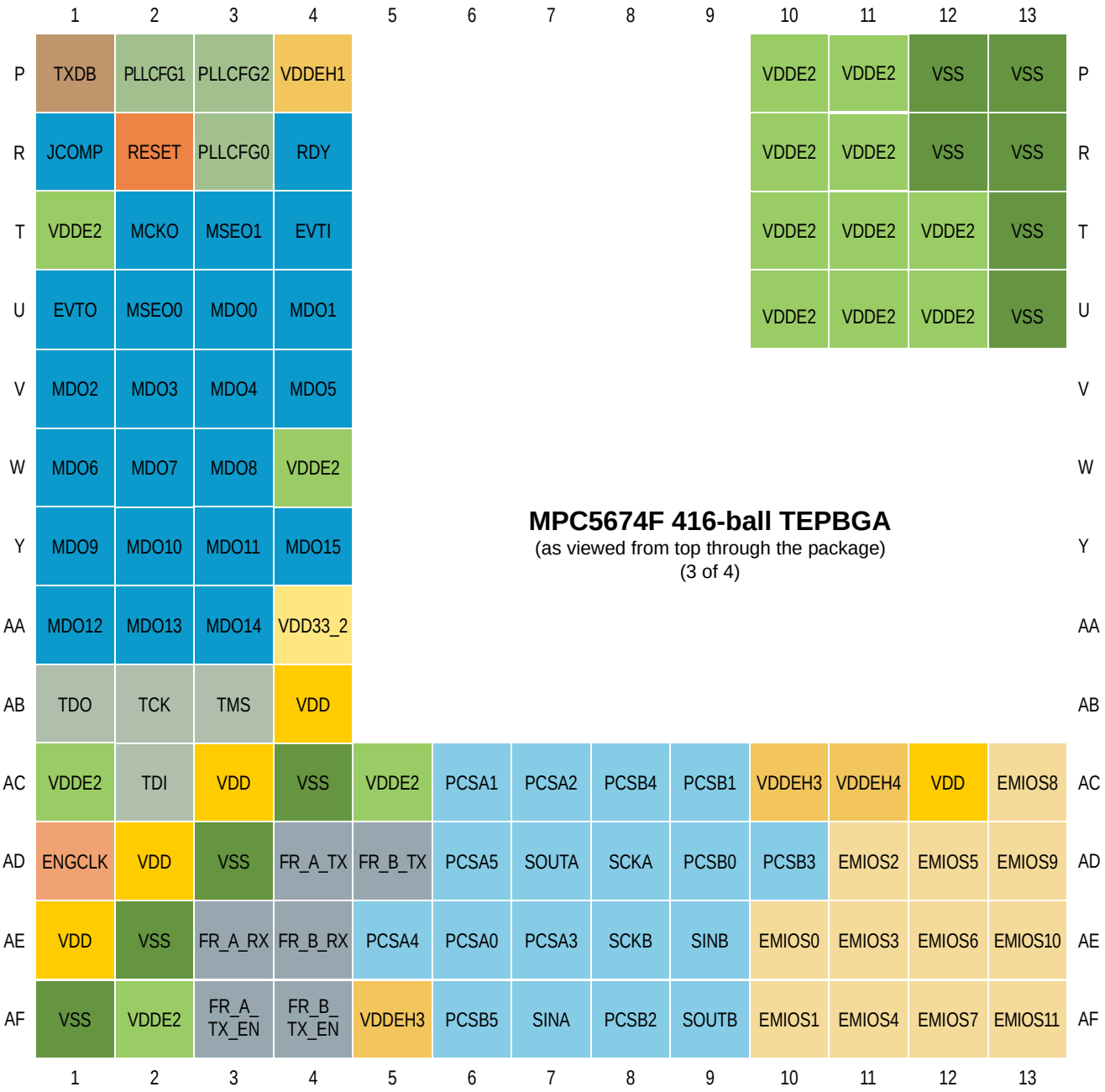


Figure 7. MPC5674F 416-ball TEPBGA (1 of 4)



	1	2	3	4	5	6	7	8	9	10	11	12	13	
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	U
V	MDO2	MDO3	MDO4	MDO5										V
W	MDO6	MDO7	MDO8	VDDE2										W
Y	MDO9	MDO10	MDO11	MDO15										Y
AA	MDO12	MDO13	MDO14	VDD33_2										AA
AB	TDO	TCK	TMS	VDD										AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	AE
AF	VSS	VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 9. MPC5674F 416-ball TEPBGA (3 of 4)

[1] Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

[2] 2.0 V for 10 hours cumulative time, 1.2V +10% for time remaining.

[3] 6.4 V for 10 hours cumulative time, 5.0V +10% for time remaining.

[4] Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

[5] 5.3 V for 10 hours cumulative time, 3.3V +10% for time remaining.

[6] MPC5674F has two analog power supply pins on the pinout: VDDA_A and VDDA_B.

[7] MPC5674F has two analog ground supply pins on the pinout: VSSA_A and VSSA_B.

[8] MPC5674F has two analog low reference voltage pins on the pinout: VRL_A and VRL_B.

[9] MPC5674F has two analog high reference voltage pins on the pinout: VRH_A and VRH_B.

[10] Total injection current for all pins must not exceed 25 mA at maximum operating voltage.

[11] Injection current of ±5 mA allowed for limited duration for analog (ADC) pads and digital 5 V pads. The maximum accumulated time at this current shall be 60 hours. This includes an assumption of a 5.25 V maximum analog or V_{DDEH} supply when under this stress condition.

[12] Total injection current for all analog input pins must not exceed 15 mA.

[13] Lifetime operation at these specification limits is not guaranteed.

[14] Solder profile per CDF-AEC-Q100.

[15] Moisture sensitivity per JEDEC test method A112.

4.2 Thermal Characteristics

Table 4. Thermal Characteristics, 416-pin TEPBGA Package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	24	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	18	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	19	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	14	°C/W
Junction to Board [5]	$R_{\theta JB}$	9	°C/W
Junction to Case [6]	$R_{\theta JC}$	6	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	2	°C/W

[1] Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

[2] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[3] Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

[4] Per JEDEC JESD51-6 with the board horizontal.

[5] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[6] Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

[7] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4 "FM on" = FM depth of ±2%

5 K = 30 dBμV

Table 8. EMC Radiated Emissions Operating Behaviors: 516 BGA

Symbol	Description	Conditions	f_{OSC} f_{SYS}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 516 BGA EBI on CLK on FM off	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	40	dBμV	1
				50–150	48		
				150–500	48		
				500–1000	47		
				IEC and SAE level	G[2]	—	1, 3
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 516 BGA EBI on CLK on FM on[4]	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	40	dBμV	1
				50–150	44		
				150–500	41		
				500–1000	36		
				IEC and SAE level	G[2]	—	1, 3

1 Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

2 G = 48 dBμV

3 Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

4 "FM on" = FM depth of ±2%

4.4 ESD Characteristics

Table 9. ESD Ratings[1,2]

Spec	Characteristic	Symbol	Value	Unit
1	ESD for Human Body Model (HBM)	V_{HBM}	2000	V
2	ESD for Charged Device Model (CDM)	V_{CDM}	750 (corners) 500 (other)	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.5 PMC/POR/LVI Electrical Specifications

Note: For ADC internal resource measurements, see Table 20 in Section 4.9.1, "ADC Internal Resource Measurements."

Table 11. PMC Electrical Specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
12c	—	LVD VDDREG Hysteresis (LDO3V / LDO5V mode)	—	30	—	mV
12d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (LDO3V / LDO5V mode)	—	30	—	mV
13	V_{LVDREG}	Nominal rising LVD VDDREG (SMPS5V mode)	—	4.360	—	V
13a	—	Untrimmed LVD VDDREG variation before band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	V
13b	—	Trimmed LVD VDDREG variation after band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	V
13c	—	LVD VDDREG Hysteresis (SMPS5V mode)	—	50	—	mV
13d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (SMPS5V mode)	—	50	—	mV
14	V_{LVDA}	Nominal rising LVD VDDA	—	4.60	—	V
14a	—	Untrimmed LVD VDDA variation before band gap trim	V_{LVDA} – 5%	V_{LVDA}	V_{LVDA} + 5%	V
14b	—	Trimmed LVD VDDA variation after band gap trim	V_{LVDA} – 3%	V_{LVDA}	V_{LVDA} + 3%	V
14c	—	LVD VDDA Hysteresis	—	150	—	mV
14d	$V_{LVDASTEP}$	Trimming step LVD VDDA	—	20	—	mV
15	—	SMPS regulator output resistance **Note:** Pulup to VDDREG when high, pulldown to VSSREG when low.	—	15	25	Ohm
16	—	SMPS regulator clock frequency (after reset)	1.0	1.5	2.4	MHz
17	—	SMPS regulator overshoot at start-up[2]	—	1.32	1.4	V
18	—	SMPS maximum output current	—	1.0	—	A
19	—	Voltage variation on current step[2] (20% to 80% of maximum current with 4 usec constant time)	—	—	0.1	V

1 VRC linear regulator is capable of sourcing a current up to 20 mA and sinking a current up to 500 μA. When using the recommended ballast transistor the maximum output current provided by the voltage regulator VRC/ballast to the VDD core voltage is up to 1A.

2 Parameter cannot be tested; this value is based on simulation and characterization.

Table 15. V_{DDE}/V_{DDEH} I/O Pad Average DC Current[1] (continued)

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive/Slew Rate Select	Current (mA)
9	Fast w/ Slew Control	I_{DRV_FSR}	66	50	3.6	11	12.7
10			50	50	3.6	10	6.7
11			33.33	50	3.6	01	4.2
12			20	50	3.6	00	2.6
13			20	200	3.6	00	9.1

1 These are average IDDE numbers for worst case PVT from simulation. Currents apply to output pins only.

2 All loads are lumped.

Table 22. ADC Band Gap Reference / LVI Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	1.171	1.220	1.269	V

Table 23. Temperature Sensor Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	Slope –40 °C to 100 °C ±1.0 °C 100 °C to 150 °C ±1.6 °C ADC0 channel 128 ADC1 channel 128	$V_{SADC128}$[1]	—	5.8	—	mV/ °C
2	Accuracy –40 °C to 150 °C ADC0 channel 128 ADC1 channel 128	—	—	±10.0	—	°C

1 Slope is the measured voltage change per °C.

4.10 C90 Flash Memory Electrical Characteristics

Table 24. Flash Program and Erase Specifications

Spec	Characteristic	Symbol	Min	Typ[1]	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	38	—	500	µs
2	Page Program Time[4,5]	$t_{pprogram}$	—	45	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	270	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	800	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	1500	2600	7500	ms
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	3000	5200	15000	ms

1 Typical program and erase times assume nominal supply values and operation at 25 ^{o}C.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

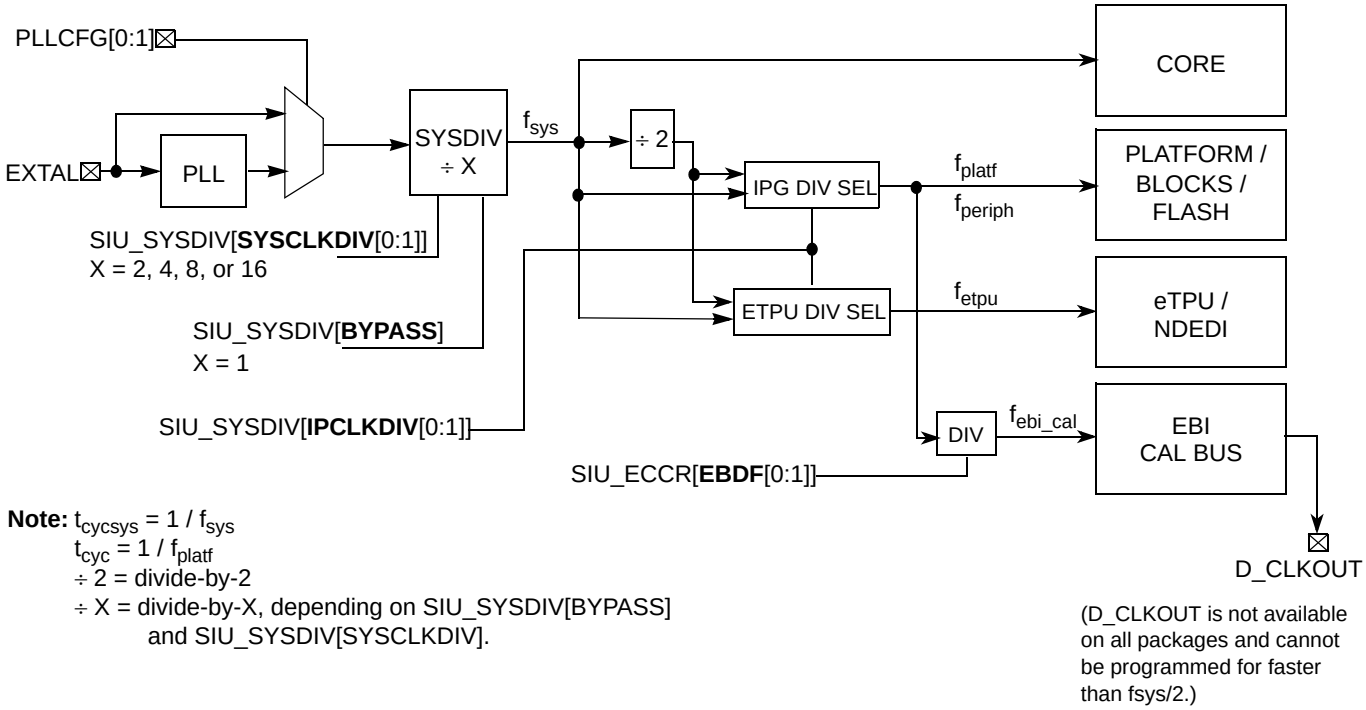
4 Program times are actual hardware programming times and do not include software overhead.

5 Page size is 128 bits (4 words).

4.11 AC Specifications

4.11.1 Clocking

The Figure 16 shows the operating frequency domains of various blocks on MPC5674F.



Note: $t_{cycsys} = 1 / f_{sys}$
$t_{cyc} = 1 / f_{platf}$
÷ 2 = divide-by-2
÷ X = divide-by-X, depending on SIU_SYSDIV[BYPASS] and SIU_SYSDIV[SYSCLKDIV].

Figure 16. MPC5674F Block Operating Frequency Domain Diagram

Table 27 shows the operating frequencies of various blocks depending on the device's clocking mode configuration settings (see Table 28 and Table 29 for descriptions of bit settings).

Table 27. MPC5674F Operating Frequencies[1, 2]

Mode	SIU_ECCR [EBDF[0:1]][3]	f_{sys} (core)	f_{platf} (platform and all blocks except eTPU)	f_{etpu} (eTPU, eTPU RAM, and NDEDI)	f_{ebi_cal}[4,5]	Unit
Enhanced	01 11	264 264	132 132	132 132	66 33	MHz
Full	01 11	200 200	100 100	200 200	50 25	MHz
Legacy	01 11	132 132	132 132	132 132	66 33	MHz

1 The values in the table are specified at:
V_{DD} = 1.02 V to 1.32 V
V_{DDE} = 3.0 V to 3.6 V
V_{DDEH} = 4.5 V to 5.5 V
V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V
$T_A = T_L$ to T_H.

4.12.5 External Bus Interface (EBI) Timing

Table 35. Bus Operation Timing [1]

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq)[2] [3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	
5	D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COH}	1.0/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 1.0 ns EBTS = 1: 1.5 ns
6	D_CLKOUT Posedge to Output Signal Valid (Output Delay) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COV}	—	7.0/7.5	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 7.0 ns EBTS = 1: 7.5 ns

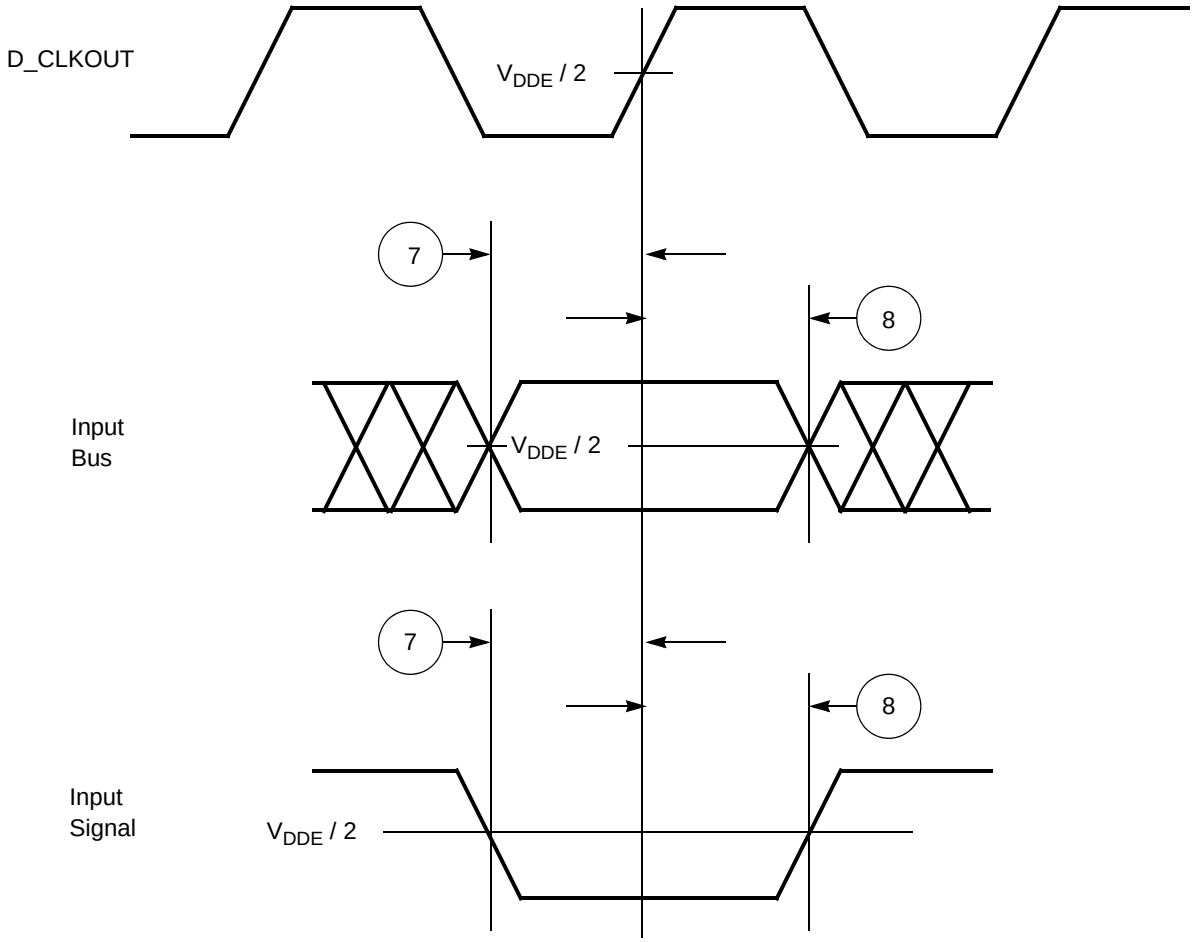


Figure 29. Synchronous Input Timing

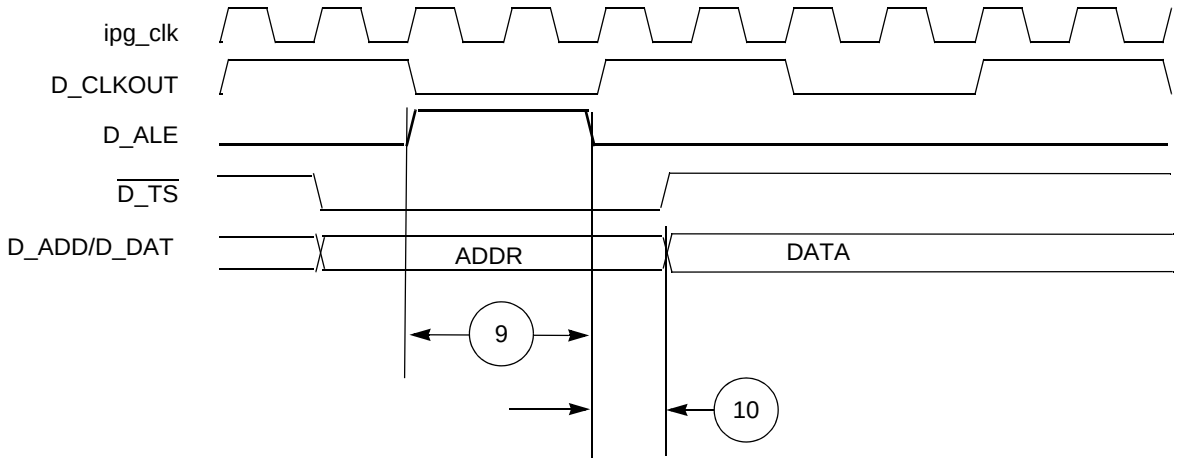


Figure 30. ALE Signal Timing

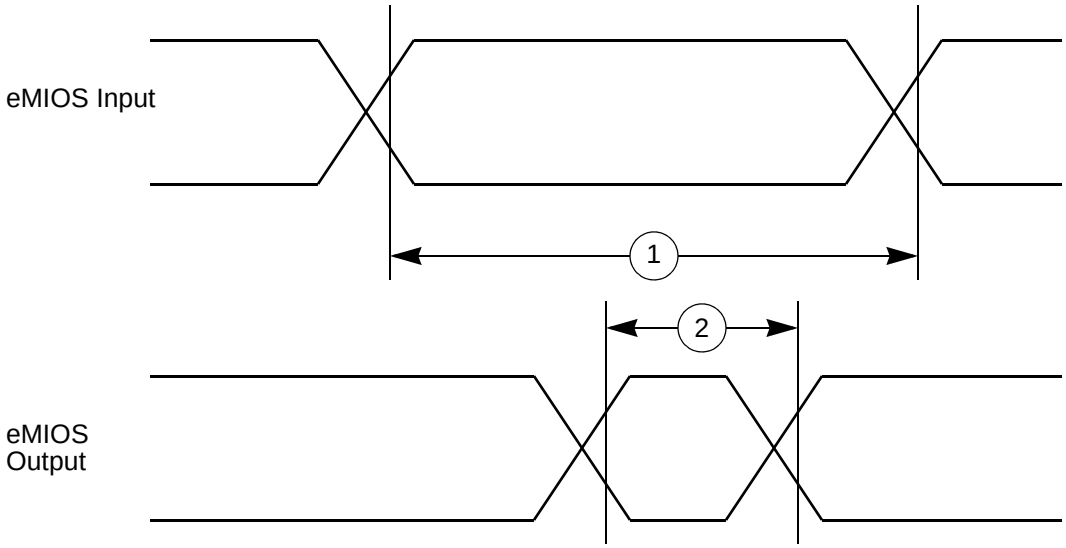


Figure 33. eMIOS Timing

4.12.9 DSPI Timing

Table 39. DSPI Timing[1 2]

Spec	Characteristic	Symbol	Peripheral Bus Freq: 132 MHz		Unit
			Min	Max	
1	DSPI Cycle Time[3, 4] Master (MTFE = 0) Slave (MTFE = 0) Master (MTFE = 1) Slave (MTFE = 1)	t_{SCK}	t_{SYS} * 2	t_{SYS}*32768*7	ns
2	PCS to SCK Delay[5]	t_{CSC}	12	—	ns
3	After SCK Delay[6] Master mode Slave mode	t_{ASC}	t_{SYS} * 2 t_{SYS} *3 – constraints [7]	—	ns
4	SCK Duty Cycle	t_{SDC}	0.33 * t_{SCK}	0.66 * t_{SCK}	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCS*x* to $\overline{PCSS}$ time	t_{PCSC}	t_{SYS} * 2	t_{SYS} * 7	ns
8	$\overline{PCSS}$ to PCS*x* time	t_{PASC}	t_{SYS} * 2	t_{SYS} * 7	ns

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
458	ETPUC17_FR_A_RX_ GPIO458[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G22	H25	H23
		A1	FR_A_RX	FlexRay A receive	I							
		A2	—	—	—							
		G	GPIO458	GPIO	I/O							
459	ETPUC18_FR_A_TX_EN_ GPIO459[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G20	H26	H24
		A1	FR_A_TX_EN	FlexRay A transfer enable	O							
		A2	—	—	—							
		G	GPIO459	GPIO	I/O							
460	ETPUC19_TXDA_ GPIO460[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G21	J23	H21
		A1	TXDA	eSCI A transmit	O							
		A2	—	—	—							
		G	GPIO460	GPIO	I/O							
461	ETPUC20_RXDA _ GPIO461[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G19	J24	H25
		A1	RXDA	eSCI A receive	I							
		A2	—	—	—							
		G	GPIO461	GPIO	I/O							
462	ETPUC21_TXDB_ GPIO462[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H22	J25	H26
		A1	TXDB	eSCI B transmit	O							
		A2	—	—	—							
		G	GPIO462	GPIO	I/O							
463	ETPUC22_RXDB_ GPIO463[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H21	J26	J22
		A1	RXDB	eSCI B receive	I							
		A2	—	—	—							
		G	GPIO463	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
470	ETPUC29_SCKD_ GPIO470[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K21	L25	K23
		A1	SCKD	DSPI D clock	I/O							
		A2	—	—	—							
		G	GPIO470	GPIO	I/O							
471	ETPUC30_SOUTD_ GPIO471[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K20	L26	K24
		A1	SOUTD	DSPI D data output	O							
		A2	—	—	—							
		G	GPIO471	GPIO	I/O							
472	ETPUC31_SIND_ GPIO472[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K19	M23	K25
		A1	SIND	DSPI D data input	I							
		A2	—	—	—							
		G	GPIO472	GPIO	I/O							
eMIOS												
179	EMIOS0_ETPUA0_ GPIO179	P	EMIOS0	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA9	AE10	AC13
		A1	ETPUA0	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO179	GPIO	I/O							
180	EMIOS1_ETPUA1_ GPIO180	P	EMIOS1	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB9	AF10	AB13
		A1	ETPUA1	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO180	GPIO	I/O							
181	EMIOS2_ETPUA2_ GPIO181	P	EMIOS2	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y10	AD11	AD13
		A1	ETPUA2	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO181	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
188	EMIOS9_ETPUA9_ GPIO188	P	EMIOS9	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W11	AD13	AF15
		A1	ETPUA9	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO188	GPIO	I/O							
189	EMIOS10_SCKD_ GPIO189	P	EMIOS10	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA11	AE13	AE15
		A1	SCKD	DSPI D clock	O							
		A2	—	—	—							
		G	GPIO189	GPIO	I/O							
190	EMIOS11_SIND_ GPIO190	P	EMIOS11	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB12	AF13	AB14
		A1	SIND	DSPI D data input	I							
		A2	—	—	—							
		G	GPIO190	GPIO	I/O							
191	EMIOS12_SOUTC_ GPIO191	P	EMIOS12	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB13	AF14	AD15
		A1	SOUTC	DSPI C data output	O							
		A2	—	—	—							
		G	GPIO191	GPIO	I/O							
192	EMIOS13_SOUTD_ GPIO192	P	EMIOS13	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA12	AE14	AC15
		A1	SOUTD	DSPI D data output	O							
		A2	—	—	—							
		G	GPIO192	GPIO	I/O							
193	EMIOS14_IRQ0_ GPIO193	P	EMIOS14	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y12	AC14	AF17
		A1	IRQ0	External interrupt request	I							
		A2	CNTXD	FlexCAN D transmit	O							
		G	GPIO193	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	ANA3	P	ANA3[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA3	ANA3	B6	D6	D6
—	ANA4	P	ANA4[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA4	ANA4	A6	A5	A5
—	ANA5	P	ANA5[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA5	ANA5	A7	B6	B6
—	ANA6	P	ANA6[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA6	ANA6	B7	C6	C6
—	ANA7	P	ANA7[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA7	ANA7	B8	D7	C7
—	ANA8	P	ANA8	eQADC A analog input	I	AE	V_{DDA_A1}	ANA8	ANA8	C5	A6	D7
—	ANA9	P	ANA9	eQADC A analog input	I	AE	V_{DDA_A1}	ANA9	ANA9	C7	C7	A6
—	ANA10	P	ANA10	eQADC A analog input	I	AE	V_{DDA_A1}	ANA10	ANA10	C6	B7	B7
—	ANA11	P	ANA11	eQADC A analog input	I	AE	V_{DDA_A1}	ANA11	ANA11	D6	A7	A7
—	ANA12	P	ANA12	eQADC A analog input	I	AE	V_{DDA_A1}	ANA12	ANA12	D7	D8	D8
—	ANA13	P	ANA13	eQADC A analog input	I	AE	V_{DDA_A1}	ANA13	ANA13	C8	C8	C8
—	ANA14	P	ANA14	eQADC A analog input	I	AE	V_{DDA_A1}	ANA14	ANA14	D8	B8	B8
—	ANA15	P	ANA15	eQADC A analog input	I	AE	V_{DDA_A1}	ANA15	ANA15	A8	A8	A8
—	ANA16	P	ANA16	eQADC A analog input	I	AE	V_{DDA_A1}	ANA16	ANA16	D9	D9	D9
—	ANA17	P	ANA17	eQADC A analog input	I	AE	V_{DDA_A1}	ANA17	ANA17	C9	C9	C9
—	ANA18	P	ANA18	eQADC A analog input	I	AE	V_{DDA_A1}	ANA18	ANA18	D10	D10	D10
—	ANA19	P	ANA19	eQADC A analog input	I	AE	V_{DDA_A1}	ANA19	ANA19	C10	C10	C10
—	ANA20	P	ANA20	eQADC A analog input	I	AE	V_{DDA_A1}	ANA20	ANA20	D11	D11	D11
—	ANA21	P	ANA21	eQADC A analog input	I	AE	V_{DDA_A1}	ANA21	ANA21	C11	C11	C11
—	ANA22	P	ANA22	eQADC A analog input	I	AE	V_{DDA_A1}	ANA22	ANA22	D12	D12	C12
—	ANA23	P	ANA23	eQADC A analog input	I	AE	V_{DDA_A1}	ANA23	ANA23	C12	C12	D12
—	AN24	P	AN24	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN24	AN24	—	B12	B12
—	AN25	P	AN25	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN25	AN25	—	D13	C13
—	AN26	P	AN26	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN26	AN26	—	C13	D13

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	ANB9	P	ANB9	eQADC B analog input	I	AE	V_{DDA_B0}	ANB9	ANB9	C14	D20	A21
—	ANB10	P	ANB10	eQADC B analog input	I	AE	V_{DDA_B0}	ANB10	ANB10	C13	B21	B21
—	ANB11	P	ANB11	eQADC B analog input	I	AE	V_{DDA_B0}	ANB11	ANB11	C15	A21	C21
—	ANB12	P	ANB12	eQADC B analog input	I	AE	V_{DDA_B0}	ANB12	ANB12	C16	C21	A22
—	ANB13	P	ANB13	eQADC B analog input	I	AE	V_{DDA_B0}	ANB13	ANB13	D14	D21	B22
—	ANB14	P	ANB14	eQADC B analog input	I	AE	V_{DDA_B0}	ANB14	ANB14	C17	A22	D20
—	ANB15	P	ANB15	eQADC B analog input	I	AE	V_{DDA_B0}	ANB15	ANB15	D15	B22	C22
—	ANB16	P	ANB16	eQADC B analog input	I	AE	V_{DDA_B0}	ANB16	ANB16	C18	C22	D21
—	ANB17	P	ANB17	eQADC B analog input	I	AE	V_{DDA_B0}	ANB17	ANB17	D16	A23	D22
—	ANB18	P	ANB18	eQADC B analog input	I	AE	V_{DDA_B0}	ANB18	ANB18	D17	B23	A23
—	ANB19	P	ANB19	eQADC B analog input	I	AE	V_{DDA_B0}	ANB19	ANB19	B19	C23	B23
—	ANB20	P	ANB20	eQADC B analog input	I	AE	V_{DDA_B0}	ANB20	ANB20	C19	D22	C23
—	ANB21	P	ANB21	eQADC B analog input	I	AE	V_{DDA_B0}	ANB21	ANB21	D18	A24	A24
—	ANB22	P	ANB22	eQADC B analog input	I	AE	V_{DDA_B0}	ANB22	ANB22	A21	B24	B24
—	ANB23	P	ANB23	eQADC B analog input	I	AE	V_{DDA_B0}	ANB23	ANB23	B20	A25	E20
—	VRH_A	P	VRH_A	ADC A Voltage reference high	I	VDDINT	V_{RH_A}	VRH_A	VRH_A	A10	A12	A12
—	VRL_A	P	VRL_A	ADC A Voltage reference low	I	VSSINT	V_{RL_A}	VRL_A	VRL_A	A11	A11	A11
—	VRH_B	P	VRH_B	ADC B Voltage reference high	I	VDDINT	V_{RH_B}	VRH_B	VRH_B	A16	A19	A19
—	VRL_B	P	VRL_B	ADC B Voltage reference low	I	VSSINT	V_{RL_B}	VRL_B	VRL_B	A15	A18	A18
—	REFBYPCB	P	REFBYPCB	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB	REFBYPCB	B12	B18	B18
—	REFBYPCA	P	REFBYPCA	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA	REFBYPCA	B11	B11	B11
—	VDDA_A0	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A0}	VDDA_A0	VDDA_A0	A9	A9	A9
—	VDDA_A1	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A1}	VDDA_A1	VDDA_A1	B9	B9	B9
—	REFBYPCA1	P	REFBYPCA1	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA1	REFBYPCA1	A12	A10	A10
—	VSSA_A1	P	VSSA_A	Ground	I	VSSE	V_{SSA_A1}	VSSA_A1	VSSA_A1	B10	B10	B10
—	VDDA_B0	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B0}	VDDA_B0	VDDA_B0	A13	A16	A16
—	VDDA_B1	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B1}	VDDA_B1	VDDA_B1	B13	B16	B16

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
288	D_ADD_DAT10_ GPIO288	P	D_ADD_DAT10	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO288	GPIO	I/O							
289	D_ADD_DAT11_ GPIO289	P	D_ADD_DAT11	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO289	GPIO	I/O							
290	D_ADD_DAT12_ GPIO290	P	D_ADD_DAT12	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO290	GPIO	I/O							
291	D_ADD_DAT13 _GPIO291	P	D_ADD_DAT13	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO291	GPIO	I/O							
292	D_ADD_DAT14_GPIO292	P	D_ADD_DAT14	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	L22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO292	GPIO	I/O							

Table 43 lists the pin locations of the power and ground signals on the 324 TEPBGA package.

Table 43. 324-pin Power Supply Locations

VDD

A2	B3	C4	D5	K3	V19	W5	W9	W20	Y4	Y21	AA3	AA22	AB2

VDD33

W21	V4

VDDE2

AB4	M9	N1	N10	N9	P10	P9	T4	W6	V2

VDDEH1

B1	L4

VDDEH4

AB20	W8

VDDEH6

N20	T21

VDDEH7

C22	H19	L22

VSS

A1	A22	AA2	AA21	AB1	AB22	B2	B21	C20	C3	D19	D4	J10	J11	J12	J13	J14	J9
K10	K11	K12	K13	K14	K9	L10	L11	L12	L13	L14	L9	M10	M11	M12	M13	M14	N11
N12	N13	N14	P11	P12	P13	P14	W19	W4	Y20	Y3							

Table 46. Revision History (continued)

Revision (Date)	Description of changes
9 (Oct-2012)	Updated Table 1 (Orderable Part Numbers) with actual available parts.Added new part number SPC5673FF3MVY2 ,Package description 516 PBGA, w/EBI, Pb-free.Speed is 200Mhz nom and max. —Removed note attached to “Orderable Part Numbers” and “Freescale Part Number”. Updated footnotes of Table 3 (Absolute Maximum Ratings) to: • 2.0 V for 10 hours cumulative time, 1.2V +10% for time remaining. • 6.4 V for 10 hours cumulative time, 5.0V +10% for time remaining. • 5.3 V for 10 hours cumulative time, 3.3V +10% for time remaining. Updated Table 6 (Thermal Characteristics, 324-pin Package) to show MPC5674F thermal characteristics. In Table 10 (PMC Operating conditions) updated the parameter “Supply voltage VDD 1.2V nominal" to “Core supply voltage". In Table 11 (PMC Electrical Specifications) updated the following rows: —Parameter “Nominal VRC regulated 1.2V output VDD” updated column “Typ” to 1.27 V. —The minimum and maximum value of “Untrimmed VRC 1.2V output variation before band gap trim (unloaded)” updated to “-14%” and “+10%” respectively. —The minimum and maximum value of “Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max 1A)” updated to “-10%” and “+5%” respectively. In Table 12 (Power Sequence Pin States for MH and AE pads) updated the row(VDD33 = low, VDDE = high), parameter “MH+LVDS Pads” to “Outputs disabled”. In Table 13 (Power Sequence Pin States for F and FS pads) updated the rows (VDD = low, VDD33 = low, VDDE = high) and (VDD = high, VDD33 = low, VDDE = high) ,parameter “F and FS pad” to “Outputs disabled”. In Table 14 (DC Electrical Specifications) updated the spec 24 “Operating Current 1.2 V Supplies @ f_{SYS} = 264 MHz” with 'V_{DD} @ 1.32 V' Max value to 850 mA from 1.0 A, and deleted corresponding footnote stating that the previous information was preliminary. Updated current(mA) values in Table 15 (V_{DDE}/V_{DDEH} I/O Pad Average DC Current) from Spec 5 to 13. -Spec 5 Current (mA) from 6.5 to 7.4 -Spec 6 Current (mA) from 9.4 to 10.5 -Spec 7 Current (mA) from 10.8 to 12.3 -Spec 8 Current (mA) from 33.3 to 35.2 -Spec 9 Current (mA) from 12.0 to 12.7 -Spec 10 Current (mA) from 6.2 to 6.7 -Spec 11 Current (mA) from 4.0 to 4.2 -Spec 12 Current (mA) from 2.4 to 2.6 -Spec 13 Current (mA) from8.9 to 9.1 In Table 34 (Nexus Debug Port Timing) updated the footnote of parameter “t_{CYC}” to “See Notes on tcyc in Table 27 “.Removed references to “Section I/O Pad VDD33 Current Specifications” .