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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674ff3mvy3

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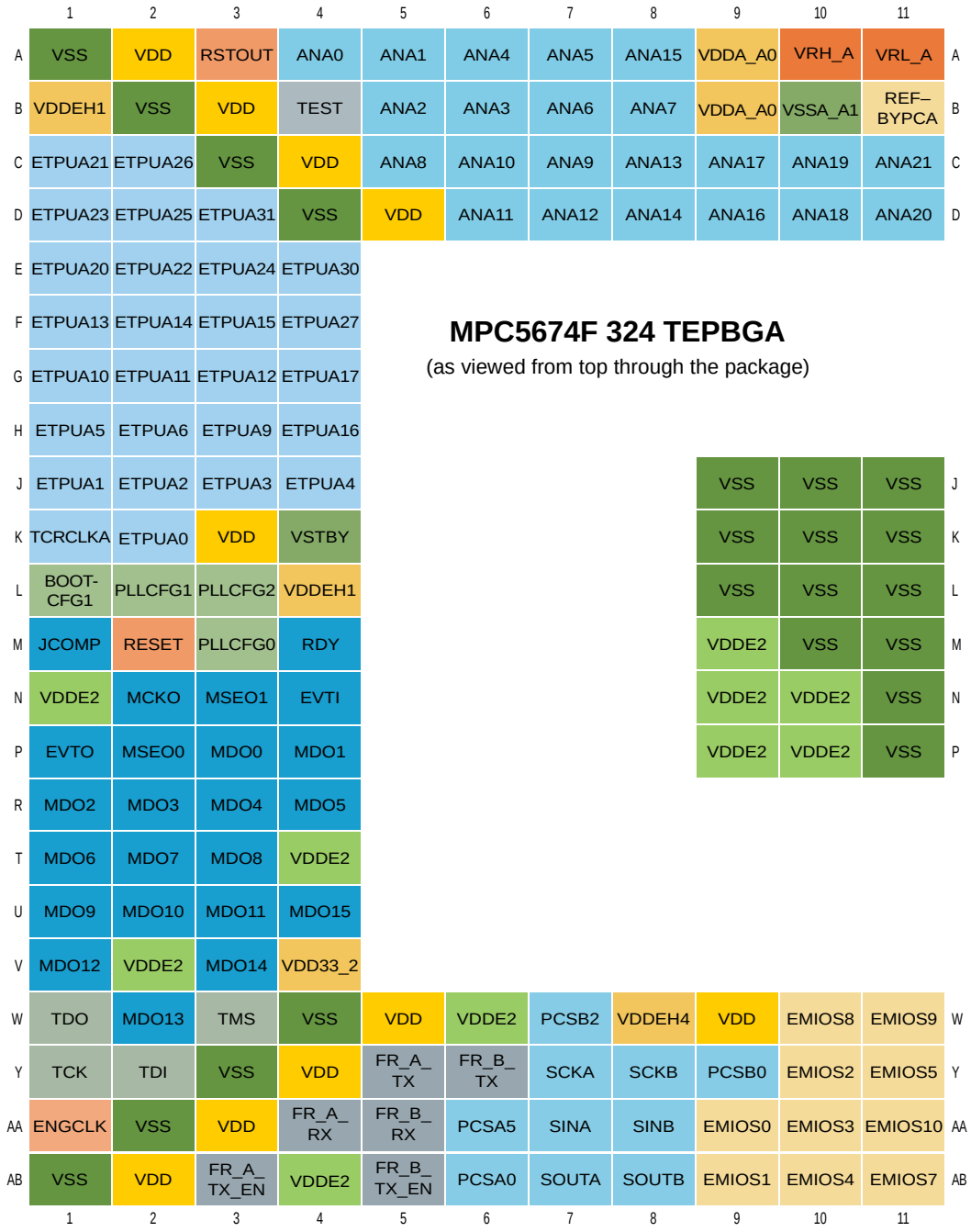

Figure 4. MPC5674F 324-ball TEPBGA (1 of 2)

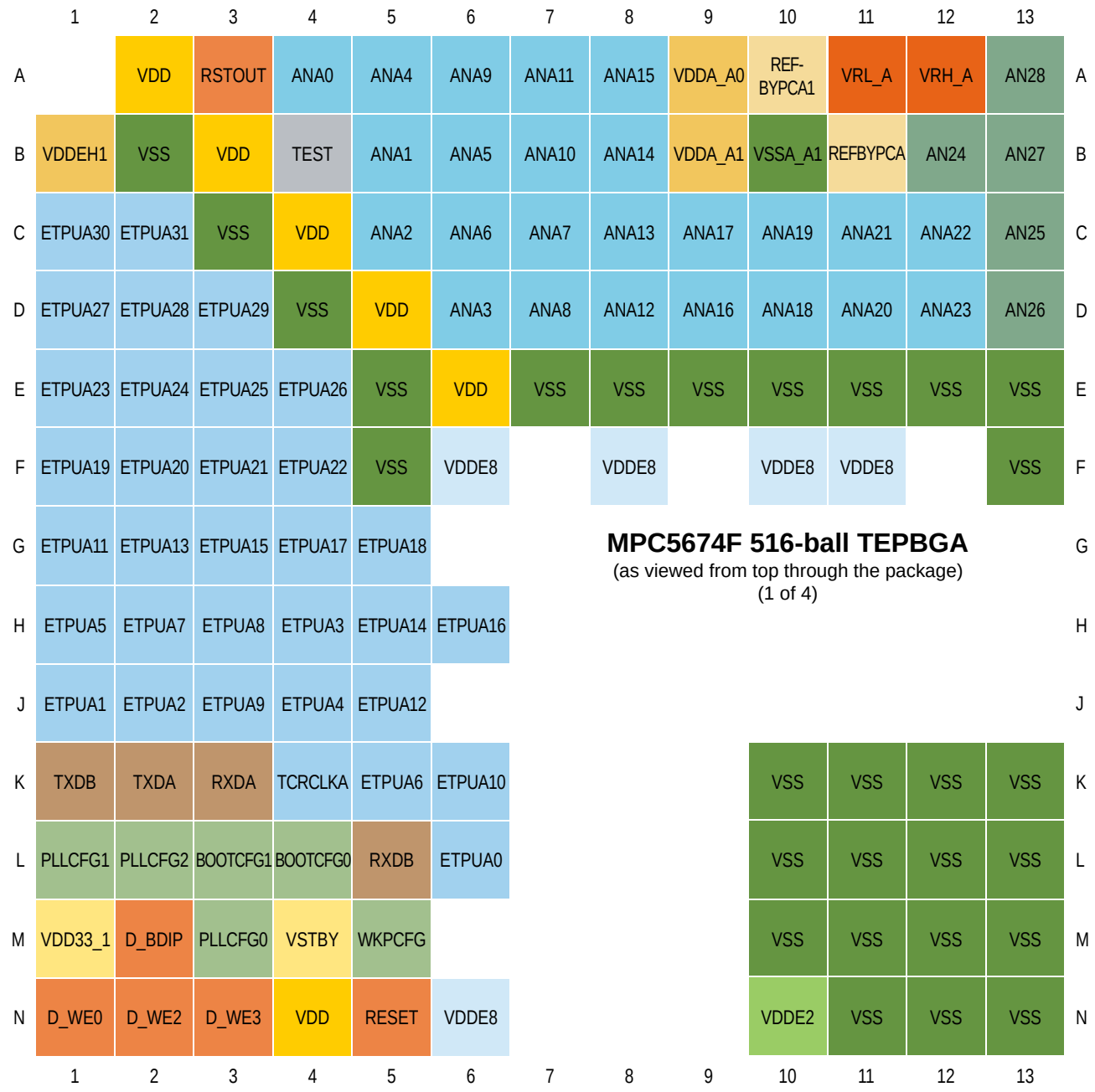

Figure 12. MPC5674F 516-ball TEPBGA (1 of 4)

Table 25. Flash EEPROM Module Life

Spec	Characteristic	Symbol	Min	Typical[1]	Unit
1	Number of program/erase cycles per block for 16 KB and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
2	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range (T_J)	P/E	1,000	100,000	cycles
3	Minimum Data Retention at 85 °C ambient temperature[2] Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	Retention	 20 10 5	 — — —	years

1 Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

2 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

Table 26 shows the Platform Flash Configuration Register 1 (PFCPR1) settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

Table 26. PFCPR1 Settings vs. Frequency of Operation[1]

Spec	Clock Mode	Maximum Frequency[2] (MHz)		APC = RWSC	WWSC	DPFEN[3]	IPFEN[3]	PFLIM[4]	BFEN[5]
		Core f_{sys}	Platform f_{platf}						
1	Enhanced	264 MHz[6]	132 MHz[6]	0b011	0b01	0b0 0b1	0b0 0b1	0b00 0b01 0b1x	0b0 0b1
2	Enhanced/ Full	200 MHz	100 MHz	0b010	0b01	0b0 0b1	0b0 0b1	0b00 0b01 0b1x	0b0 0b1
3	Legacy	132 MHz	132 MHz	0b100	0b01	0b0 0b1	0b0 0b1	0b00 0b01 0b1x	0b0 0b1
Default setting after reset:				0b111	0b11	0b00	0b00	0b00	0b0

1 Illegal combinations exist. Use entries from the same row in this table.

2 This is the nominal maximum frequency of operation: platform runs at $f_{sys}/2$ in Enhanced Mode .

3 For maximum flash performance, set to 0b1.

4 For maximum flash performance, set to 0b10.

5 For maximum flash performance, set to 0b1.

6 This is the nominal maximum frequency of operation in Enchanced Mode. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system core clock(f_{sys}) + 2% FM and 132 Mhz platform clock (f_{platf})+ 2% FM.

2 Up to the maximum frequency rating of the device (refer to Table 1). The f_{sys} speed is the nominal maximum frequency. 270 Mhz parts allow for 264 Mhz system clock + 2% FM.

3 See the *MPC5674F Reference Manual* for full description as not all bit combinations are valid.

4 EBI/Calibration bus is not available in all packages.

5 The EBI/Calibration Bus operating frequency, f_{ebi_cal} , depends on clock divider settings of block's max allowed frequency of operation. Normally $f_{ebi\_cal} = f_{platf}$ /2, but can be limited to < f_{platf} /2 in Full Mode.

Table 28. IPCLKDIV Settings

SIU_SYSDIV [IPCLKDIV[0:1]]	Mode	Description
00	Enhanced	CPU frequency is doubled (Max 264Mhz). Platform, peripheral, and eTPU clocks are 1/2 of CPU frequency
01	Full	CPU and eTPU frequency is doubled (Max 200Mhz). Platform and peripheral clocks are 1/2 of CPU frequency.
10	—	Reserved
11	Legacy	CPU, eTPU, platform, and peripheral's clocks all run at same speed (Max 132Mhz).

Table 29. SYSCLKDIV Settings

SIU_SYSDIV [SYSCLKDIV[0:1]]	Description
00	Divide by 2.
01	Divide by 4.
10	Divide by 8.
11	Divide by 16.

[2] See Notes on t_{cyc} on Figure 16 and Table 27 in Section 4.11.1, “Clocking.”

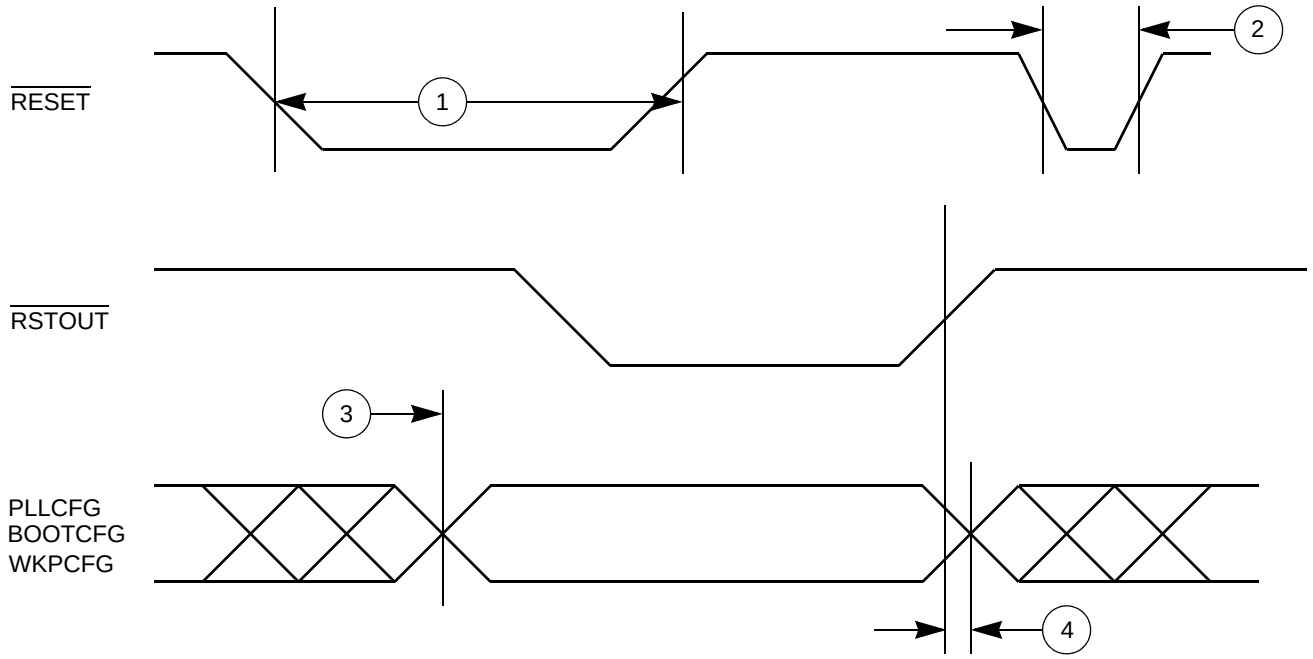

Figure 20. Reset and Configuration Pin Timing

4.12.3 IEEE 1149.1 Interface Timing

Table 33. JTAG Pin AC Electrical Characteristics[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at V_{DDE} / 2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40%–70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	10	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

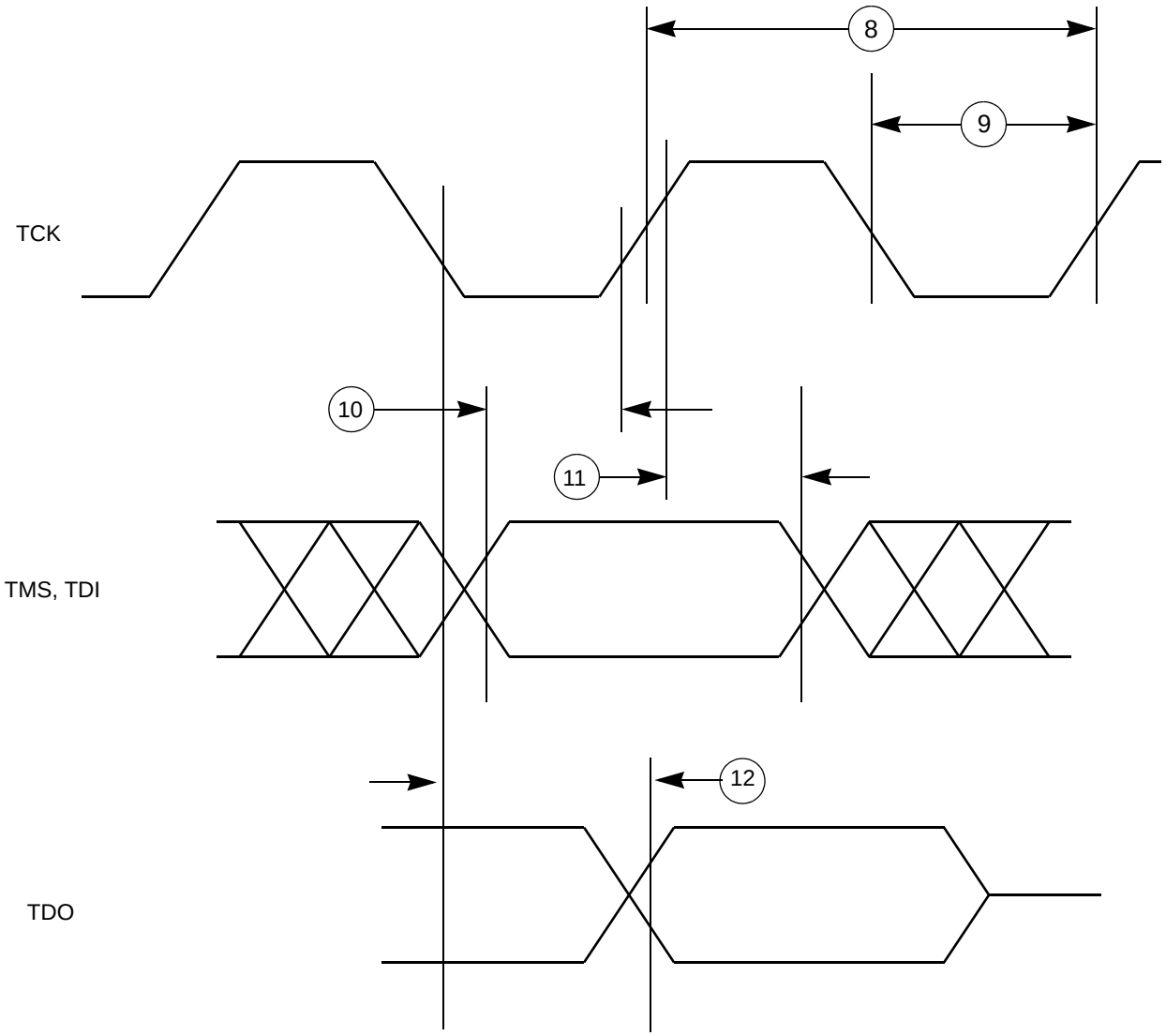

Figure 26. Nexus TCK, TDI, TMS, TDO Timing

4.12.6 External Interrupt Timing (IRQ Pin)

Table 36. External Interrupt Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}[2]
2	IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}[2]
3	IRQ Edge to Edge Time[3]	t_{ICYC}	6	—	t_{cyc}[2]

1 IRQ timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 See Notes on t_{cyc} on Figure 16 and Table 27 in Section 4.11.1, Clocking.

3 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

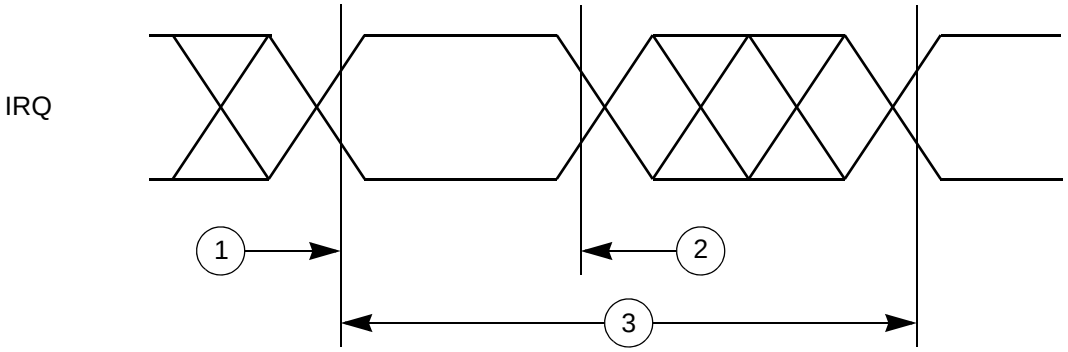

Figure 31. External Interrupt Timing

4.12.7 eTPU Timing

Table 37. eTPU Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{cyc}[2]
2	eTPU Output Channel Pulse Width	t_{OCPW}	1[3]	—	t_{cyc}[2]

1 eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 16 and Table 27 in Section 4.11.1, Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Table 39. DSPI Timing[1] [2] (continued)

Spec	Characteristic	Symbol	Peripheral Bus Freq: 132 MHz		Unit
			Min	Max	
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[8] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 20 4 6 20	 — — — —	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[8] Master (MTFE = 1, CPHA = 1)	t_{HI}	 –3 7 12 –3	 — — — —	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{SUO}	 — — — —	 5 25 13 5	 ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 –5 2.5 3 –5	 — — — —	 ns ns ns ns

1 DSPI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, and $T_A = T_L$ to T_H

2 Speed is the nominal maximum frequency of platform clock (f_{platf}). Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 Mhz for system core clock (f_{sys}) + 2% FM.

3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTAR*n*[PSSCK] and DSPI_CTAR*n*[CSSCK].

6 The maximum value is programmable in DSPI_CTAR*n*[PASC] and DSPI_CTAR*n*[ASC].

7 For example, external master should start SCK clock not earlier than 3 system clock periods after assertion SS

8 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

The DSPI in this device can be configured to serialize data to an external device that implements the Microsecond Bus protocol. DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) for data and clock signals to improve high speed operation.

Table 40. DSPI LVDS Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit
LVDS Clock to Data/Chip Select Outputs	$t_{LVDSDATA}$	–0.25 × t_{SCYC}	+0.25 × t_{SCYC}	ns

1 These are typical values that are estimated from simulation.

2 See DSPI LVDS Pad related data in Table 16.

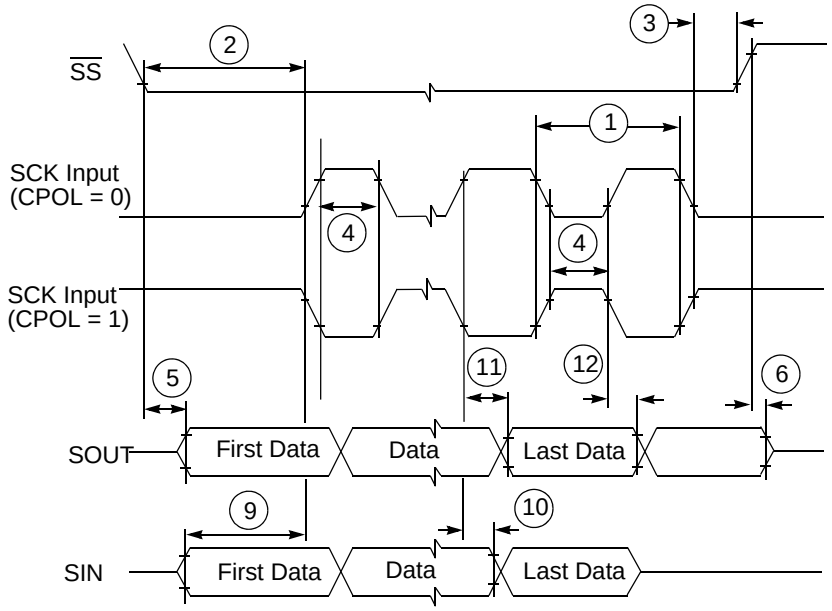

Figure 40. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

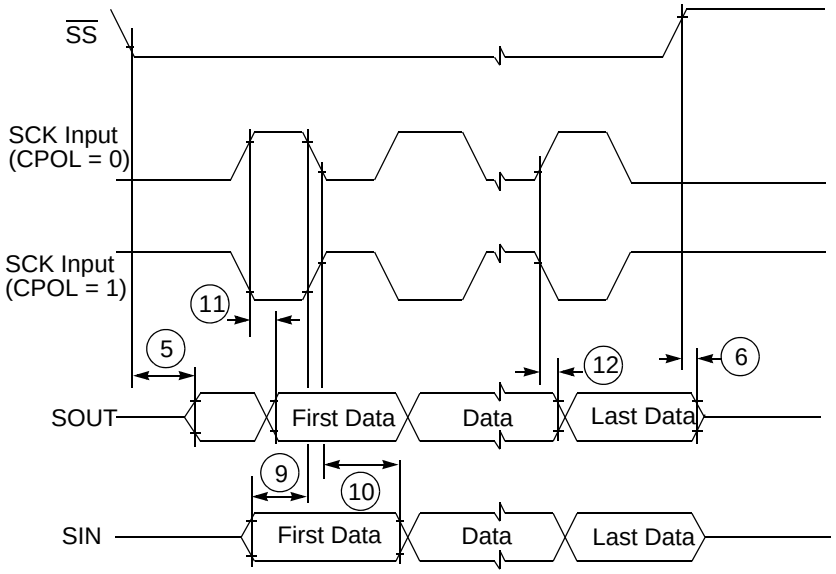

Figure 41. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

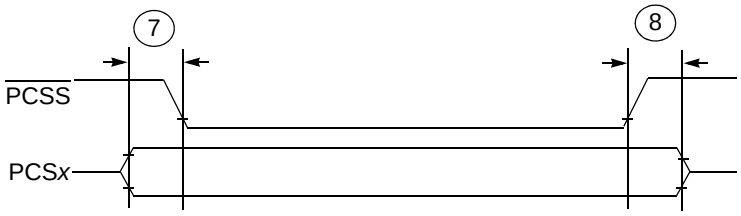

Figure 42. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

5.1 324-Pin Package

The package drawings of the 324-pin TEPBGA package are shown in Figure 43 and Figure 44.

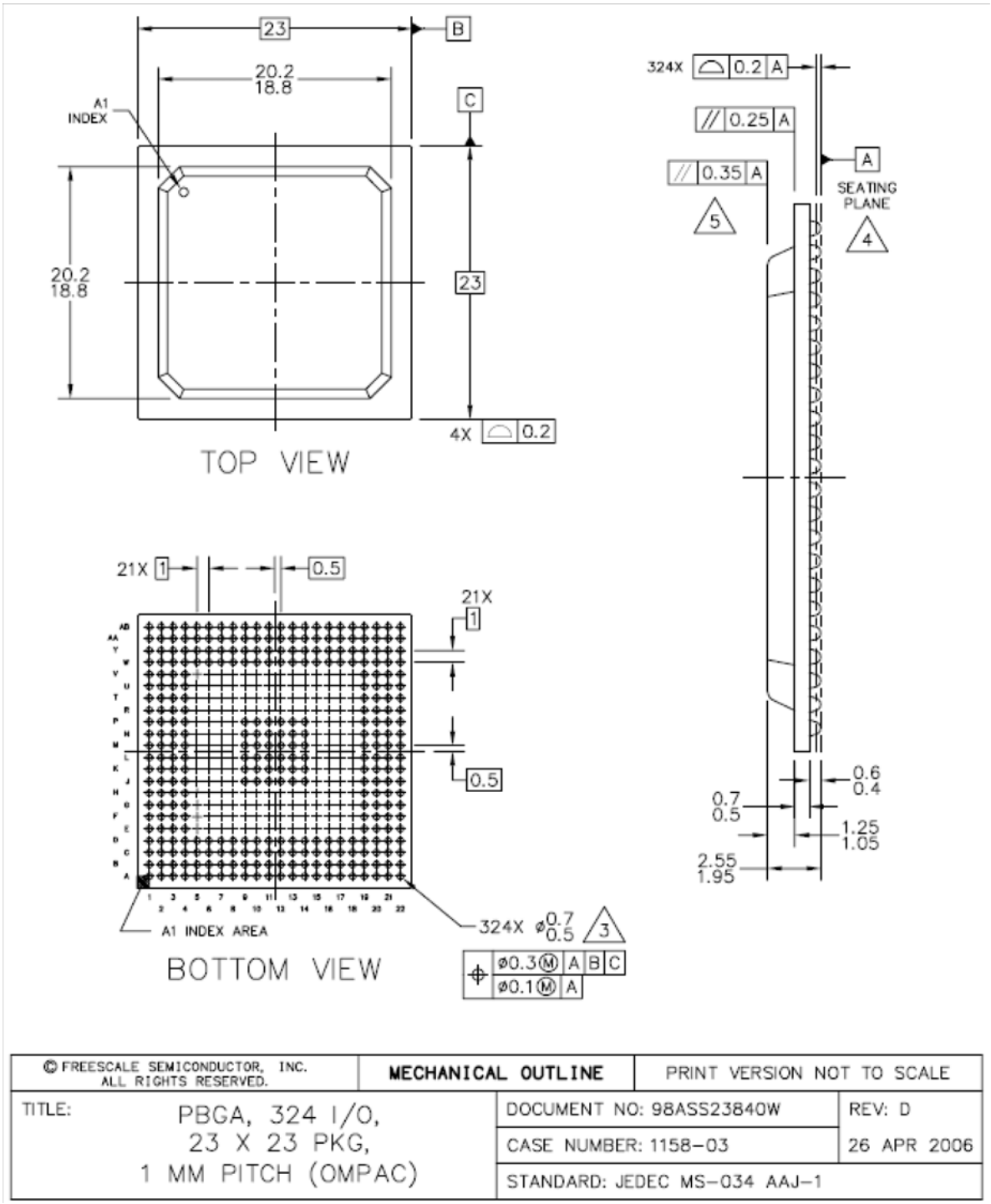

Figure 43. 324 TEPBGA Package (1 of 2)

5.2 416-Pin Package

The package drawings of the 416-pin TEPBGA package are shown in Figure 45 and Figure 46.

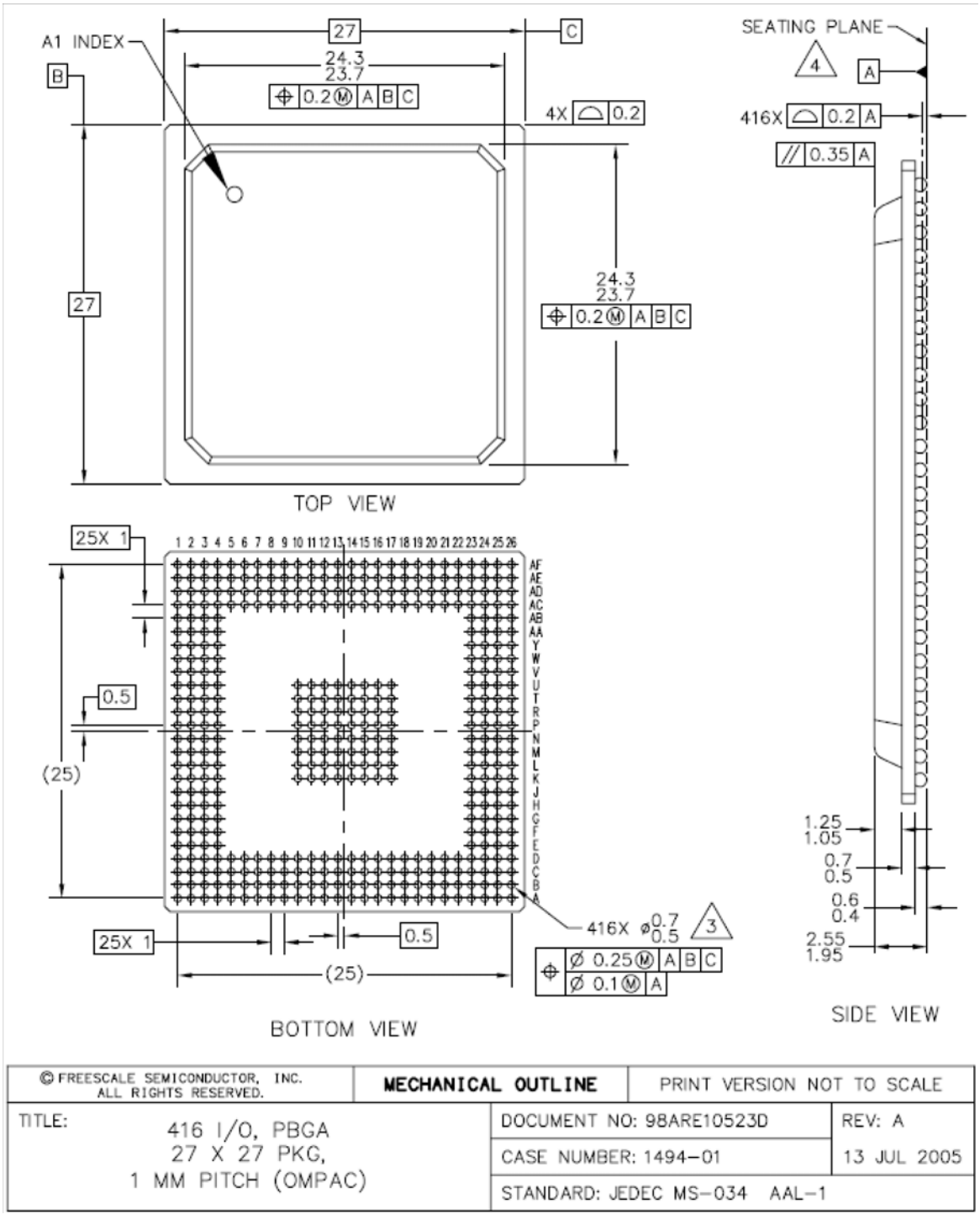

Figure 45. 416 TEPBGA Package (1 of 2)

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
161	ETPUB14_ETPUB30_ GPIO161	P	ETPUB14	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	L21	M25	R24
		A1	ETPUB30	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO161	GPIO	I/O							
162	ETPUB15_ETPUB31_ GPIO162	P	ETPUB15	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	—	M24	R25
		A1	ETPUB31	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO162	GPIO	I/O							
163	ETPUB16_PCSA1_ GPIO163	P	ETPUB16	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	P20	U26	V24
		A1	PCSA1	DSPI A peripheral chip select	O							
		A2	—	—	—							
		G	GPIO163	GPIO	I/O							
164	ETPUB17_PCSA2_ GPIO164	P	ETPUB17	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R20	U25	T21
		A1	PCSA2	DSPI A peripheral chip select	O							
		A2	—	—	—							
		G	GPIO164	GPIO	I/O							
165	ETPUB18_PCSA3_ GPIO165	P	ETPUB18	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	T20	U24	W26
		A1	PCSA3	DSPI A peripheral chip select	O							
		A2	—	—	—							
		G	GPIO165	GPIO	I/O							
166	ETPUB19_PCSA4_ GPIO166	P	ETPUB19	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	T19	U23	W25
		A1	PCSA4	DSPI A peripheral chip select	O							
		A2	—	—	—							
		G	GPIO166	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
433	EMIOS27_PCSB3_ GPIO433	P	EMIOS27	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W14	AC17	AD18
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO433	GPIO	I/O							
434	EMIOS28_PCSC0_ GPIO434	P	EMIOS28	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA16	AF18	AC18
		A1	PCSC0	DSPI C peripheral chip select	I/O							
		A2	—	—	—							
		G	GPIO434	GPIO	I/O							
435	EMIOS29_PCSC1_ GPIO435	P	EMIOS29	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA17	AE18	AB17
		A1	PCSC1	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO435	GPIO	I/O							
436	EMIOS30_PCSC2_ GPIO436	P	EMIOS30	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y17	AD18	AF19
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO436	GPIO	I/O							
437	EMIOS31_PCSC5_ GPIO437	P	EMIOS31	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W15	AC18	AA17
		A1	PCSC5	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO437	GPIO	I/O							
eQADC												
—	ANA0	P	ANA0[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA0	ANA0	A4	A4	A4
—	ANA1	P	ANA1[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA1	ANA1	A5	B5	B5
—	ANA2	P	ANA2[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA2	ANA2	B5	C5	C5

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	VSSA_B0	P	VSSA_B	Ground	I	VSSE	V_{SSA_B0}	VSSA_B0	VSSA_B0	B14	B17	B17
—	REFBYPCB1	P	REFBYPCB1	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB1	REFBYPCB1	A14	A17	A17
FlexRay												
248	FR_A_TX_ GPIO248	P	FR_A_TX	FlexRay A transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	Y5	AD4	AD4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO248	GPIO	I/O							
249	FR_A_RX_ GPIO249	P	FR_A_RX	FlexRay A receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AA4	AE3	AE3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO249	GPIO	I/O							
250	FR_A_TX_EN_ GPIO250	P	FR_A_TX_EN	FlexRay A transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AB3	AF3	AF3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO250	GPIO	I/O							
251	FR_B_TX_ GPIO251	P	FR_B_TX	FlexRay B transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	Y6	AD5	AD5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO251	GPIO	I/O							
252	FR_B_RX_ GPIO252	P	FR_B_RX	FlexRay B receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AA5	AE4	AE4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO252	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
253	FR_B_TX_EN_ GPIO253	P	FR_B_TX_EN	FlexRay B transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AB5	AF4	AF4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO253	GPIO	I/O							
FlexCAN												
83	CNTXA_TXDA_ GPIO83	P	CNTXA	FlexCAN A transmit	O	MH	V_{DDEH4}	—/Up	—/Up	AB17	AF19	AE19
		A1	TXDA	eSCI A transmit	O							
		A2	—	—	—							
		G	GPIO83	GPIO	I/O							
84	CNRXA_RXDA_ GPIO84	P	CNRXA	FlexCAN A receive	I	MH	V_{DDEH4}	—/Up	—/Up	AA18	AE19	AD19
		A1	RXDA	eSCI A receive	I							
		A2	—	—	—							
		G	GPIO84	GPIO	I/O							
85	CNTXB_PCSC3_ GPIO85	P	CNTXB	FlexCAN B transmit	O	MH	V_{DDEH4}	—/Up	—/Up	Y18	AD19	AC19
		A1	PCSC3	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO85	GPIO	I/O							
86	CNRXB_PCSC4_ GPIO86	P	CNRXB	FlexCAN B receive	I	MH	V_{DDEH4}	—/Up	—/Up	W18	AC19	AA19
		A1	PCSC4	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO86	GPIO	I/O							
87	CNTXC_PCSD3_ GPIO87	P	CNTXC	FlexCAN C transmit	O	MH	V_{DDEH4}	—/Up	—/Up	W16	AF20	AF20
		A1	PCSD3	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO87	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	VSSSYN	—	VSSSYN	Clock synthesizer ground input	I	VSSE	V_{DDSYN}	VSSSYN	VSSSYN	U22	AA26	AA26
—	VSTBY	—	VSTBY	SRAM standby power input	I	VHV	V_{DDEH1}	VSTBY	VSTBY	K4	M4	M4
—	REGSEL	—	REGSEL	Selects regulator mode (Linear/Switch mode)	I	AE	V_{DDREG}	REGSEL	REGSEL	V20	W23	W23
—	REGCTL	—	REGCTL	Regulator controller output to base/gate of power transistor	O	AE	V_{DDREG}	REGCTL	REGCTL	T22	Y26	Y26
—	VSSFL	—	VSSFL	Tie to V_{SS}	I	VSS	V_{DDREG}	VSSFL	VSSFL	V21	AB25	AB25
—	VDDREG	—	VDDREG	Source voltage for on-chip regulators and Low voltage detect circuits	I	VDDINT	V_{DDREG}	VDDREG	VDDREG	U21	AA25	AA25

1 The GPIO number is the same as the corresponding pad configuration register (SIU_PCRn) number in pins that have GPIO functionality. For pins that do not have GPIO functionality, this number is the PCR number.

2 The primary signal name is used as the pin label on the BGA map for identification purposes. However, the primary signal function is not available on all devices and is indicated by a dash in the following table columns: Signal Functions, P/F/G, and I/O Type.

3 P/A/G stands for Primary/Alternate/GPIO . This column indicates which function on a pin is Primary, Alternate 1, Alternate 2, (Alternate *n*) and GPIO.

4 Each line in the Function column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the SIU_PCRn registers except where explicitly noted.

5 MH = High voltage, medium speed
F = Fast speed
FS = Fast speed with slew
AE = Analog with ESD protection circuitry (up/down = pull up and pull down circuits included in the pad)
VHV = Very high voltage

6 VDDE (fast I/O) and VDDEH (slow I/O) power supply inputs are grouped into segments. Each segment of VDDEH pins can connect to a separate 3.3–5.0 V (+5%/–10%) power supply input. Each segment of VDDE pins can connect to a separate 1.8–3.3 V (±10%) power supply.

7 The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high, ABS — Auto Baud Select (during Reset or until JCOMP assertion). A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

8 The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

9 This signal name includes eTPU_C functionality that this device does not have. This is for forward compatibility with devices that have an eTPU_C.

10 During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

11 NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU_IREER and SIU_IFEER registers.

Table 43 lists the pin locations of the power and ground signals on the 324 TEPBGA package.

Table 43. 324-pin Power Supply Locations

VDD

A2	B3	C4	D5	K3	V19	W5	W9	W20	Y4	Y21	AA3	AA22	AB2

VDD33

W21	V4

VDDE2

AB4	M9	N1	N10	N9	P10	P9	T4	W6	V2

VDDEH1

B1	L4

VDDEH4

AB20	W8

VDDEH6

N20	T21

VDDEH7

C22	H19	L22

VSS

A1	A22	AA2	AA21	AB1	AB22	B2	B21	C20	C3	D19	D4	J10	J11	J12	J13	J14	J9
K10	K11	K12	K13	K14	K9	L10	L11	L12	L13	L14	L9	M10	M11	M12	M13	M14	N11
N12	N13	N14	P11	P12	P13	P14	W19	W4	Y20	Y3							

Table 45 lists the pin locations of the power and ground signals on the 516 TEPBGA package.

Table 45. 516-pin Power Supply Locations

VDD

A2	B3	C4	D5	E6	N4	AB4	AB23	AC3	AC12	AC24	AD2	AD25	AE1	AE26

VDD33

M1	P6	L21	AA4	AA11	AA14	AA23

VDDE10

F16	F17	F19	F21	N21	P21	AA22

VDDE2

N10	P10	P11	R10	R11	T1	T10	T11	T12	U10	U11	U12	W4	AC1	AC5	AF2

VDDE8

F6	F8	F10	F11	N6	AA5

VDDE9

AA13	AB6	AB7	AB18	AB19	AB20	AB21

VDDEH1

B1	P4

VDDEH3

AC10	AF5

VDDEH4

AC11	AF22

VDDEH5

AC21	AF25

VDDEH6

N23	AC25

VDDEH7

D24	E23	M26

VSS

A25	B2	B25	B26	C3	C24	D4	D23	E5	E7	E8	E9	E10	E11	E12	E13	E14	E15
E16	E17	E18	E19	E21	E22	F5	F13	F14	K10	K11	K12	K13	K14	K15	K16	K17	L10
L11	L12	L13	L14	L15	L16	L17	M10	M11	M12	M13	M14	M15	M16	M17	N11	N12	N13
N14	N15	N16	N17	P12	P13	P14	P15	P16	P17	R12	R13	R14	R15	R16	R17	T13	T14
T15	T16	T17	U13	U14	U15	U16	U17	AA6	AA21	AB5	AB22	AC4	AC23	AD3	AD24	AE2	AE25

Table 46. Revision History (continued)

Revision (Date)	Description of changes
8 (Jun-2011)	Removed spec 3 from Table 27 “PFCPR1 Settings vs Frequency of Operation” Updated spec 2a (Untrimmed VRC 1.2V) in Table 11 “PMC Electrical Specifications“ to a max value of VDD12OUT + 17%. Updated item 26 (Operating Current VDDA Supply) in table 14 “Electrical Specifications” from 30 mA to 40 mA. Updated Note 11 for Table 14 (Electrical Specifications) to read IOH_F = {16,32,47,77} mA and IOL_F = {24,48,71,115} mA for {00,01,10,11} drive mode with VDDE = 3.0 V. Updated ID 9 in Table 11 (PMC Electrical Specifications) to V_{REG} = 4.5 V, max DC output current with a max of 80 mA V_{REG} = 4.25 V, max DC output current, crank condition with a max of 40 mA Updated Table 17 (DSPI LVDS Pad Specification) with the following: • Spec 1 typical value updated from 40 MHz to 50 MHz • Spec 2 added SRC conditions and associated values: – SRC=0b00 or SRC=0b11 Min 150 mV Max 400 mV – SRC=0b01 Min 90 mV Max 320 mV – SRC=0b10 Min 160 mV Max 480 mV • Spec 3 - Min value from 1.075 V to 1.06 V - Max value from 1.325 V to 1.39 V • Added Spec 5, 6 and 7
	Updated table 17 "DSPI LVDS pad specification" to include Temperature with a min value of -40 C and max of 150 C Updated Spec 5 of Table 18, "FMPLL Electrical Specifications" to < 400 us as the Max vaule. Added the sentence "Violating the VCO min/max range may prevent the system from exiting reset." to the end of Footnote 16 of Table 18, "FMPLL Electrical Specifications" Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", Crystal Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz. Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", External Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz. Removed Note 9, 'Duty cycle can be 20–80% when PLL is used with a pre-divider greater than 1', from Table 18, "FMPLL Electrical Specifications". Updated ID 16 in Table 11, “PMC Electrical Specifications”, SMPS regulator clock frequency (after reset) 2.4MHz Max
	Updated Table 16 “Flash EEPROM Module Life”, spec 3, ‘Blocks with 10,001–100,000 P/E cycles’ to 5 Years. Added Typ column to Table 25, “Flash Program and Erase Specifications”