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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	32
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674ff3mvy3r

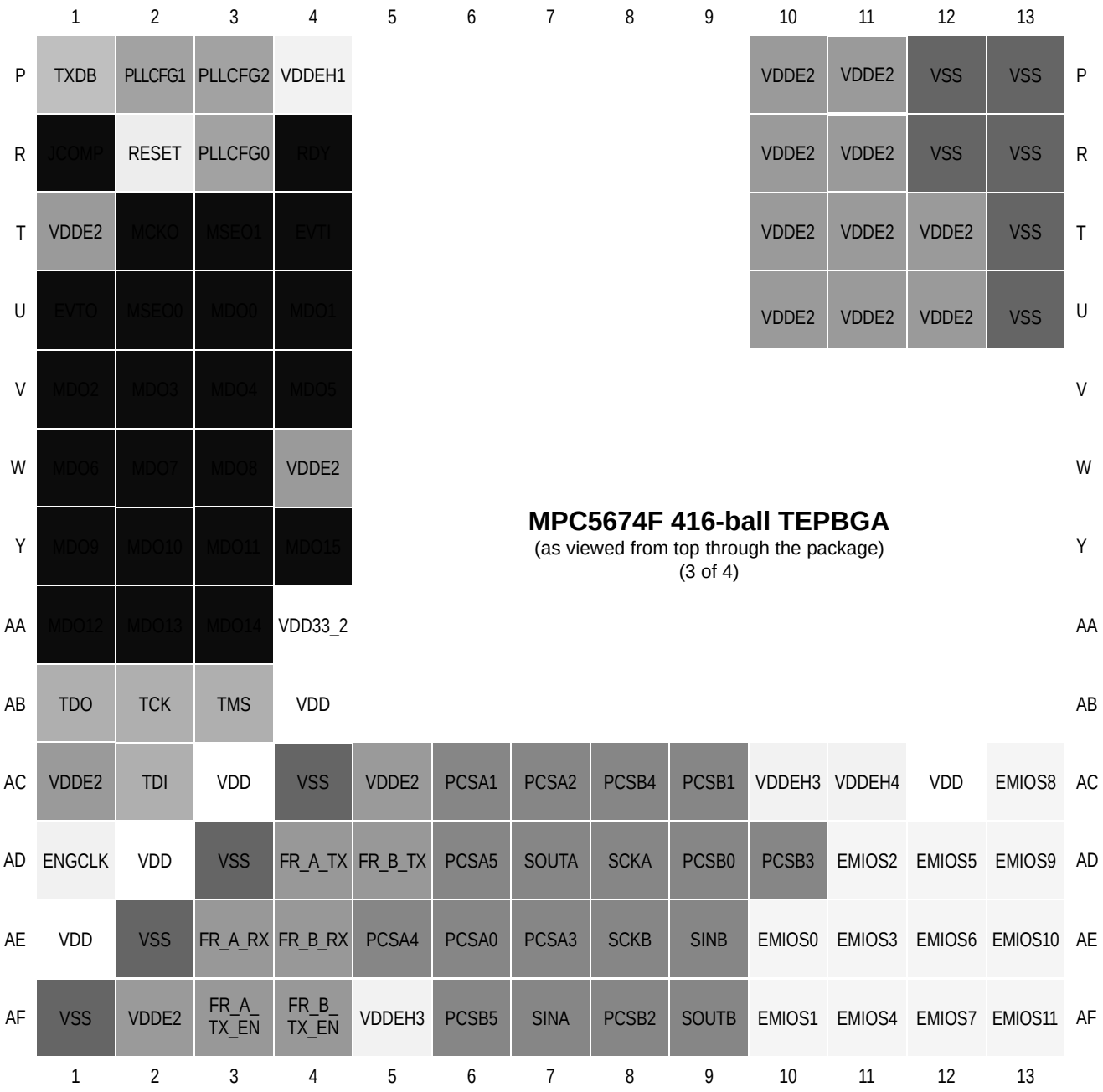

Figure 9. MPC5674F 416-ball TEPBGA (3 of 4)

MPC5674F 416-ball TEPBGA
(as viewed from top through the package)
(4 of 4)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
P	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V										ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W										REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y										ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA										VDD33_3	ETPUB30	VDDREG	VSSSYN	AA
AB										VDD	ETPUB31	VSSFL	EXTAL	AB
AC	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 10. MPC5674F 416-ball TEPBGA (4 of 4)

MPC5674F 516-ball TEPBGA
(as viewed from top through the package)
(4 of 4)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
P	VSS	VSS	VSS	VSS				VDDE10	ETPUB13	D_OE	D_ALE	D_DAT0	D_DAT1	P
R	VSS	VSS	VSS	VSS					ETPUB9	ETPUB12	ETPUB14	ETPUB15	D_RD_WR	R
T	VSS	VSS	VSS	VSS				ETPUB17	ETPUB3	ETPUB7	ETPUB8	ETPUB10	ETPUB11	T
U	VSS	VSS	VSS	VSS				ETPUB23	ETPUB1	ETPUB2	ETPUB4	ETPUB5	ETPUB6	U
V									ETPUB21	ETPUB22	ETPUB16	TCRCLKB	ETPUB0	V
W								ETPUB25	ETPUB29	REGSEL	ETPUB20	ETPUB19	ETPUB18	W
Y									ETPUB31	ETPUB26	ETPUB27	ETPUB24	REGCTL	Y
AA	VDD33_4		EMIOS23	EMIOS31		CNRXB		VSS	VDDE10	VDD33_3	ETPUB28	VDDREG	VSSSYN	AA
AB	EMIOS11	EMIOS17	EMIOS19	EMIOS29	VDDE9	VDDE9	VDDE9	VDDE9	VSS	VDD	ETPUB30	VSSSFL	EXTAL	AB
AC	EMIOS8	EMIOS13	EMIOS22	EMIOS24	EMIOS28	CNTXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	EMIOS7	EMIOS12	EMIOS16	EMIOS18	EMIOS27	CNRXA	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	EMIOS6	EMIOS10	EMIOS15	EMIOS21	EMIOS26	CNTXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	EMIOS5	EMIOS9	EMIOS20	EMIOS14	EMIOS25	EMIOS30	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5		AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 15. MPC5674F 516-ball TEPBGA (4 of 4)

Table 14. DC Electrical Specifications (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Clock Synthesizer Operating Voltage[9]	V_{DDSYN}	3.0	3.6[1,4]	V
9	Fast I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_F}	 0.65 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Fast I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_F}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE}	V
11	Medium I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_S}	 0.65 × V_{DDEH} 0.55 × V_{DDEH}	V_{DDEH} + 0.3	V
12	Medium I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_S}	V_{SS} – 0.3	 0.35 × V_{DDEH} 0.40 × V_{DDEH}	V
13	Fast I/O Input Hysteresis	V_{HYS_F}	0.1 × V_{DDE}	—	V
14	Medium I/O Input Hysteresis	V_{HYS_S}	0.1 × V_{DDEH}	—	V
15	Analog Input Voltage	V_{INDC}	V_{SSA} – 0.1	V_{DDA} + 0.1	V
16	Fast I/O Output High Voltage[10]	V_{OH_F}	0.8 × V_{DDE}	—	V
17	Medium I/O Output High Voltage[11]	V_{OH_S}	0.8 × V_{DDEH}	—	V
18	Fast I/O Output Low Voltage[10]	V_{OL_F}	—	0.2 × V_{DDE}	V
19	Medium I/O Output Low Voltage[11]	V_{OL_S}	—	0.2 × V_{DDEH}	V
20	Load Capacitance (Fast I/O)[12] DSC(PCR[8:9]) = 0b00 DSC(PCR[8:9]) = 0b01 DSC(PCR[8:9]) = 0b10 DSC(PCR[8:9]) = 0b11	C_L	 — — — —	 10 20 30 50	 pF pF pF pF
21	Input Capacitance (Digital Pins)	C_{IN}	—	7	pF
22	Input Capacitance (Analog Pins)	C_{IN_A}	—	10	pF
24	Operating Current 1.2 V Supplies @ f_{sys} = 264 MHz V_{DD} @1.32 V V_{STBY}[13] @1.2 V and 85°C V_{STBY} @6.0 V and 85°C	 I_{DD} I_{DDSTBY} $I_{DDSTBY6}$	 — — —	 850 0.10 0.15	 mA mA mA
25	Operating Current 3.3 V Supplies @ f_{sys} = 264 MHz V_{DD33}[14] V_{DDSYN}	 I_{DD33} I_{DDSYN}	 — —	 note[14] 7[15]	 mA mA
26	Operating Current 5.0 V Supplies @ f_{sys} = 264 MHz V_{DDA} Analog Reference Supply Current (Transient) V_{DDREG}	 I_{DDA} I_{REF} I_{REG}	 — — —	 50[16] 1.0 22	 mA mA mA

Table 17. FMPLL Electrical Specifications[1] (continued)

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
5	Duty Cycle of Reference [7]	t_{DC}	40	60	%
6	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{sys}
7	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{sys}
8	D_CLKOUT Period Jitter[8, 9] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{clkout}
9	Peak-to-Peak Frequency Modulation Range Limit [10,11] (f_{sys} Max must not be exceeded)	C_{mod}	0	4	%f_{sys}
10	FM Depth Tolerance[12]	C_{mod_err}	–0.25	0.25	%f_{sys}
11	VCO Frequency	f_{VCO}	192	600	MHz
12	Modulation Rate Limits[13]	f_{mod}	0.400	1	MHz
13	Predivider output frequency range[14]	f_{prediv}	4	10	MHz

1 All values given are initial design targets and subject to change.

2 Crystal and External reference frequency limits depend on device relying on PLL to lock prior to release of reset, default PREDIV/EPREDIV, MFD/EMFD default settings, and VCO frequency range. Absolute minimum loop frequency is 4 MHz.

3 Upper tolerance of less than 1% is allowed on 40MHz crystal.

4 “Loss of Reference Frequency” is the reference frequency detected internally, which transitions the PLL into self clocked mode.

5 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}. This frequency is measured at D_CLKOUT. A default RFD value of (0x05) is used in SCM mode, and the programmed MFD and RFD values have no effect

6 This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

7 For Flexray operation, duty cycle requirements are higher.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval. D_CLKOUT divider set to divide-by-2.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

10 Modulation depth selected must not result in f_{pll} value greater than the f_{pll} maximum specified value.

11 Maximum and minimum variation from programmed modulation depth is pending characterization. Depth settings available in control register are: 2%, 3%, and 4% peak-to-peak.

12 Depth tolerance is the programmed modulation depth ±0.25% of F_{sys}. Violating the VCO min/max range may prevent the system from exiting reset.

13 Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

14 Violating this range will cause the VCO max/min range to be violated with the default MFD settings out of reset.

Table 19. eQADC Conversion Specifications (Operating) (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
9	Offset Error without Calibration	OFFNC	0[4]	100[4]	LSB
10	Offset Error with Calibration	OFFWC	–4[4]	4[4]	LSB
11	Full Scale Gain Error without Calibration	GAINNC	–120[4]	0[4]	LSB
12	Full Scale Gain Error with Calibration	GAINWC	–4[4,6]	4[4,6]	LSB
13	Non-Disruptive Input Injection Current [7, 8, 9, 10]	I_{INJ}	–3	3	mA
14	Incremental Error due to injection current[11, 12]	E_{INJ}	–4[4]	4[4]	Counts
15	TUE value at 8 MHz [13, 14] (with calibration)	TUE8	–4[4,6]	4[4,6]	Counts
16	TUE value at 16 MHz [13, 14] (with calibration)	TUE16	–8	8	Counts
17	Maximum differential voltage[15] (DANx+ - DANx-) or (DANx- - DANx+) PREGAIN set to 1X setting PREGAIN set to 2X setting PREGAIN set to 4X setting	 $DIFF_{max}$ $DIFF_{max2}$ $DIFF_{max4}$	 — — —	 $(V_{RH} – V_{RL})/2$ $(V_{RH} – V_{RL})/4$ $(V_{RH} - V_{RL})/8$	 V V V
18	Differential input Common mode voltage[15] (DANx- + DANx+)/2	$DIFF_{cmv}$	$(V_{RH} – V_{RL})/2$ – 5%	$(V_{RH} – V_{RL})/2$ + 5%	V

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} – V_{RL}$ = 5.12 V, one count = 1.25 mV without using pregain.

3 INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB. The eQADC is guaranteed to be monotonic at 10 bit accuracy (12 bit resolution selected).

4 New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

5 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

6 The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

7 Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.

8 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = –0.3 V, then use the larger of the calculated values.

10 Condition applies to two adjacent pins at injection limits.

11 Performance expected with production silicon.

12 All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, I_{INJ}=I_{INJMAX},I_{INJMIN}.

13 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

14 TUE does not apply to differential conversions.

15 Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

Table 22. ADC Band Gap Reference / LVI Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	1.171	1.220	1.269	V

Table 23. Temperature Sensor Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	Slope –40 °C to 100 °C ±1.0 °C 100 °C to 150 °C ±1.6 °C ADC0 channel 128 ADC1 channel 128	$V_{SADC128}$[1]	—	5.8	—	mV/ °C
2	Accuracy –40 °C to 150 °C ADC0 channel 128 ADC1 channel 128	—	—	±10.0	—	°C

1 Slope is the measured voltage change per °C.

4.10 C90 Flash Memory Electrical Characteristics

Table 24. Flash Program and Erase Specifications

Spec	Characteristic	Symbol	Min	Typ[1]	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	38	—	500	µs
2	Page Program Time[4,5]	$t_{pprogram}$	—	45	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	270	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	800	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	1500	2600	7500	ms
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	3000	5200	15000	ms

1 Typical program and erase times assume nominal supply values and operation at 25 ^{o}C.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Program times are actual hardware programming times and do not include software overhead.

5 Page size is 128 bits (4 words).

4.11.2 Pad AC Specifications

Table 30. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,4] L → H/H → L (ns)	Rise/Fall[3,4] (ns)	Load Drive (pF)
1	Medium[5]	00	152/165	70/74	50
2			205/220	96/96	200
3		01	28/34	12/15	50
4			52/59	28/31	200
5		11	12/12	5.3/5.9	50
6			32/32	22/22	200
7	Fast[5]	00	2.5	1.2	10
8		01			20
9		10			30
10		11			50
11	Fast with Slew Rate	00	40/40	16/16	50
12			50/50	21/21	200
13		01	13/13	5/5	50
14			19/19	8/8	200
15		10	8/8	2.4/2.4	50
16			12/12	5/5	200
17		11	5/5	1.1/1/1	50
18			8/8	2.6	2.6
19	Pull Up/Down (3.6 V max)	—	—	7500	50
20	Pull Up/Down (5.25 V max)	—	6000	5000/5000	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.02 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 4.75 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Delay and rise/fall are measured to 20% or 80% of the respective signal.

5 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

[2] See Notes on t_{cyc} on Figure 16 and Table 27 in Section 4.11.1, “Clocking.”

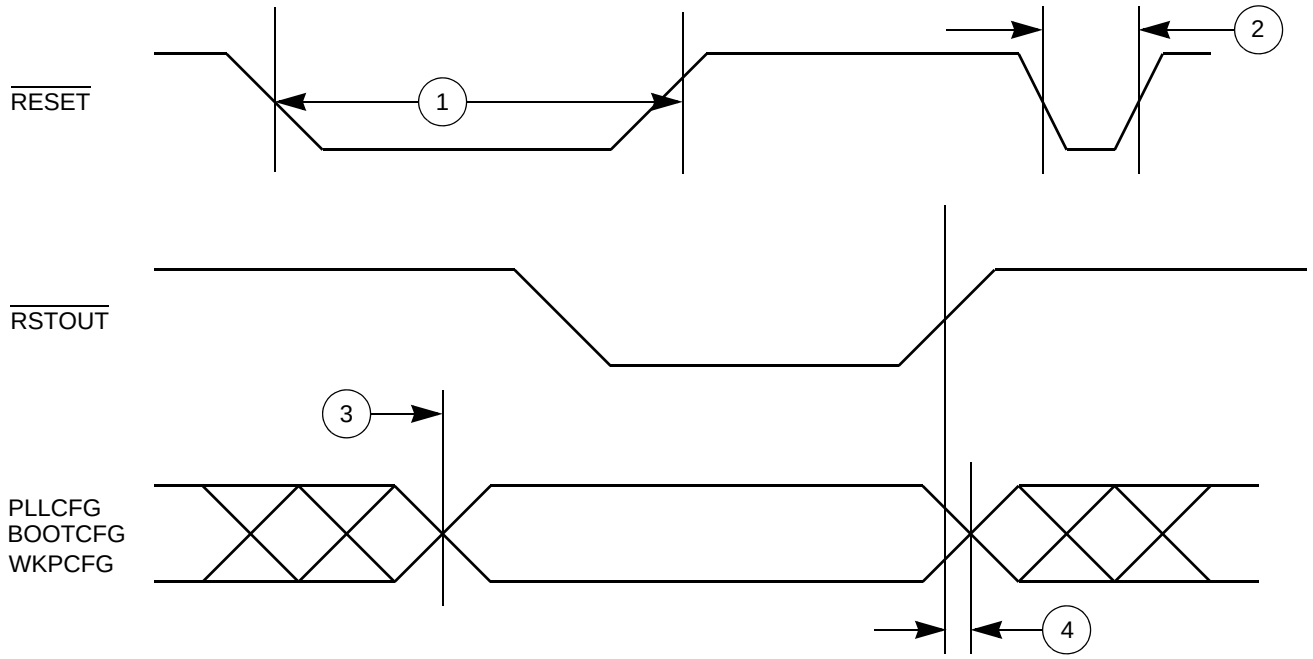

Figure 20. Reset and Configuration Pin Timing

4.12.3 IEEE 1149.1 Interface Timing

Table 33. JTAG Pin AC Electrical Characteristics[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at V_{DDE} / 2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40%–70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	10	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] JTAG timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10, SRC = 0b00. These specifications apply to JTAG boundary scan only. See Table 34 for functional specifications.

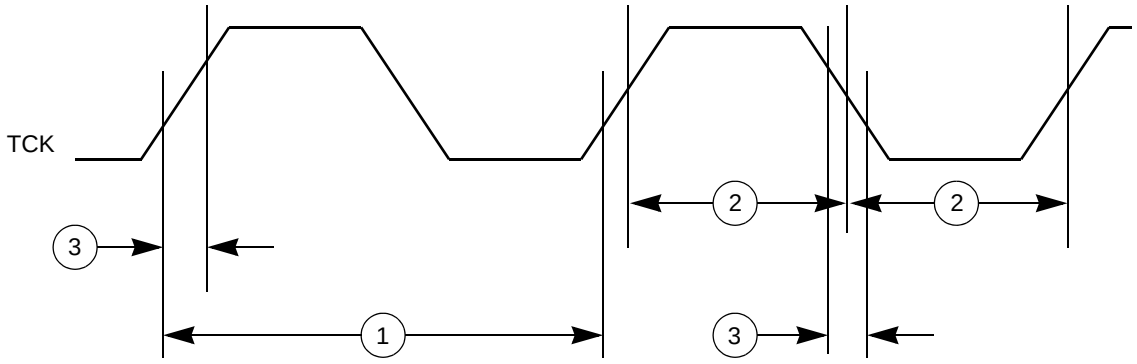

Figure 21. JTAG Test Clock Input Timing

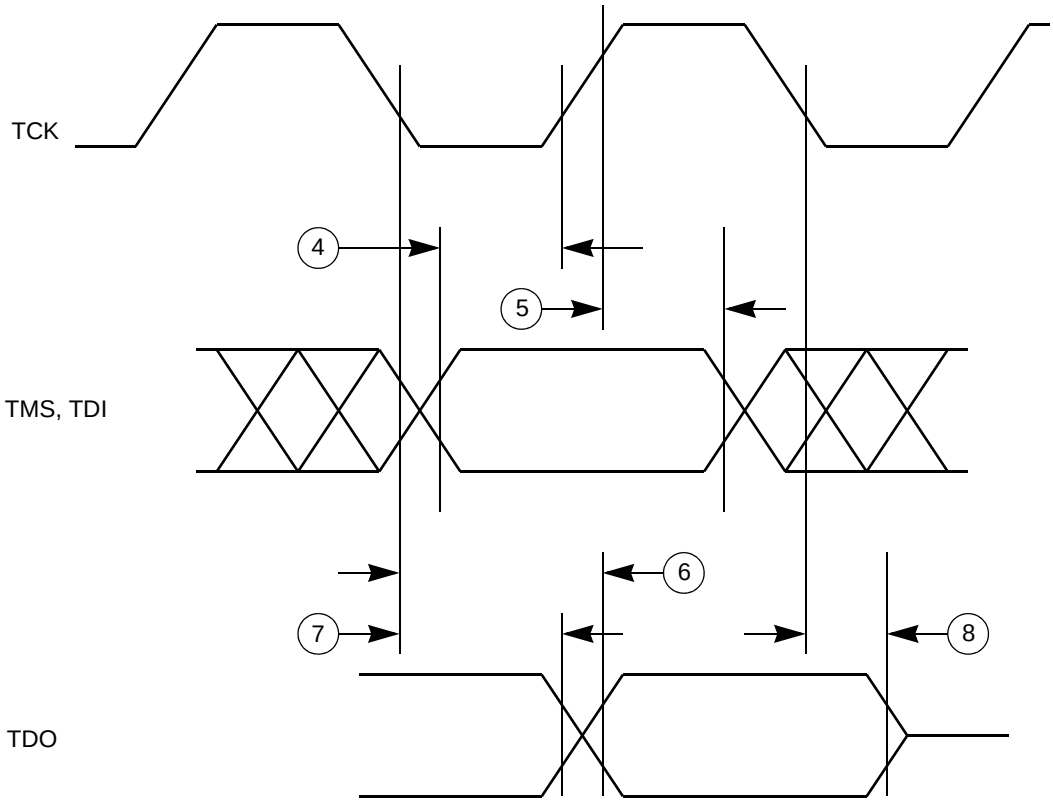

Figure 22. JTAG Test Access Port Timing

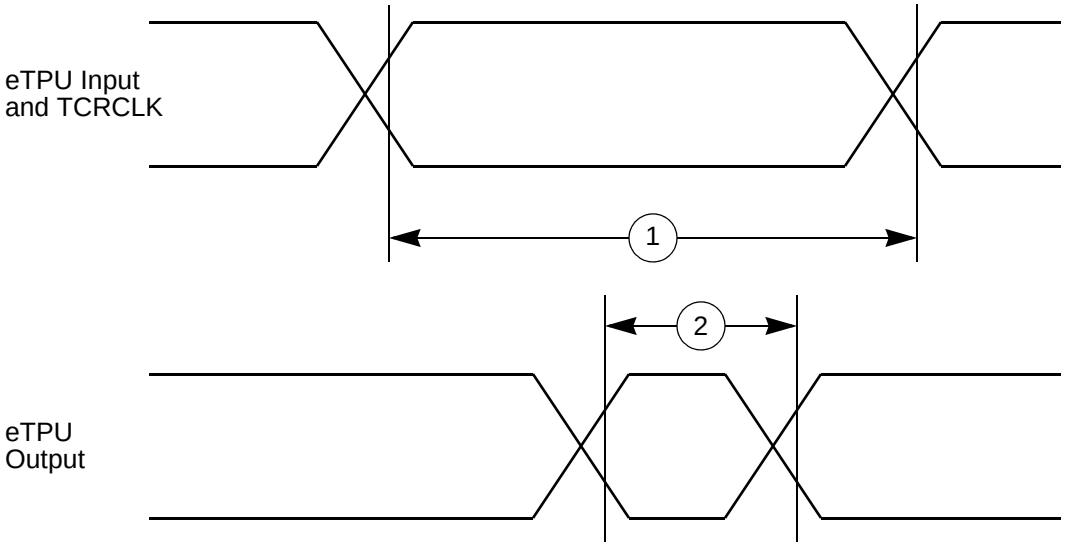

Figure 32. eTPU Timing

4.12.8 eMIOS Timing

Table 38. eMIOS Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{cyc}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{cyc}[2]

1 eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 16 and Table 27 in Section 4.11.1, Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

5.3 516-Pin Package

The package drawings of the 516-pin TEPBGA package are shown in Figure 47 and Figure 48.

Figure 47. 516 TEPBGA Package (1 of 2)

Appendix A Signal Properties and Muxing

The following table shows the signals properties for each pin on the MPC5674F. For each port pin that has an associated SIU_PCR*n* register to control its pin properties, the supported functions column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit in the order: Primary function (P), Function 2 (F2), Function 3 (F3), and GPIO (G). See Figure 49.

Table 2. Signal Properties Summary

GPIO/ PCR[1]	Signal Name[2]	P/ F/ G	Function[3]	Function Summary	I/O	Pad Type
113	TCRCLKA_IRQ7_GPIO113	P	TCRCLKA	eTPU A TCR clock	I	5V M
		A1	IRQ7	External interrupt request	I	
		A2	—	—	—	
		G	GPIO113	GPIO	I/O	

Primary Functions are listed First

Secondary Functions are alternate functions

GPIO Functions are listed **Last**

Function not implemented on this device

Figure 49. Supported Functions Example

Table 42. Signal Properties and Muxing Summary

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
eTPU_A												
113	TCRCLKA_IRQ7_ GPIO113	P	TCRCLKA	eTPU A TCR clock	I	MH	V_{DDEH1}	—/Up	—/Up	K1	L1	K4
		A1	IRQ7	External interrupt request	I							
		A2	—	—	—							
		G	GPIO113	GPIO	I/O							
114	ETPUA0_ETPUA12_ GPIO114	P	ETPUA0	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K2	L2	L6
		A1	ETPUA12	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO114	GPIO	I/O							
115	ETPUA1_ETPUA13_ GPIO115	P	ETPUA1	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J1	L3	J1
		A1	ETPUA13	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO115	GPIO	I/O							
116	ETPUA2_ETPUA14_ GPIO116	P	ETPUA2	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J2	L4	J2
		A1	ETPUA14	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO116	GPIO	I/O							
117	ETPUA3_ETPUA15_ GPIO117	P	ETPUA3	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J3	K1	H4
		A1	ETPUA15	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO117	GPIO	I/O							
118	ETPUA4_ETPUA16_ GPIO118	P	ETPUA4	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J4	K2	J4
		A1	ETPUA16	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO118	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
452	ETPUC11_IRQ2_ GPIO452[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	E21	G23	G22
		A1	IRQ2	External interrupt request	I							
		A2	—	—	—							
		G	GPIO452	GPIO	I/O							
453	ETPUC12_IRQ3_ GPIO453[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F19	G24	G23
		A1	IRQ3	External interrupt request	I							
		A2	—	—	—							
		G	GPIO453	GPIO	I/O							
454	ETPUC13_3_IRQ4_ GPIO454[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F21	G25	G24
		A1	IRQ4	External interrupt request	I							
		A2	—	—	—							
		G	GPIO454	GPIO	I/O							
455	ETPUC14_4_IRQ5_ GPIO455[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F20	G26	G25
		A1	IRQ5	External interrupt request	I							
		A2	—	—	—							
		G	GPIO455	GPIO	I/O							
456	ETPUC15__ GPIO456[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	—	H23	G26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO456	GPIO	I/O							
457	ETPUC16_FR_A_TX_ GPIO457[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	—	H24	H22
		A1	FR_A_TX	FlexRay A transfer	O							
		A2	—	—	—							
		G	GPIO457	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
470	ETPUC29_SCKD_ GPIO470[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K21	L25	K23
		A1	SCKD	DSPI D clock	I/O							
		A2	—	—	—							
		G	GPIO470	GPIO	I/O							
471	ETPUC30_SOUTD_ GPIO471[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K20	L26	K24
		A1	SOUTD	DSPI D data output	O							
		A2	—	—	—							
		G	GPIO471	GPIO	I/O							
472	ETPUC31_SIND_ GPIO472[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K19	M23	K25
		A1	SIND	DSPI D data input	I							
		A2	—	—	—							
		G	GPIO472	GPIO	I/O							
eMIOS												
179	EMIOS0_ETPUA0_ GPIO179	P	EMIOS0	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA9	AE10	AC13
		A1	ETPUA0	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO179	GPIO	I/O							
180	EMIOS1_ETPUA1_ GPIO180	P	EMIOS1	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB9	AF10	AB13
		A1	ETPUA1	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO180	GPIO	I/O							
181	EMIOS2_ETPUA2_ GPIO181	P	EMIOS2	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y10	AD11	AD13
		A1	ETPUA2	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO181	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
182	EMIOS3_ETPUA3_ GPIO182	P	EMIOS3	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA10	AE11	AE13
		A1	ETPUA3	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO182	GPIO	I/O							
183	EMIOS4_ETPUA4_ GPIO183	P	EMIOS4	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB10	AF11	AF13
		A1	ETPUA4	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO183	GPIO	I/O							
184	EMIOS5_ETPUA5_ GPIO184	P	EMIOS5	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y11	AD12	AF14
		A1	ETPUA5	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO184	GPIO	I/O							
185	EMIOS6_ETPUA6_ GPIO185	P	EMIOS6	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	—	AE12	AE14
		A1	ETPUA6	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO185	GPIO	I/O							
186	EMIOS7_ETPUA7_ GPIO186	P	EMIOS7	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB11	AF12	AD14
		A1	ETPUA7	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO186	GPIO	I/O							
187	EMIOS8_ETPUA8_ GPIO187	P	EMIOS8	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	W10	AC13	AC14
		A1	ETPUA8	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO187	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	VSSA_B0	P	VSSA_B	Ground	I	VSSE	V_{SSA_B0}	VSSA_B0	VSSA_B0	B14	B17	B17
—	REFBYPCB1	P	REFBYPCB1	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB1	REFBYPCB1	A14	A17	A17
FlexRay												
248	FR_A_TX_ GPIO248	P	FR_A_TX	FlexRay A transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	Y5	AD4	AD4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO248	GPIO	I/O							
249	FR_A_RX_ GPIO249	P	FR_A_RX	FlexRay A receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AA4	AE3	AE3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO249	GPIO	I/O							
250	FR_A_TX_EN_ GPIO250	P	FR_A_TX_EN	FlexRay A transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AB3	AF3	AF3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO250	GPIO	I/O							
251	FR_B_TX_ GPIO251	P	FR_B_TX	FlexRay B transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	Y6	AD5	AD5
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO251	GPIO	I/O							
252	FR_B_RX_ GPIO252	P	FR_B_RX	FlexRay B receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AA5	AE4	AE4
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO252	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
EBI												
256	D_CS0_ GPIO256	P	D_CS0	EBI chip select 0	O	F	V_{DDE9}	—/Up	—/Up	—	—	AD9
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO256	GPIO	I/O							
257	D_CS2_D_ADD_DAT31_ GPIO257	P	D_CS2	EBI chip select 2	O	F	V_{DDE8}	—/Up	—/Up	—	—	U1
		A1	D_ADD_DAT31	EBI data only in non-mux mode. Address and data in mux mode.	I/O							
		A2	—	—	—							
		G	GPIO257	GPIO	I/O							
258	D_CS3_D_TEA_ GPIO258	P	D_CS3	EBI chip select 3	O	F	V_{DDE8}	—/Up	—/Up	—	—	T6
		A1	D_TEA	EBI transfer error acknowledge	I							
		A2	—	—	—							
		G	GPIO258	GPIO	I/O							
259	D_ADD12_ GPIO259	P	D_ADD12	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R1
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO259	GPIO	I/O							
260	D_ADD13_ GPIO260	P	D_ADD13	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R2
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO260	GPIO	I/O							
261	D_ADD14_ GPIO261	P	D_ADD14	EBI address bus	I/O	F	V_{DDE8}	—/Up	—/Up	—	—	R3
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO261	GPIO	I/O							

Table 46. Revision History (continued)

Revision (Date)	Description of changes
9 (Oct-2012)	Updated Table 1 (Orderable Part Numbers) with actual available parts.Added new part number SPC5673FF3MVY2 ,Package description 516 PBGA, w/EBI, Pb-free.Speed is 200Mhz nom and max. —Removed note attached to “Orderable Part Numbers” and “Freescale Part Number”. Updated footnotes of Table 3 (Absolute Maximum Ratings) to: • 2.0 V for 10 hours cumulative time, 1.2V +10% for time remaining. • 6.4 V for 10 hours cumulative time, 5.0V +10% for time remaining. • 5.3 V for 10 hours cumulative time, 3.3V +10% for time remaining. Updated Table 6 (Thermal Characteristics, 324-pin Package) to show MPC5674F thermal characteristics. In Table 10 (PMC Operating conditions) updated the parameter “Supply voltage VDD 1.2V nominal" to “Core supply voltage". In Table 11 (PMC Electrical Specifications) updated the following rows: —Parameter “Nominal VRC regulated 1.2V output VDD” updated column “Typ” to 1.27 V. —The minimum and maximum value of “Untrimmed VRC 1.2V output variation before band gap trim (unloaded)” updated to “-14%” and “+10%” respectively. —The minimum and maximum value of “Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max 1A)” updated to “-10%” and “+5%” respectively. In Table 12 (Power Sequence Pin States for MH and AE pads) updated the row(VDD33 = low, VDDE = high), parameter “MH+LVDS Pads” to “Outputs disabled”. In Table 13 (Power Sequence Pin States for F and FS pads) updated the rows (VDD = low, VDD33 = low, VDDE = high) and (VDD = high, VDD33 = low, VDDE = high) ,parameter “F and FS pad” to “Outputs disabled”. In Table 14 (DC Electrical Specifications) updated the spec 24 “Operating Current 1.2 V Supplies @ f_{SYS} = 264 MHz” with 'V_{DD} @ 1.32 V' Max value to 850 mA from 1.0 A, and deleted corresponding footnote stating that the previous information was preliminary. Updated current(mA) values in Table 15 (V_{DDE}/V_{DDEH} I/O Pad Average DC Current) from Spec 5 to 13. -Spec 5 Current (mA) from 6.5 to 7.4 -Spec 6 Current (mA) from 9.4 to 10.5 -Spec 7 Current (mA) from 10.8 to 12.3 -Spec 8 Current (mA) from 33.3 to 35.2 -Spec 9 Current (mA) from 12.0 to 12.7 -Spec 10 Current (mA) from 6.2 to 6.7 -Spec 11 Current (mA) from 4.0 to 4.2 -Spec 12 Current (mA) from 2.4 to 2.6 -Spec 13 Current (mA) from8.9 to 9.1 In Table 34 (Nexus Debug Port Timing) updated the footnote of parameter “t_{CYC}” to “See Notes on tcyc in Table 27 “.Removed references to “Section I/O Pad VDD33 Current Specifications” .