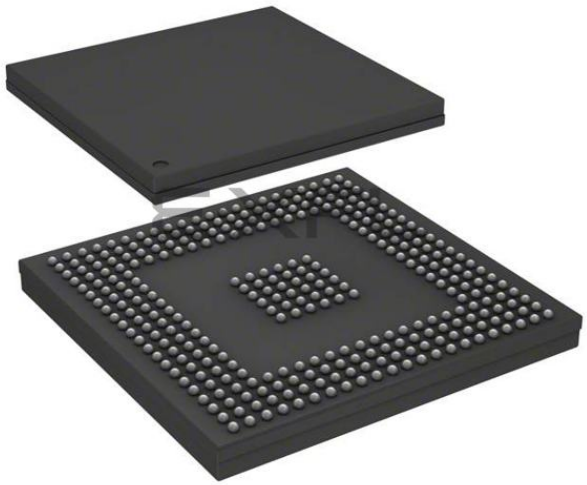

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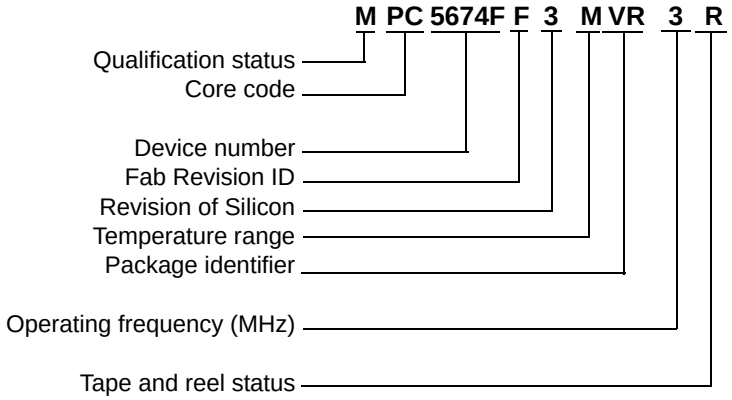
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z7
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, SCI, SPI
Peripherals	DMA, POR, PWM
Number of I/O	22
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 5.25V
Data Converters	A/D 48x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674ff3mvz2

1 Ordering Information

1.1 Orderable Parts

Figure 1 and Table 1 describe and list the orderable part numbers for the MPC5674F.



Note: Not all options are available on all devices. Refer to Table 1.

Temperature Range
M = –40 °C to 125 °C

Package Identifier
VZ = 324 BGA Pb-free
VR = 416 BGA Pb-free
VY = 516 BGA Pb-free
VV = 516 BGA SnPb

Operating Frequency
2 = 200 MHz
3 = 264 MHz

Tape and Reel Status
R = Tape and reel
(blank) = Trays

Qualification Status
P = Pre qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Revision of Silicon
3 = Rev 3

Fab Revision ID
F = ATMC

Figure 1. MPC5674F Orderable Part Number Description

Table 1. Orderable Part Numbers

Freescale Part Number	Package Description	Speed (MHz)[1]		Operating Temperature[2]	
		Nominal	Max[3] (f_{MAX})	Min (T_L)	Max (T_H)
SPC5673FF3MVR3	416 PBGA, no EBI, Pb-free	264	270	–40 °C	125 °C
SPC5673FF3MVY3	516 PBGA, w/EBI, Pb-free	264	270	–40 °C	125 °C
SPC5673FF3MVV2	516 PBGA, w/EBI, SnPb	264	270	–40 °C	125 °C
SPC5674FF3MVR3	416 PBGA, no EBI, Pb-free	264	270	–40 °C	125 °C
SPC5673FF3MVY2	516 PBGA, w/EBI, Pb-free	200	200	–40 °C	125 °C
SPC5674FF3MVY3	516 PBGA, w/EBI, Pb-free	264	270	–40 °C	125 °C
SPC5674FF3MVV3	516 PBGA, w/EBI, SnPb	264	270	–40 °C	125 °C
SPC5674FF3MVZ2	324 PBGA, no EBI, Pb-free	200	200	–40 °C	125 °C

1 For the operating mode frequency of various blocks on the device, see Table 27.

2 The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

3 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system clock + 2% FM.

MPC5674F 416-ball TEPBGA
(as viewed from top through the package)
(4 of 4)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
P	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V										ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W										REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y										ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA										VDD33_3	ETPUB30	VDDREG	VSSSYN	AA
AB										VDD	ETPUB31	VSSFL	EXTAL	AB
AC	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 10. MPC5674F 416-ball TEPBGA (4 of 4)

3.3 516-ball TEPBGA Pin Assignments

Figure 11 shows the 516-ball TEPBGA pin assignments in one figure. The same information is shown split into four quadrants in Figure 12 through Figure 15.

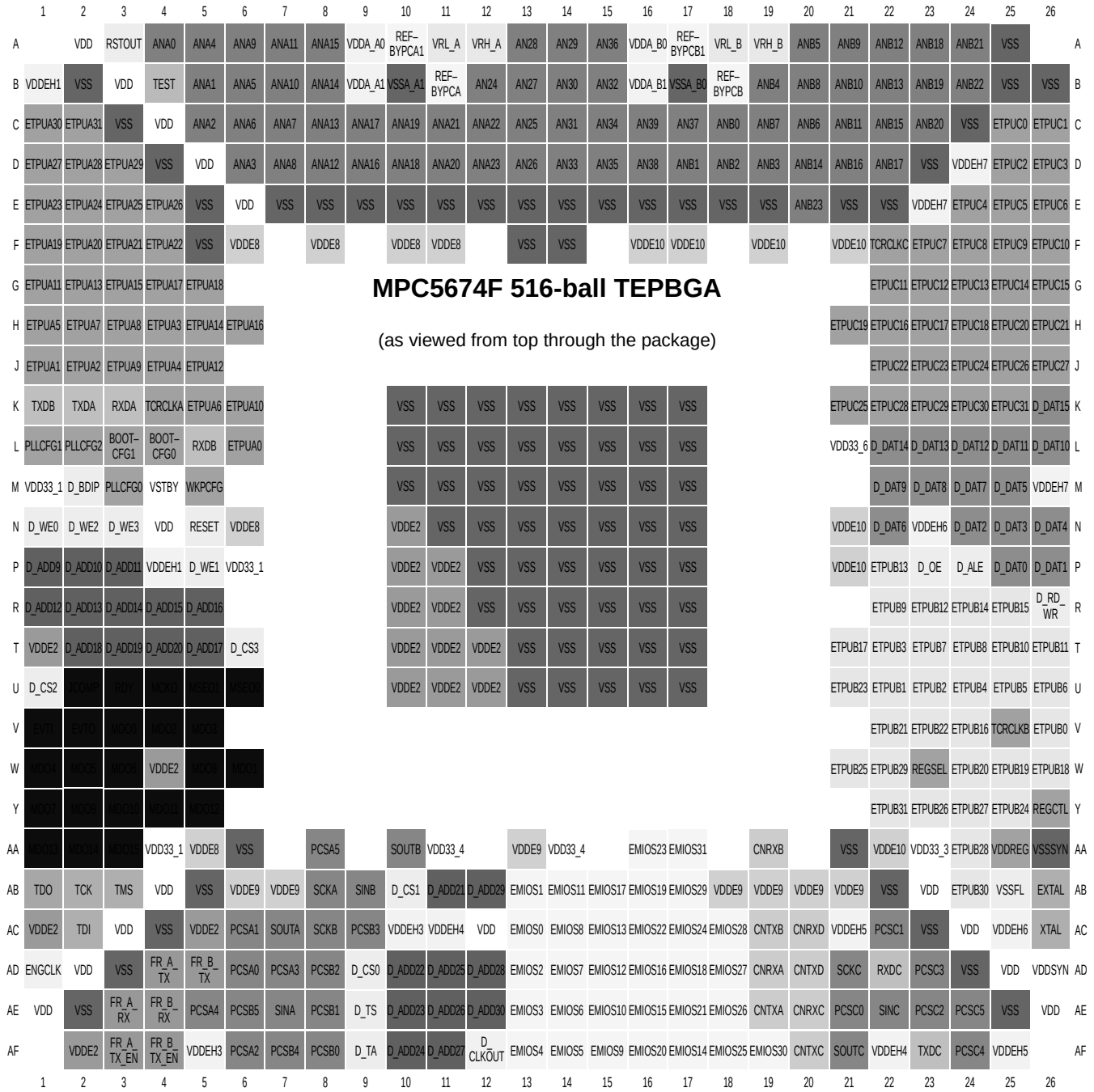


Figure 11. MPC5674F 516-ball TEPBGA (full diagram)

3.4 Signal Properties and Muxing

See Appendix A, Signal Properties and Muxing, for a listing and description of the pin functions and properties.

Table 5. Thermal Characteristics, 516-pin TEPBGA Package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	25	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	18	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	20	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	15	°C/W
Junction to Board [5]	$R_{\theta JB}$	10	°C/W
Junction to Case [6]	$R_{\theta JC}$	6	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 6. Thermal Characteristics, 324-pin Package[1]

MPC5674F Thermal Characteristic	Symbol	Value	Unit
Junction to ambient [2, 3], natural convection (one-layer board)	$R_{\theta JA}$	29	°C/W
Junction to ambient [1, 4], natural convection (four-layer board 2s2p)	$R_{\theta JA}$	19	°C/W
Junction to ambient (@200 ft./min., one-layer board)	$R_{\theta JMA}$	23	°C/W
Junction to ambient (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	16	°C/W
Junction to board [5] (four-layer board 2s2p)	$R_{\theta JB}$	10	°C/W
Junction to case [6]	$R_{\theta JC}$	7	°C/W
Junction to package top [7], natural convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

Table 11. PMC Electrical Specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
12c	—	LVD VDDREG Hysteresis (LDO3V / LDO5V mode)	—	30	—	mV
12d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (LDO3V / LDO5V mode)	—	30	—	mV
13	V_{LVDREG}	Nominal rising LVD VDDREG (SMPS5V mode)	—	4.360	—	V
13a	—	Untrimmed LVD VDDREG variation before band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	V
13b	—	Trimmed LVD VDDREG variation after band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	V
13c	—	LVD VDDREG Hysteresis (SMPS5V mode)	—	50	—	mV
13d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (SMPS5V mode)	—	50	—	mV
14	V_{LVDA}	Nominal rising LVD VDDA	—	4.60	—	V
14a	—	Untrimmed LVD VDDA variation before band gap trim	V_{LVDA} – 5%	V_{LVDA}	V_{LVDA} + 5%	V
14b	—	Trimmed LVD VDDA variation after band gap trim	V_{LVDA} – 3%	V_{LVDA}	V_{LVDA} + 3%	V
14c	—	LVD VDDA Hysteresis	—	150	—	mV
14d	$V_{LVDASTEP}$	Trimming step LVD VDDA	—	20	—	mV
15	—	SMPS regulator output resistance **Note:** Pulup to VDDREG when high, pulldown to VSSREG when low.	—	15	25	Ohm
16	—	SMPS regulator clock frequency (after reset)	1.0	1.5	2.4	MHz
17	—	SMPS regulator overshoot at start-up[2]	—	1.32	1.4	V
18	—	SMPS maximum output current	—	1.0	—	A
19	—	Voltage variation on current step[2] (20% to 80% of maximum current with 4 usec constant time)	—	—	0.1	V

1 VRC linear regulator is capable of sourcing a current up to 20 mA and sinking a current up to 500 μA. When using the recommended ballast transistor the maximum output current provided by the voltage regulator VRC/ballast to the VDD core voltage is up to 1A.

2 Parameter cannot be tested; this value is based on simulation and characterization.

[10] I_{OH_F} = {16,32,47,77} mA and I_{OL_F} = {24,48,71,115} mA for {00,01,10,11} drive mode with V_{DDE} = 3.0 V. This spec is for characterization only.

[11] I_{OH_S} = {11.6} mA and IOL_S = {17.7} mA for {medium} I/O with V_{DDE} = 4.5 V;
I_{OH_S} = {5.4} mA and IOL_S = {8.1} mA for {medium} I/O with V_{DDE} = 3.0 V. These specs are for characterization only.

[12] Applies to D_CLKOUT, external bus pins, and Nexus pins.

[13] V_{STBY} current specified at 1.0 V at a junction temperature of 85 ^{o}C. V_{STBY} current is 700 µA maximum at a junction temperature of 150 ^{o}C.

[14] Power requirements for the V_{DD33} supply depend on the frequency of operation and load of all I/O pins, and the voltages on the I/O segments.

[15] This value is a target that is subject to change.

[16] This value allows a 5 V reference to supply ADC + REF.

[17] Power requirements for each I/O segment depend on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Section 4.7.1, “I/O Pad Current Specifications,” for information on I/O pad power. Also refer to Table 15 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[18] Absolute value of current, measured at V_{IL} and V_{IH}.

[19] Absolute value of current, measured at V_{IL} and V_{IH}.

[20] Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types F and MH.

[21] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types AE and AE/up-down. See Appendix A, Signal Properties and Muxing.

[22] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics

[23] Pull-up and pull-down resistances are both enabled and settings are equal.

4.7.1 I/O Pad Current Specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 15 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 15.

The AC timing of these pads are described in the Section 4.11.2, “Pad AC Specifications.”

Table 15. V_{DDE}/V_{DDEH} I/O Pad Average DC Current[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive/Slew Rate Select	Current (mA)
1	Medium	I_{DRV_MH}	50	50	5.25	11	16.0
2			20	50	5.25	01	6.3
3			3.0	50	5.25	00	1.1
4			2.0	200	5.25	00	2.4
5	Fast	I_{DRV_FC}	66	10	3.6	00	7.4
6			66	20	3.6	01	10.5
7			66	30	3.6	10	12.3
8			66	50	3.6	11	35.2

Table 15. V_{DDE}/V_{DDEH} I/O Pad Average DC Current[1] (continued)

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive/Slew Rate Select	Current (mA)
9	Fast w/ Slew Control	I_{DRV_FSR}	66	50	3.6	11	12.7
10			50	50	3.6	10	6.7
11			33.33	50	3.6	01	4.2
12			20	50	3.6	00	2.6
13			20	200	3.6	00	9.1

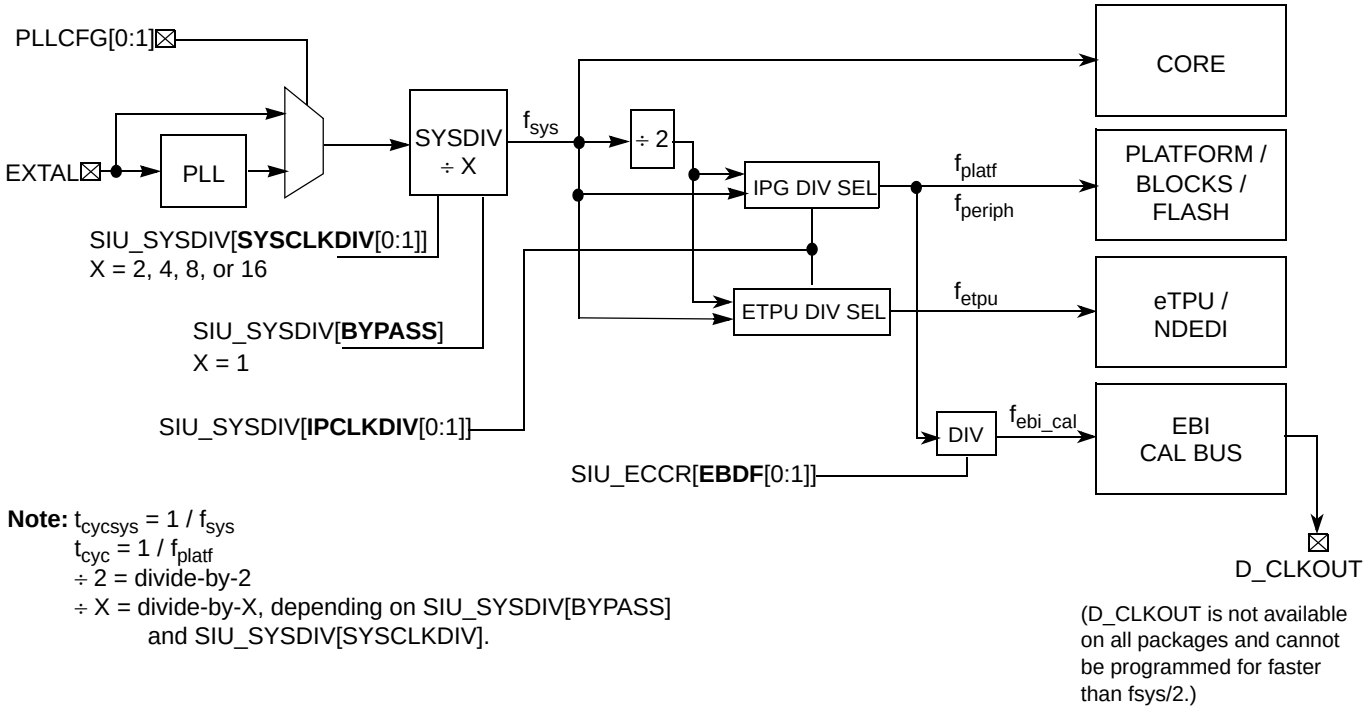
1 These are average IDDE numbers for worst case PVT from simulation. Currents apply to output pins only.

2 All loads are lumped.

4.11 AC Specifications

4.11.1 Clocking

The Figure 16 shows the operating frequency domains of various blocks on MPC5674F.



Note: $t_{cycsys} = 1 / f_{sys}$
$t_{cyc} = 1 / f_{platf}$
÷ 2 = divide-by-2
÷ X = divide-by-X, depending on SIU_SYSDIV[BYPASS] and SIU_SYSDIV[SYSCLKDIV].

Figure 16. MPC5674F Block Operating Frequency Domain Diagram

Table 27 shows the operating frequencies of various blocks depending on the device's clocking mode configuration settings (see Table 28 and Table 29 for descriptions of bit settings).

Table 27. MPC5674F Operating Frequencies[1, 2]

Mode	SIU_ECCR [EBDF[0:1]][3]	f_{sys} (core)	f_{platf} (platform and all blocks except eTPU)	f_{etpu} (eTPU, eTPU RAM, and NDEDI)	f_{ebi_cal}[4,5]	Unit
Enhanced	01 11	264 264	132 132	132 132	66 33	MHz
Full	01 11	200 200	100 100	200 200	50 25	MHz
Legacy	01 11	132 132	132 132	132 132	66 33	MHz

1 The values in the table are specified at:
V_{DD} = 1.02 V to 1.32 V
V_{DDE} = 3.0 V to 3.6 V
V_{DDEH} = 4.5 V to 5.5 V
V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V
$T_A = T_L$ to T_H.

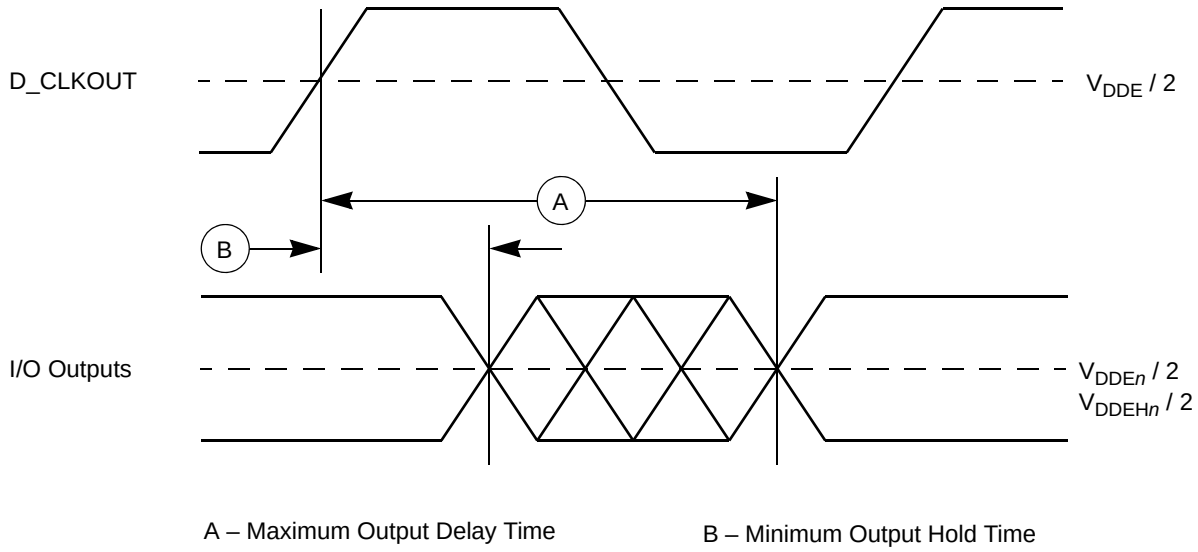


Figure 18. Generic Output Delay/Hold Timing

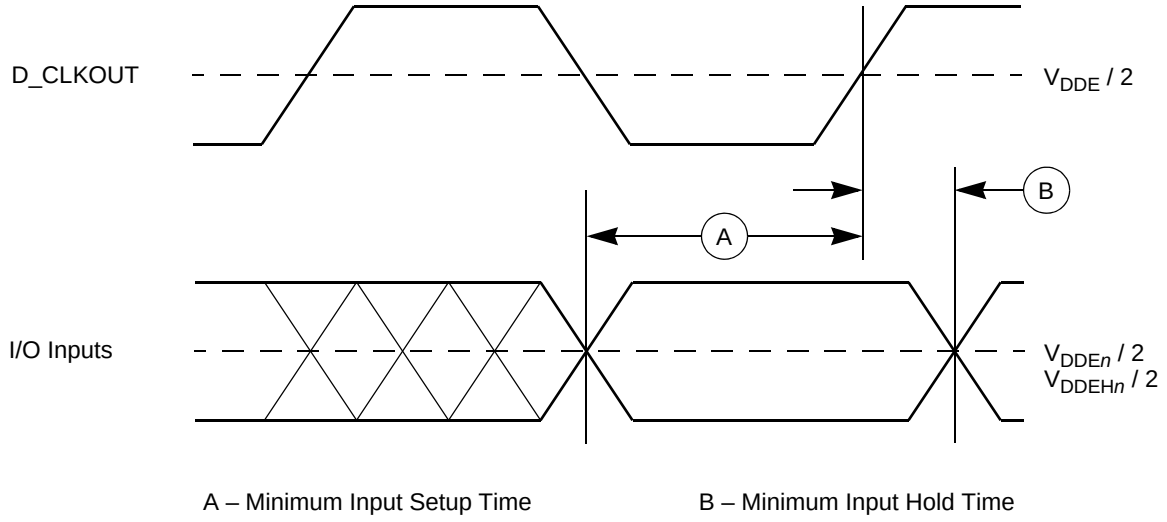


Figure 19. Generic Input Setup/Hold Timing

4.12.2 Reset and Configuration Pin Timing

Table 32. Reset and Configuration Pin Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

[1] Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, $T_A = T_L$ to T_H.

[2] See Notes on t_{cyc} on Figure 16 and Table 27 in Section 4.11.1, “Clocking.”

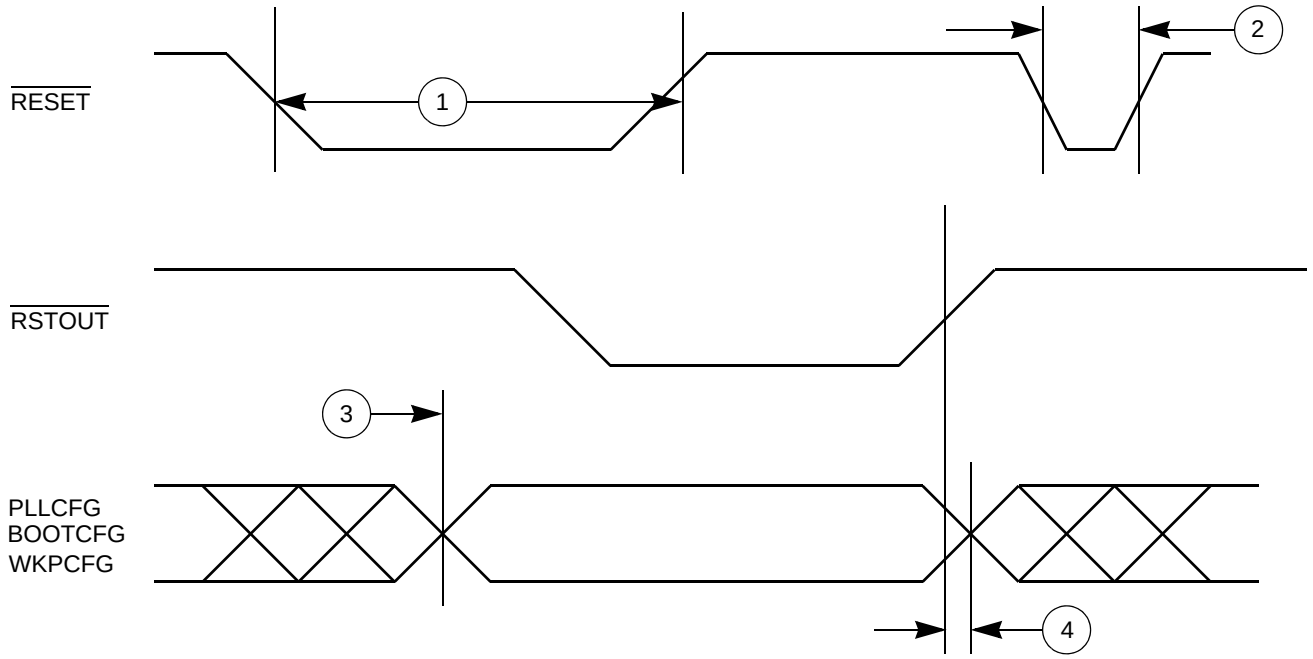


Figure 20. Reset and Configuration Pin Timing

4.12.3 IEEE 1149.1 Interface Timing

Table 33. JTAG Pin AC Electrical Characteristics[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at V_{DDE} / 2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40%–70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	10	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

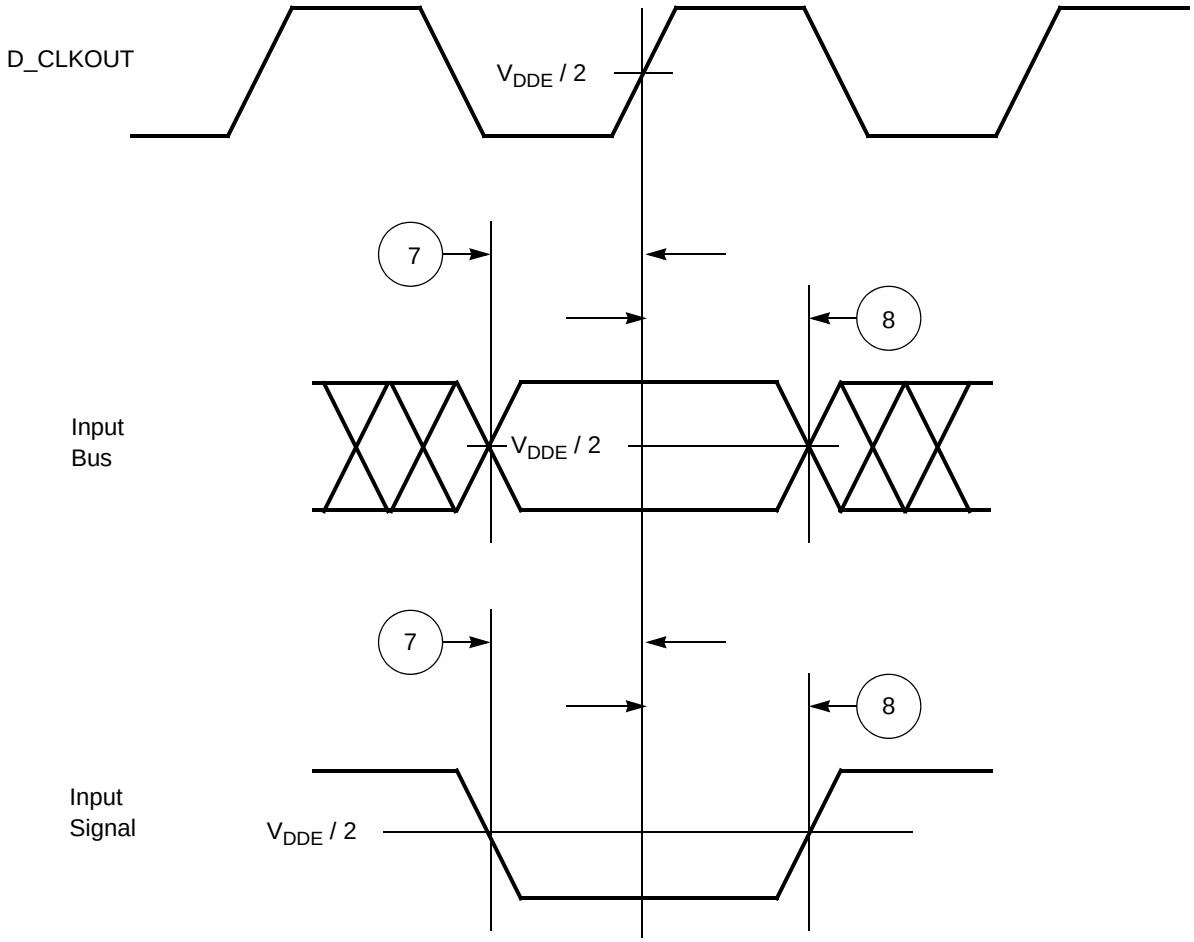


Figure 29. Synchronous Input Timing

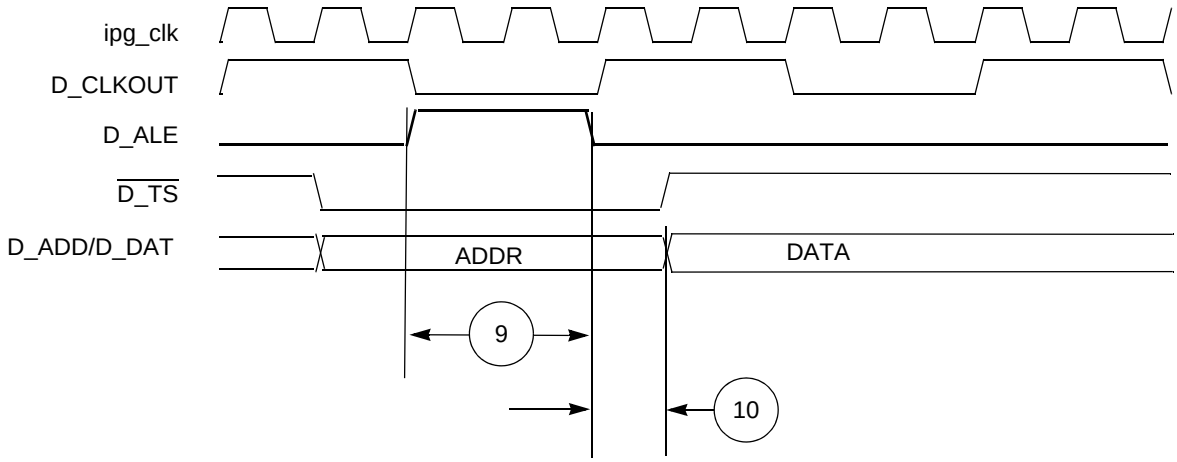


Figure 30. ALE Signal Timing

Table 39. DSPI Timing[1] [2] (continued)

Spec	Characteristic	Symbol	Peripheral Bus Freq: 132 MHz		Unit
			Min	Max	
9	Data Setup Time for Inputs	t_{SUI}			
	Master (MTFE = 0)		20	—	ns
	Slave		4	—	ns
	Master (MTFE = 1, CPHA = 0)[8]		6	—	ns
	Master (MTFE = 1, CPHA = 1)		20	—	ns
10	Data Hold Time for Inputs	t_{HI}			
	Master (MTFE = 0)		–3	—	ns
	Slave		7	—	ns
	Master (MTFE = 1, CPHA = 0)[8]		12	—	ns
	Master (MTFE = 1, CPHA = 1)		–3	—	ns
11	Data Valid (after SCK edge)	t_{SUO}			
	Master (MTFE = 0)		—	5	ns
	Slave		—	25	ns
	Master (MTFE = 1, CPHA = 0)		—	13	ns
	Master (MTFE = 1, CPHA = 1)		—	5	ns
12	Data Hold Time for Outputs	t_{HO}			
	Master (MTFE = 0)		–5	—	ns
	Slave		2.5	—	ns
	Master (MTFE = 1, CPHA = 0)		3	—	ns
	Master (MTFE = 1, CPHA = 1)		–5	—	ns

1 DSPI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, and $T_A = T_L$ to T_H

2 Speed is the nominal maximum frequency of platform clock (f_{platf}). Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 Mhz for system core clock (f_{sys}) + 2% FM.

3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTAR*n*[PSSCK] and DSPI_CTAR*n*[CSSCK].

6 The maximum value is programmable in DSPI_CTAR*n*[PASC] and DSPI_CTAR*n*[ASC].

7 For example, external master should start SCK clock not earlier than 3 system clock periods after assertion SS

8 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

The DSPI in this device can be configured to serialize data to an external device that implements the Microsecond Bus protocol. DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) for data and clock signals to improve high speed operation.

Table 40. DSPI LVDS Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit
LVDS Clock to Data/Chip Select Outputs	$t_{LVDSDATA}$	–0.25 × t_{SCYC}	+0.25 × t_{SCYC}	ns

1 These are typical values that are estimated from simulation.

2 See DSPI LVDS Pad related data in Table 16.

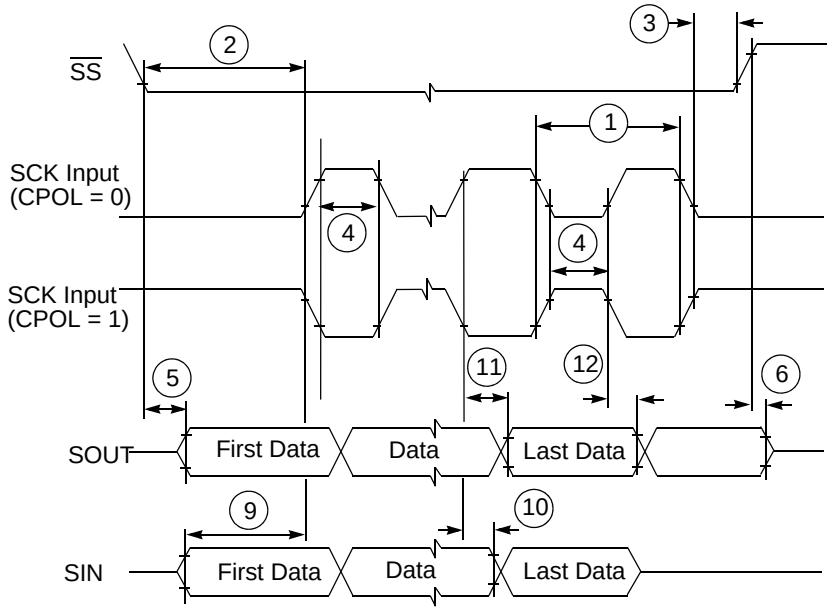


Figure 40. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

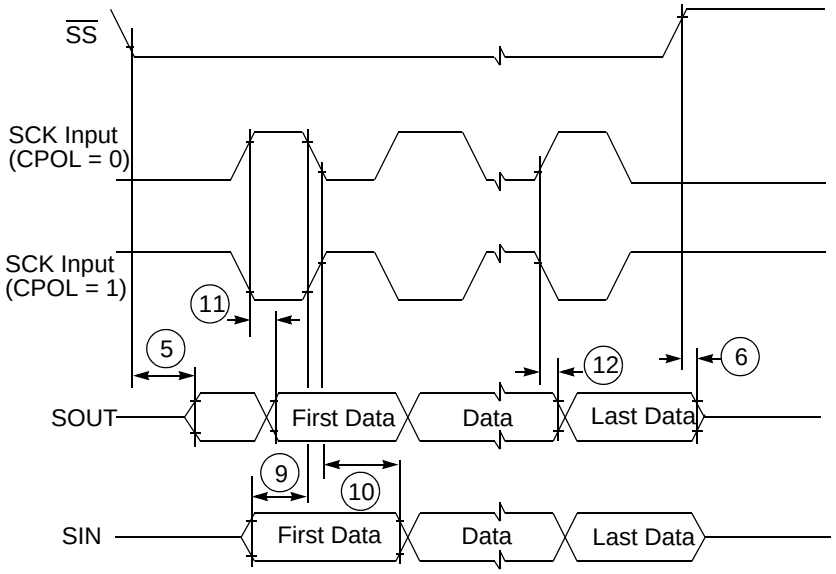


Figure 41. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

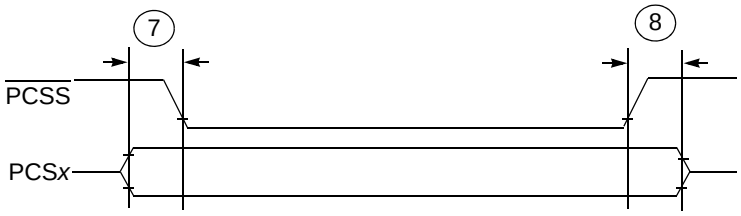


Figure 42. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
125	ETPUA11_ETPUA23_ GPIO125	P	ETPUA11	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G2	H1	G1
		A1	ETPUA23	eTPU A channel (output only)	O							
		A2	—	—	—							
		G	GPIO125	GPIO	I/O							
126	ETPUA12_PCSB1_ GPIO126	P	ETPUA12	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G3	H2	J5
		A1	PCSB1	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO126	GPIO	I/O							
127	ETPUA13_PCSB3_ GPIO127	P	ETPUA13	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F1	H4	G2
		A1	PCSB3	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO127	GPIO	I/O							
128	ETPUA14_PCSB4_ GPIO128	P	ETPUA14	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F2	H3	H5
		A1	PCSB4	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO128	GPIO	I/O							
129	ETPUA15_PCSB5_ GPIO129	P	ETPUA15	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F3	G1	G3
		A1	PCSB5	DSPI B peripheral chip select	O							
		A2	—	—	—							
		G	GPIO129	GPIO	I/O							
130	ETPUA16_PCSD1_ GPIO130	P	ETPUA16	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H4	G2	H6
		A1	PCSD1	DSPI D peripheral chip select	O							
		A2	—	—	—							
		G	GPIO130	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
143	ETPUA29_PCSC2_ GPIO143	P	ETPUA29	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	—	D3	D3
		A1	PCSC2	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO143	GPIO	I/O							
144	ETPUA30_PCSC3_ GPIO144	P	ETPUA30	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E4	C1	C1
		A1	PCSC3	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO144	GPIO	I/O							
145	ETPUA31_PCSC4_ GPIO145	P	ETPUA31	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D3	C2	C2
		A1	PCSC4	DSPI C peripheral chip select	O							
		A2	—	—	—							
		G	GPIO145	GPIO	I/O							
eTPU_B												
146	TCRCLKB_IRQ6_ GPIO146	P	TCRCLKB	eTPU B TCR clock	I	MH	V_{DDEH6}	—/Up	—/Up	P19	T23	V25
		A1	IRQ6	External interrupt request	I							
		A2	—	—	—							
		G	GPIO146	GPIO	I/O							
147	ETPUB0_ETPUB16_ GPIO147	P	ETPUB0	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	N19	T24	V26
		A1	ETPUB16	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO147	GPIO	I/O							
148	ETPUB1_ETPUB17_ GPIO148	P	ETPUB1	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R19	T25	U22
		A1	ETPUB17	eTPU B channel (output only)	O							
		A2	—	—	—							
		G	GPIO148	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
452	ETPUC11_IRQ2_ GPIO452[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	E21	G23	G22
		A1	IRQ2	External interrupt request	I							
		A2	—	—	—							
		G	GPIO452	GPIO	I/O							
453	ETPUC12_IRQ3_ GPIO453[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F19	G24	G23
		A1	IRQ3	External interrupt request	I							
		A2	—	—	—							
		G	GPIO453	GPIO	I/O							
454	ETPUC13_3_IRQ4_ GPIO454[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F21	G25	G24
		A1	IRQ4	External interrupt request	I							
		A2	—	—	—							
		G	GPIO454	GPIO	I/O							
455	ETPUC14_4_IRQ5_ GPIO455[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F20	G26	G25
		A1	IRQ5	External interrupt request	I							
		A2	—	—	—							
		G	GPIO455	GPIO	I/O							
456	ETPUC15__ GPIO456[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	—	H23	G26
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO456	GPIO	I/O							
457	ETPUC16_FR_A_TX_ GPIO457[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	—	H24	H22
		A1	FR_A_TX	FlexRay A transfer	O							
		A2	—	—	—							
		G	GPIO457	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
470	ETPUC29_SCKD_ GPIO470[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K21	L25	K23
		A1	SCKD	DSPI D clock	I/O							
		A2	—	—	—							
		G	GPIO470	GPIO	I/O							
471	ETPUC30_SOUTD_ GPIO471[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K20	L26	K24
		A1	SOUTD	DSPI D data output	O							
		A2	—	—	—							
		G	GPIO471	GPIO	I/O							
472	ETPUC31_SIND_ GPIO472[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K19	M23	K25
		A1	SIND	DSPI D data input	I							
		A2	—	—	—							
		G	GPIO472	GPIO	I/O							
eMIOS												
179	EMIOS0_ETPUA0_ GPIO179	P	EMIOS0	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AA9	AE10	AC13
		A1	ETPUA0	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO179	GPIO	I/O							
180	EMIOS1_ETPUA1_ GPIO180	P	EMIOS1	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AB9	AF10	AB13
		A1	ETPUA1	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO180	GPIO	I/O							
181	EMIOS2_ETPUA2_ GPIO181	P	EMIOS2	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	Y10	AD11	AD13
		A1	ETPUA2	eTPU A channel	O							
		A2	—	—	—							
		G	GPIO181	GPIO	I/O							

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
—	ANA3	P	ANA3[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA3	ANA3	B6	D6	D6
—	ANA4	P	ANA4[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA4	ANA4	A6	A5	A5
—	ANA5	P	ANA5[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA5	ANA5	A7	B6	B6
—	ANA6	P	ANA6[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA6	ANA6	B7	C6	C6
—	ANA7	P	ANA7[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA7	ANA7	B8	D7	C7
—	ANA8	P	ANA8	eQADC A analog input	I	AE	V_{DDA_A1}	ANA8	ANA8	C5	A6	D7
—	ANA9	P	ANA9	eQADC A analog input	I	AE	V_{DDA_A1}	ANA9	ANA9	C7	C7	A6
—	ANA10	P	ANA10	eQADC A analog input	I	AE	V_{DDA_A1}	ANA10	ANA10	C6	B7	B7
—	ANA11	P	ANA11	eQADC A analog input	I	AE	V_{DDA_A1}	ANA11	ANA11	D6	A7	A7
—	ANA12	P	ANA12	eQADC A analog input	I	AE	V_{DDA_A1}	ANA12	ANA12	D7	D8	D8
—	ANA13	P	ANA13	eQADC A analog input	I	AE	V_{DDA_A1}	ANA13	ANA13	C8	C8	C8
—	ANA14	P	ANA14	eQADC A analog input	I	AE	V_{DDA_A1}	ANA14	ANA14	D8	B8	B8
—	ANA15	P	ANA15	eQADC A analog input	I	AE	V_{DDA_A1}	ANA15	ANA15	A8	A8	A8
—	ANA16	P	ANA16	eQADC A analog input	I	AE	V_{DDA_A1}	ANA16	ANA16	D9	D9	D9
—	ANA17	P	ANA17	eQADC A analog input	I	AE	V_{DDA_A1}	ANA17	ANA17	C9	C9	C9
—	ANA18	P	ANA18	eQADC A analog input	I	AE	V_{DDA_A1}	ANA18	ANA18	D10	D10	D10
—	ANA19	P	ANA19	eQADC A analog input	I	AE	V_{DDA_A1}	ANA19	ANA19	C10	C10	C10
—	ANA20	P	ANA20	eQADC A analog input	I	AE	V_{DDA_A1}	ANA20	ANA20	D11	D11	D11
—	ANA21	P	ANA21	eQADC A analog input	I	AE	V_{DDA_A1}	ANA21	ANA21	C11	C11	C11
—	ANA22	P	ANA22	eQADC A analog input	I	AE	V_{DDA_A1}	ANA22	ANA22	D12	D12	C12
—	ANA23	P	ANA23	eQADC A analog input	I	AE	V_{DDA_A1}	ANA23	ANA23	C12	C12	D12
—	AN24	P	AN24	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN24	AN24	—	B12	B12
—	AN25	P	AN25	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN25	AN25	—	D13	C13
—	AN26	P	AN26	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN26	AN26	—	C13	D13

Table 42. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location		
										324	416	516
283	D_ADD_DAT5_ GPIO283	P	D_ADD_DAT5	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M25
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO283	GPIO	I/O							
284	D_ADD_DAT6_ GPIO284	P	D_ADD_DAT6	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	N22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO284	GPIO	I/O							
285	D_ADD_DAT7_ GPIO285	P	D_ADD_DAT7	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M24
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO285	GPIO	I/O							
286	D_ADD_DAT8_ GPIO286	P	D_ADD_DAT8	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M23
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO286	GPIO	I/O							
287	D_ADD_DAT9_ GPIO287	P	D_ADD_DAT9	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	—	M22
		A1	—	—	—							
		A2	—	—	—							
		G	GPIO287	GPIO	I/O							