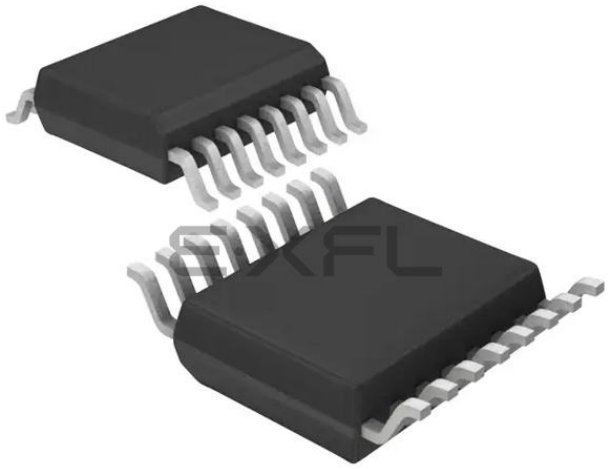
Renesas Electronics America Inc - UPD78F0550MA-FAA-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	9
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0550ma-faa-ax

<R> **Table 2-4. Pin I/O Circuit Types (78K0/KA2-L (25-pin and 32-pin products))**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 Note 1/TI000 Note 1/ INTP0 Note 1	5-AQ	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P01 Note 2/TO00 Note 2/ TI010 Note 2			
P02/$\overline{SSI11}$/INTP5			
ANI0/P20/AMP0- Note 3	11-P		<Digital input setting> Independently connect to AV_{REF} or V_{SS} via a resistor. <Digital output setting and analog input setting > Leave open. Note 4
ANI1/P21/AMP0OUT Note 3/ PGAIN Note 3	11-O		
ANI2/P22/AMP0+ Note 3	11-N		
ANI3/P23 to ANI6/P26	11-G		
ANI7/P27 Note 2			
P31/INTP2/TOOLC1	5-AQ		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P32/TOH1/INTP3/TOOLD1			
P33			
P34/INTP4 (/TOH1)(/TI51) Note 1			
P35/$\overline{SCK11}$			
P36/SI11			
P37/SO11			
P60/SCLA0/TxD6	5-AS		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave this pin open at low-level output after clearing the output latch of the port to 0.
P61/SDAA0/RxD6			
ANI8 Note 2/P70 Note 2	11-G		<Digital input setting> Independently connect to AV_{REF} or V_{SS} via a resistor. <Digital output setting and analog input setting > Leave open. Note 4
ANI9 Note 2/P71 Note 2			
ANI10 Note 2/P72 Note 2			
P121/X1/TOOLC0 Note 5 (/TI000)(/INTP0)	37-A	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P122/X2/EXCLK/ TOOLD0 Note 5			
$\overline{RESET}$/P125 (/TI000) Note 2 (/INTP0) Note 2	42-A		Connect directly to V_{DD} or via a resistor.
AV_{REF}	–	–	Connect directly to V_{DD}.

Notes 1. 25-pin products only

2. 32-pin products only

3. μPD78F0565, 78F0566, and 78F0567 (products with operational amplifier) only

4. If this pin is left open when specified as an analog input pin, the input voltage level might become undefined. It is therefore recommended to leave this pin open after specifying it as a digital output pin.

5. Use recommended connection above in input port mode (refer to **Figure 5-3 Format of Clock Operation Mode Select Register (OSCCTL)**) when these pins are not used.

Cautions 1. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, ANI3/P23 to ANI5/P25, and ANI8/P70 to ANI10/P72 are set in the analog input mode after release of reset.

2. Because $\overline{RESET}$/P125 is set in the external reset input immediately after release of reset, if a reset signal is generated during low level input, the reset status continues until the input rises to the high level.

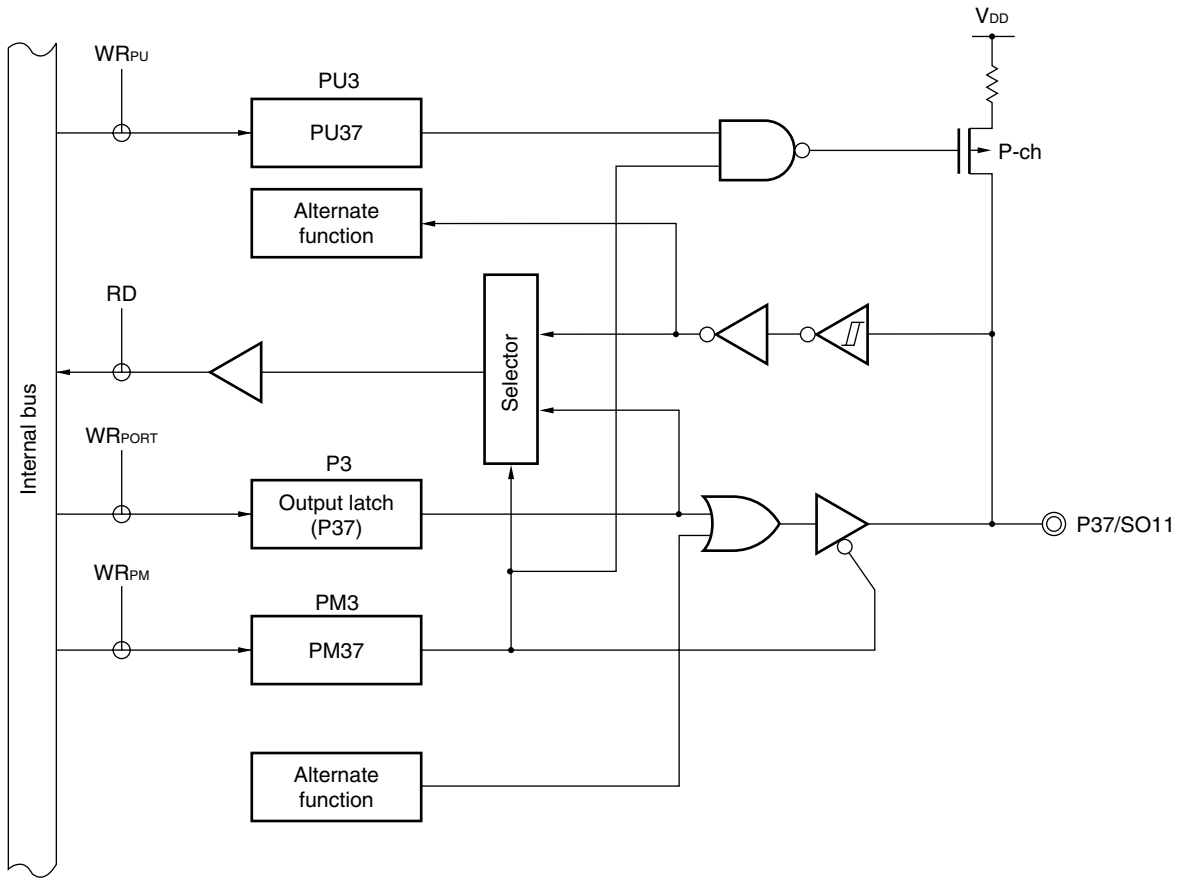
<R> **Table 3-8. Special Function Register List: 78K0/KA2-L (25-pin and 32-pin products) (5/5)**

Address	Symbol		Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
			7	6	5	4	3	2	1	0		1	8	16		
FFC0H to FFDFH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFE0H	IF0	IF0L	<SREIF6>	<PIF5>	<PIF4>	<PIF3>	<PIF2>	0	<PIF0>	<LVIIF>	R/W	√	√	√	00H	598
FFE1H		IF0H	<TMIF010>	<TMIF000>	0	0	<TMIFH1>	<CSIIF10>	<STIF6>	<SRIF6>	R/W	√	√		00H	598
FFE2H	IF1	IF1L	0	0	0	0	<TMIF51>	0	0	<ADIF>	R/W	√	√	√	00H	598
FFE3H		IF1H	0	0	0	0	0	0	0	<IICAIF0>	R/W	√	√		00H	598
FFE4H	MK0	MK0L	<SREMK6>	<PMK5>	<PMK4>	<PMK3>	<PMK2>	1	<PMK0>	<LVIMK>	R/W	√	√	√	FFH	606
FFE5H		MK0H	<TMMK010>	<TMMK000>	1	1	<TMMKH1>	<CSIMK10	<STMK6>	<SRMK6>	R/W	√	√		FFH	606
FFE6H	MK1	MK1L	1	1	1	1	<TMMK51>	1	1	<ADMK>	R/W	√	√	√	FFH	606
FFE7H		MK1H	1	1	1	1	1	1	1	<IICAMK0>	R/W	√	√		FFH	606
FFE8H	PR0	PR0L	<SREMK6>	<PPR5>	<PPR4>	<PPR3>	<PPR2>	1	<PPR0>	<LVIPR>	R/W	√	√	√	FFH	613
FFE9H		PR0H	<TMPR010>	<TMPR000>	1	1	<TMPRH1>	<CSIPR10>	<STPR6>	<SRPR6>	R/W	√	√		FFH	613
FFEAH	PR1	PR1L	1	1	1	1	<TMPR51>	1	1	<ADPR>	R/W	√	√	√	FFH	613
FFEBH		PR1H	1	1	1	1	1	1	1	<IICAPR0>	R/W	√	√		FFH	613
FFECH to FFEFH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFF0H	IMS		RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	R/W	–	√	–	CFH[Note]	699
FFF1H to FFFAH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFFBH	PCC		0	0	0	0	0	PCC2	PCC1	PCC0	R/W	√	√	–	01H	204

Note Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated in Table 3-1 after release of reset.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

Figure 4-17. Block Diagram of P37



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Table 4-15. Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KA2-L (20-pin products)) (2/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P121	X1[Note 1]	–	×	×
	TOOLC0	Input	×	×
P122	X2[Note 1]	–	×	×
	EXCLK[Note 1]	Input	×	×
	TOOLD0	I/O	×	×
P125	$\overline{\text{RESET}}$[Note 2]	Input	×	×

Notes 1. When using the P121 and P122 pins to connect a resonator for the main system clock (X1, X2) or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode or external clock input mode must be set by using OSCCTL register (for details, refer to **5.3 (1) Clock operation mode select register (OSCCTL)**). The reset value of OSCCTL is 00H (both P121 and P122 are input port pins).

2. Clear RSTM bit (bit 5 of RSTMASK register) to 0 when using P125 as an external reset input ($\overline{\text{RESET}}$).

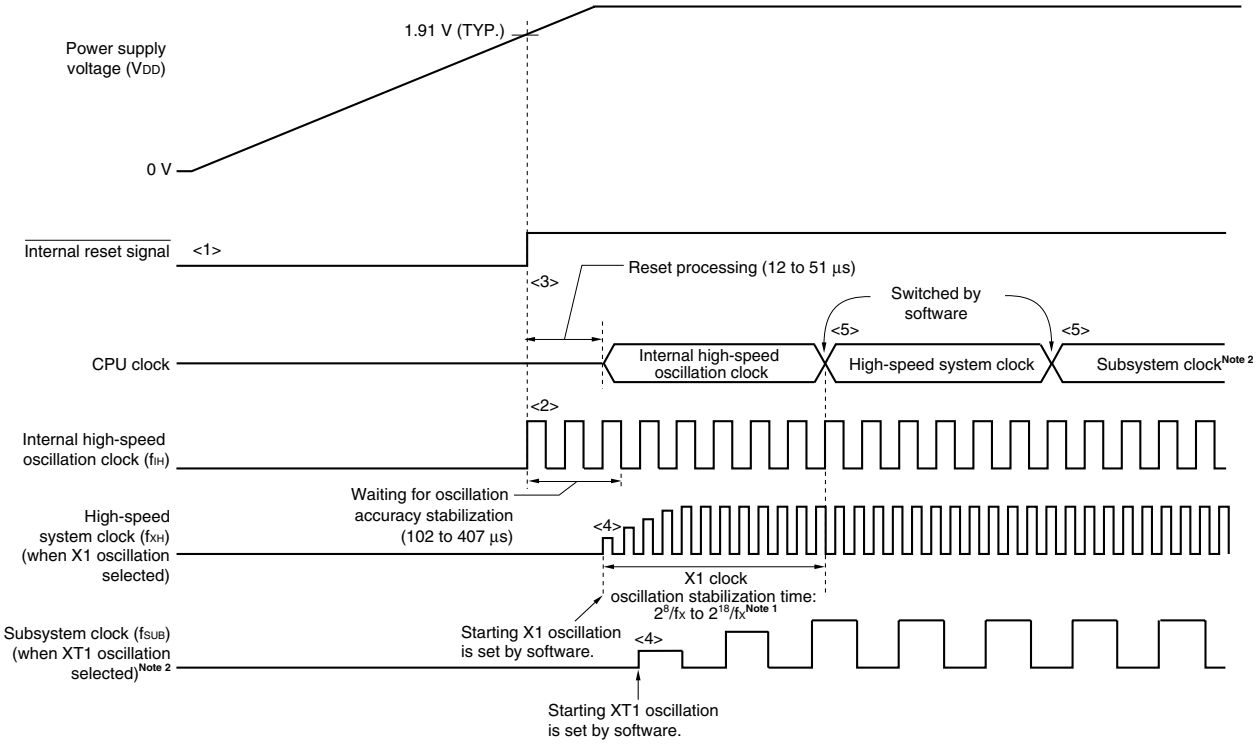
Remark ×: Don't care
PM××: Port mode register
P××: Port output latch

Cautions 1. If the voltage rises with a slope of less than 0.5 V/ms (MIN.) from power application until the voltage reaches 1.8 V, input a low level to the $\overline{\text{RESET}}$ pin from power application until the voltage reaches 1.8 V, or set the LVI default start function enabled by using the option byte (LVISTART = 1) (refer to Figure 5-17). When a low level has been input to the $\overline{\text{RESET}}$ pin until the voltage reaches 1.8 V, the CPU operates with the same timing as <2> and thereafter in Figure 5-16, after the reset has been released by the $\overline{\text{RESET}}$ pin.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK and EXCLKS pins is used.

Remark While the microcontroller is operating, a clock that is not used as the CPU clock can be stopped via software settings. The internal high-speed oscillation clock and high-speed system clock can be stopped by executing the STOP instruction (refer to **(4)** in **5.6.1 Example of controlling high-speed system clock**, **(3)** in **5.6.2 Example of controlling internal high-speed oscillation clock**, and **(4)** in **5.6.3 Example of controlling subsystem clock**).

Figure 5-17. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Enabled Is Set (Option Byte: LVISTART = 1))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 1.91 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

<3> After the reset is released and reset processing is performed, the CPU starts operation on the internal high-speed oscillation clock.

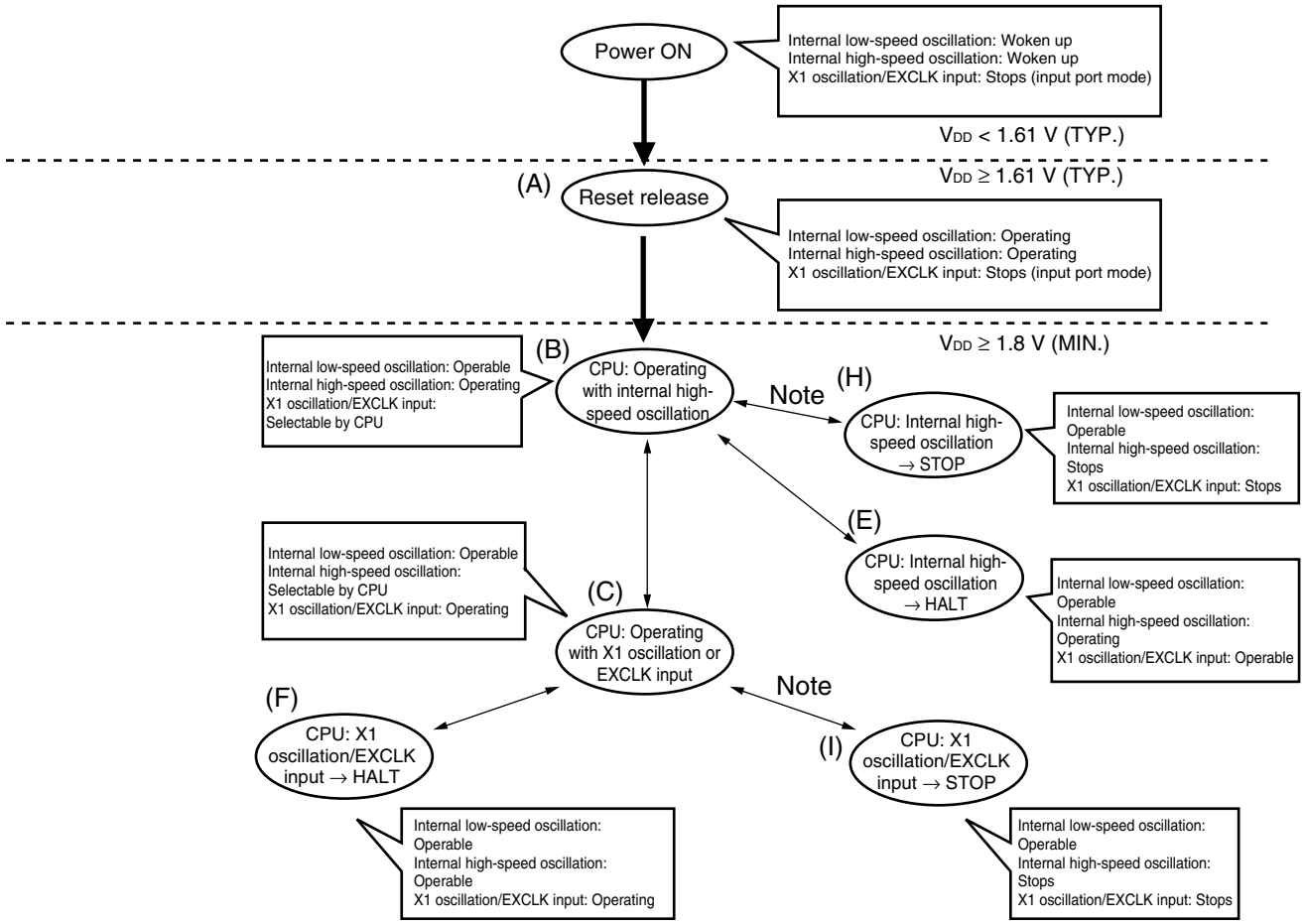
<4> Set the start of oscillation of the X1 or XT1 clock via software (refer to **(1)** in **5.6.1 Example of controlling high-speed system clock** and **(1)** in **5.6.3 Example of controlling subsystem clock**).

<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (refer to **(3)** in **5.6.1 Example of controlling high-speed system clock** and **(3)** in **5.6.3 Example of controlling subsystem clock**).

5.6.6 CPU clock status transition diagram

Figures 5-18 and 5-19 show the CPU clock status transition diagram of this product.

Figure 5-18. CPU Clock Status Transition Diagram (When LVI Default Start Mode Function Stopped Is Set (Option Byte: LVISTART = 0), 78K0/KY2-L, 78K0/KA2-L, and 78K0/KB2-L)



<R> **Note** When transitioning to the STOP mode, it is possible to achieve low power consumption by setting RMC = 56H first.

Remark When LVI default start function enabled is set (option byte: LVISTART = 1), the CPU clock status changes to (A) in the above figure when the supply voltage exceeds 1.91 V (TYP.), and to (B) after reset processing (12 to 51 μs).

7.4.3 Square-wave output operation

A square wave with any selected frequency is output at intervals determined by the value preset to 8-bit timer compare register 5n (CR5n).

The TO5n pin output status is inverted at intervals determined by the count value preset to CR5n by setting bit 0 (TOE5n) of 8-bit timer mode control register 5n (TMC5n) to 1. This enables a square wave with any selected frequency to be output (duty = 50%).

Remark Square-wave output is operable only in the 78K0/KB2-L and 78K0/KC2-L.

Setting

<1> Set each register.

- Clear the port output latch (P17 or P33)[Note] and port mode register (PM17 or PM33)[Note] to 0.
- TCL5n: Select the count clock.
- CR5n: Compare value
- TMC5n: Stop the count operation, select the mode in which clear & start occurs on a match of TM5n and CR5n.

LVS5n	LVR5n	Timer Output F/F Status Setting
0	1	Timer output F/F clear (0) (default value of TO5n output: low level)
1	0	Timer output F/F set (1) (default value of TO5n output: high level)

Timer output enabled
(TMC5n = 00001011B or 00000111B)

<2> After TCE5n = 1 is set, the count operation starts.

<3> The timer output F/F is inverted by a match of TM5n and CR5n. After INTTM5n is generated, TM5n is cleared to 00H.

<4> After these settings, the timer output F/F is inverted at the same interval and a square wave is output from TO5n. The frequency is as follows.

- Frequency = 1/2t (N + 1)
  (N: 00H to FFH)

Note 8-bit timer/event counter 50: P17, PM17
8-bit timer/event counter 51: P33, PM33

Caution Do not write other values to CR5n during operation.

Remarks 1. For how to enable the INTTM5n signal interrupt, refer to **CHAPTER 17 INTERRUPT FUNCTIONS**.

2. 78K0/KB2-L, 78K0/KC2-L: n = 0, 1

(5) Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

ADS can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

<R> **Remark** A/D converter analog input pins differ depending on products.

- 78K0/KY2-L: ANI0 to ANI3
- 78K0/KA2-L (20-pin products): ANI0 to ANI5
- 78K0/KA2-L (25-pin products): ANI0 to ANI6
- 78K0/KA2-L (32-pin products): ANI0 to ANI10
- 78K0/KB2-L: ANI0 to ANI3, ANI8 to ANI10
- 78K0/KC2-L (40-pin product): ANI0 to ANI6, ANI8 to ANI10
- 78K0/KC2-L (44-pin and 48-pin products): ANI0 to ANI10

Figure 12-8. Format of Analog Input Channel Specification Register (ADS)

Address: FF0EH After reset: 00H R/W

Symbol	7	<6>	5	4	<3>	<2>	<1>	<0>
<R> ADS	0	ADOAS	0	0	ADS3	ADS2	ADS1	ADS0

ADOAS	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	ANI0	P20/ANI0 pin
0	0	0	0	1	ANI1	P21/ANI1 pin or operational amplifier 0 output signal[Note]
0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	1	0	1	ANI5	P25/ANI5 pin
0	0	1	1	0	ANI6	P26/ANI6 pin
0	0	1	1	1	ANI7	P27/ANI7 pin
0	1	0	0	0	ANI8	P10/ANI8 pin or P70/ANI8 pin
0	1	0	0	1	ANI9	P11/ANI9 pin or P71/ANI9 pin or operational amplifier 1 output signal[Note]
0	1	0	1	0	ANI10	P12/ANI10 pin or P72/ANI10 pin
1	×	×	×	×	PGAOUT[Note]	PGA output signal[Note]
Other than above					Setting prohibited	

Note Setting permitted in products with operational amplifier

Figure 15-5. Format of IICA Control Register 0 (IICACTL0) (1/4)

Address: FFA7H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICACTL0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

IICE0	I^2C operation enable
0	Stop operation. Reset the IICA status register 0 (IICAS0)[Note 1]. Stop internal operation.
1	Enable operation.
Be sure to set this bit (1) while the SCLA0 and SDLA0 lines are at high level.	
Condition for clearing (IICE0 = 0)	Condition for setting (IICE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

LREL0[Notes 2,3]	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCLA0 and SDAA0 lines are set to high impedance. The following flags of IICA control register 0 (IICACTL0) and IICA status register 0 (IICAS0) are cleared to 0. • STT0 • SPT0 • MSTS0 • EXC0 • COI0 • TRC0 • ACKD0 • STD0
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL0 = 0)	Condition for setting (LREL0 = 1)
• Automatically cleared after execution • Reset	• Set by instruction

WREL0[Notes 2,3]	Wait cancellation
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared after wait is canceled.
When WREL0 is set (wait canceled) during the wait period at the ninth clock pulse in the transmission status (TRC0 = 1), the SDAA0 line goes into the high impedance state (TRC0 = 0).	
Condition for clearing (WREL0 = 0)	Condition for setting (WREL0 = 1)
• Automatically cleared after execution • Reset	• Set by instruction

Notes 1. The IICAS0 register, the STCF and IICBSY bits of the IICAF0 register, and the CLD0 and DAD0 bits of the IICACTL1 register are reset.

2. The signals of these bits are invalid while the IICE0 bit is 0.

3. When the LREL0 and WREL0 bits are read, 0 is always read.

Caution If the operation of I^2C is enabled (IICE0 = 1) when the SCLA0 line is high level, the SDAA0 line is low level, and the digital filter is turned on (DFC0 of the IICACTL1 register = 1), a start condition will be inadvertently detected immediately. In this case, set (1) the LREL0 bit by using a 1-bit memory manipulation instruction immediately after enabling operation of I^2C (IICE0 = 1).

(4) IICA control register 1 (IICACTL1)

This register is used to set the operation mode of I^2C and detect the statuses of the SCLA0 and SDAA0 pins.

This register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the CLD0 and DAD0 bits are read-only.

Set the IICACTL1 register, except the WUP bit, while operation of I^2C is disabled (bit 7 (IICE0) of IICA control register 0 (IICACTL0) is 0).

Reset signal generation clears this register to 00H.

Figure 15-8. Format of IICA Control Register 1 (IICACTL1) (1/2)

Address: FFA8H After reset: 00H R/W[Note 1]

Symbol	7	6	<5>	<4>	<3>	<2>	1	0
IICACTL1	WUP	0	CLD0	DAD0	SMC0	DFC0	0	0

WUP	Control of address match wakeup
0	Stops operation of address match wakeup function in STOP mode.
1	Enables operation of address match wakeup function in STOP mode.

To shift to STOP mode when WUP = 1, execute the STOP instruction at least three clocks after setting (1) WUP bit (see **Figure 15-23 Flow When Setting WUP = 1**).
Clear (0) the WUP bit after the address has matched or an extension code has been received. The subsequent communication can be entered by clearing (0) the WUP bit (The wait must be released and transmit data must be written after the WUP bit has been cleared (0).).
The interrupt timing when the address has matched or when an extension code has been received, while WUP = 1, is identical to the interrupt timing when WUP = 0. (A delay of the difference of sampling by the clock will occur.) Furthermore, when WUP = 1, a stop condition interrupt is not generated even if the SPIE0 bit is set to 1.

Condition for clearing (WUP = 0)	Condition for setting (WUP = 1)
• Cleared by instruction (after address match or extension code reception)	• Set by instruction (when MSTS0, EXC0, and COI0 are “0”, and STD0 also “0” (communication not entered))[Note 2]

Notes 1. Bits 4 and 5 are read-only.

2. The status of IICAS0 must be checked and WUP must be set during the period shown below.

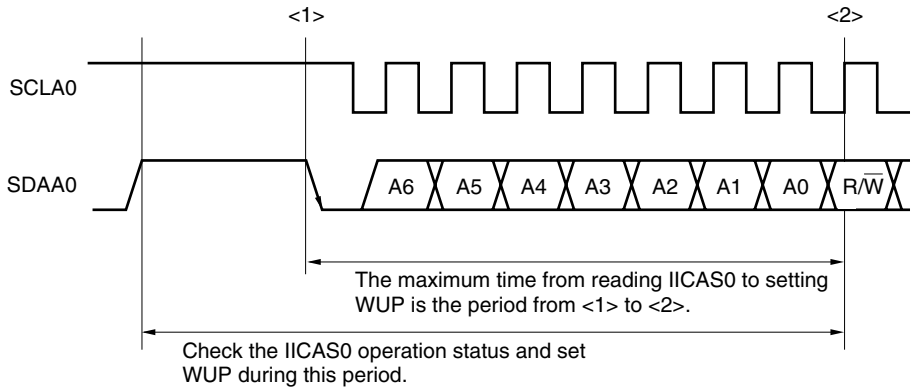
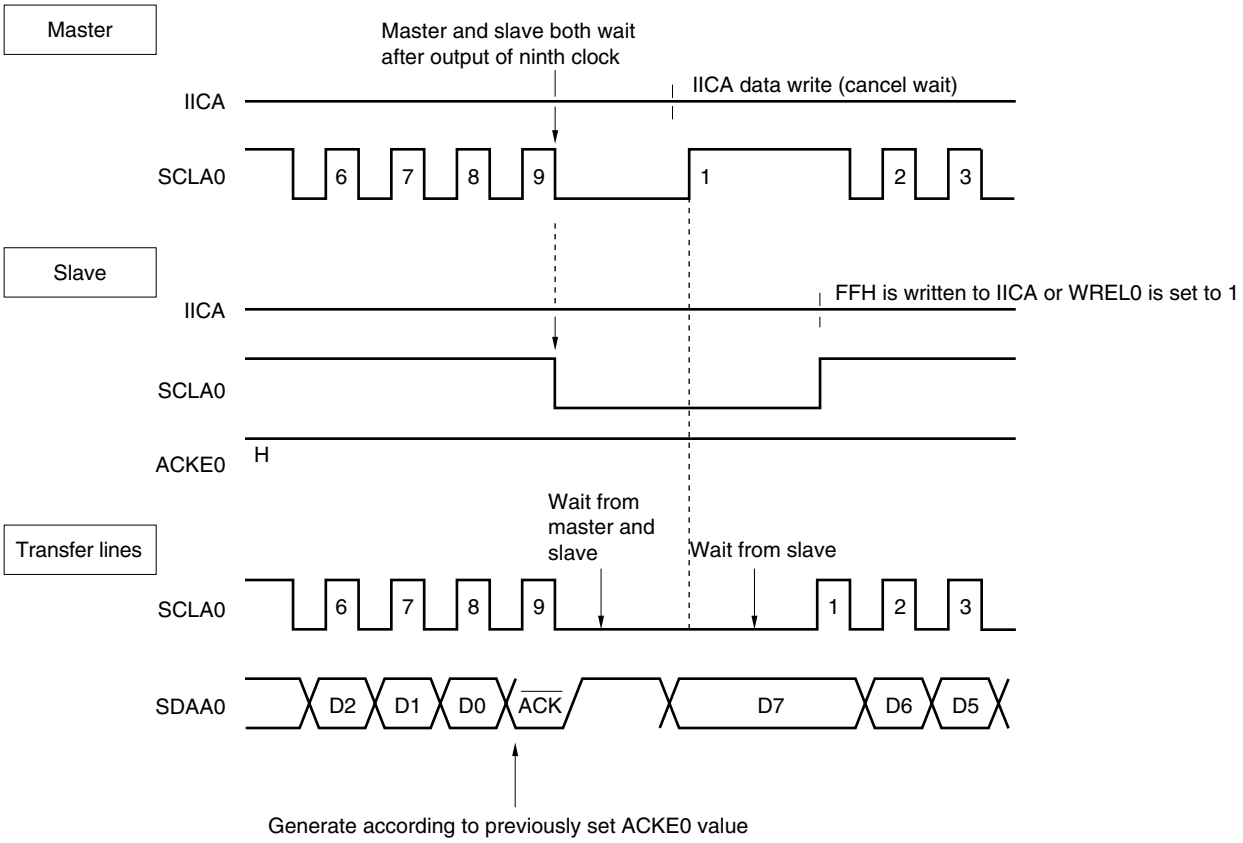


Figure 15-21. Wait (2/2)

(2) When master and slave devices both have a nine-clock wait (master transmits, slave receives, and ACKE0 = 1)



Remark ACKE0: Bit 2 of IICA control register 0 (IICACTL0)
WREL0: Bit 5 of IICA control register 0 (IICACTL0)

A wait may be automatically generated depending on the setting of bit 3 (WTIM0) of the IICA control register 0 (IICACTL0).

Normally, the receiving side cancels the wait state when bit 5 (WREL0) of the IICACTL0 register is set to 1 or when FFH is written to the IICA shift register (IICA), and the transmitting side cancels the wait state when data is written to the IICA register.

The master device can also cancel the wait state via either of the following methods.

- By setting bit 1 (STT0) of IICACTL0 register to 1
- By setting bit 0 (SPT0) of IICACTL0 register to 1

15.5.8 Interrupt request (INTIICA0) generation timing and wait control

The setting of bit 3 (WTIM0) of IICA control register 0 (IICACTL0) determines the timing by which INTIICA0 is generated and the corresponding wait control, as shown in Table 15-2.

Table 15-2. INTIICA0 Generation Timing and Wait Control

WTIM0	During Slave Device Operation			During Master Device Operation		
	Address	Data Reception	Data Transmission	Address	Data Reception	Data Transmission
0	9 Notes 1, 2	8 Note 2	8 Note 2	9	8	8
1	9 Notes 1, 2	9 Note 2	9 Note 2	9	9	9

Notes 1. The slave device's INTIICA0 signal and wait period occurs at the falling edge of the ninth clock only when there is a match with the address set to the slave address register 0 (SVA0).
At this point, $\overline{ACK}$ is generated regardless of the value set to bit 2 (ACKE0) of the IICACTL0 register. For a slave device that has received an extension code, INTIICA0 occurs at the falling edge of the eighth clock.
However, if the address does not match after restart, INTIICA0 is generated at the falling edge of the 9th clock, but wait does not occur.

2. If the received address does not match the contents of the slave address register 0 (SVA0) and extension code is not received, neither INTIICA0 nor a wait occurs.

Remark The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and wait control are both synchronized with the falling edge of these clock signals.

(1) During address transmission/reception

- Slave device operation: Interrupt and wait timing are determined depending on the conditions described in Notes 1 and 2 above, regardless of the WTIM0 bit.
- Master device operation: Interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIM0 bit.

(2) During data reception

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

(3) During data transmission

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

(4) Wait cancellation method

The four wait cancellation methods are as follows.

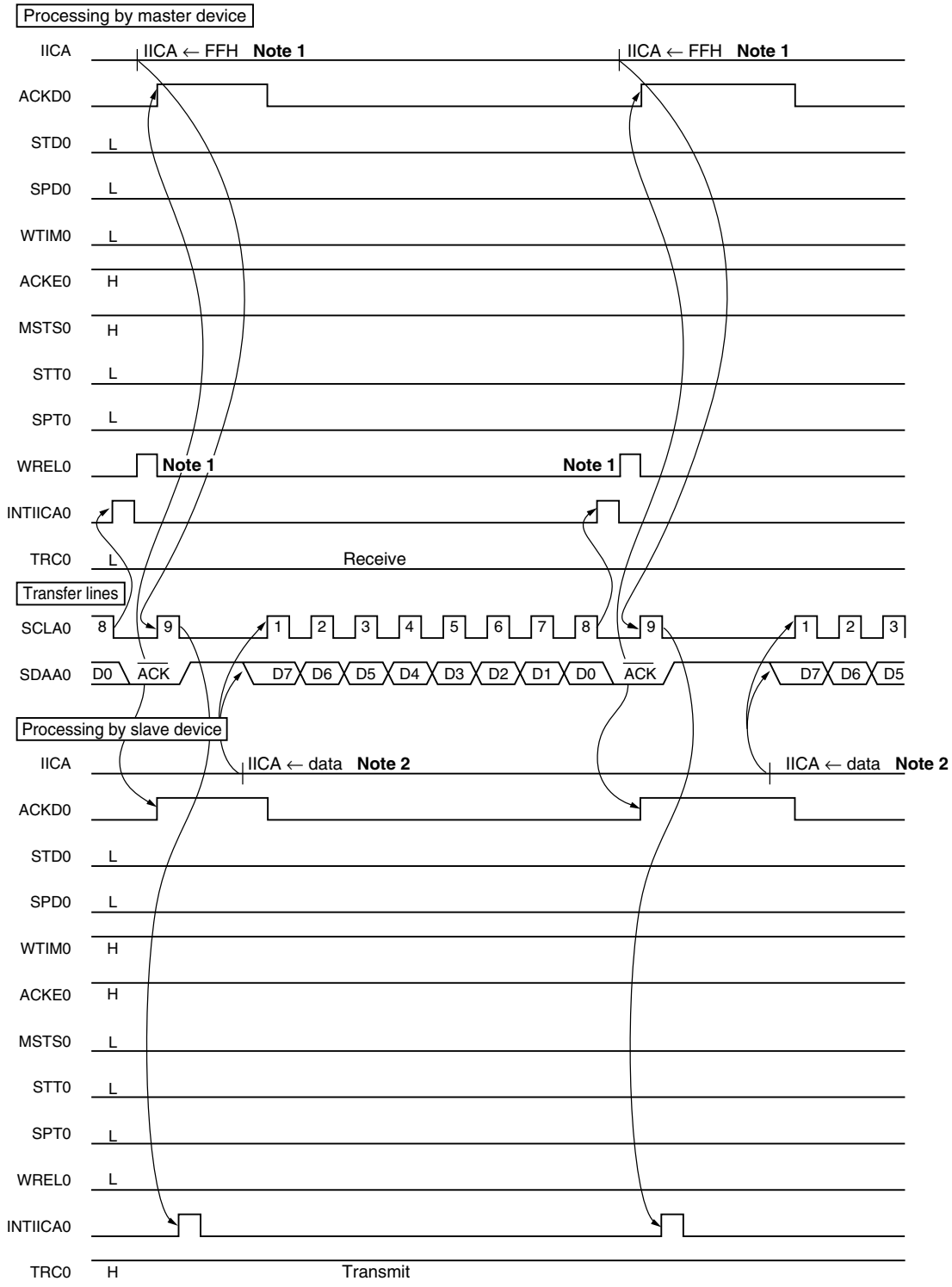
- Writing data to IICA shift register (IICA)
- Setting bit 5 (WREL0) of IICA control register 0 (IICACTL0) (canceling wait)
- Setting bit 1 (STT0) of IICACTL0 register (generating start condition) Note
- Setting bit 0 (SPT0) of IICACTL0 register (generating stop condition) Note

Note Master only.

When an 8-clock wait has been selected (WTIM0 = 0), the presence/absence of $\overline{ACK}$ generation must be determined prior to wait cancellation.

Figure 15-34. Example of Slave to Master Communication
(When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/3)

(2) Data



Notes 1. To cancel master wait, write “FFH” to IICA or set WREL0.

2. Write data to IICA, not setting WREL0, in order to cancel a wait state during slave transmission.

Figure 17-23. Format of External Interrupt Rising Edge Enable Registers (EGPCTL0, EGPCTL1) and External Interrupt Falling Edge Enable Registers (EGNCTL0, EGNCTL1) (4/5)

(f) 44-pin products of 78K0/KC2-L

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGPCTL0	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGNCTL0	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

Address: FF4AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGPCTL1	0	0	0	0	EGP11	EGP10	EGP9	EGP8

Address: FF4BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGNCTL1	0	0	0	0	EGN11	EGN10	EGP9	EGP8

EGPn	EGNn	INTPn pin valid edge selection
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

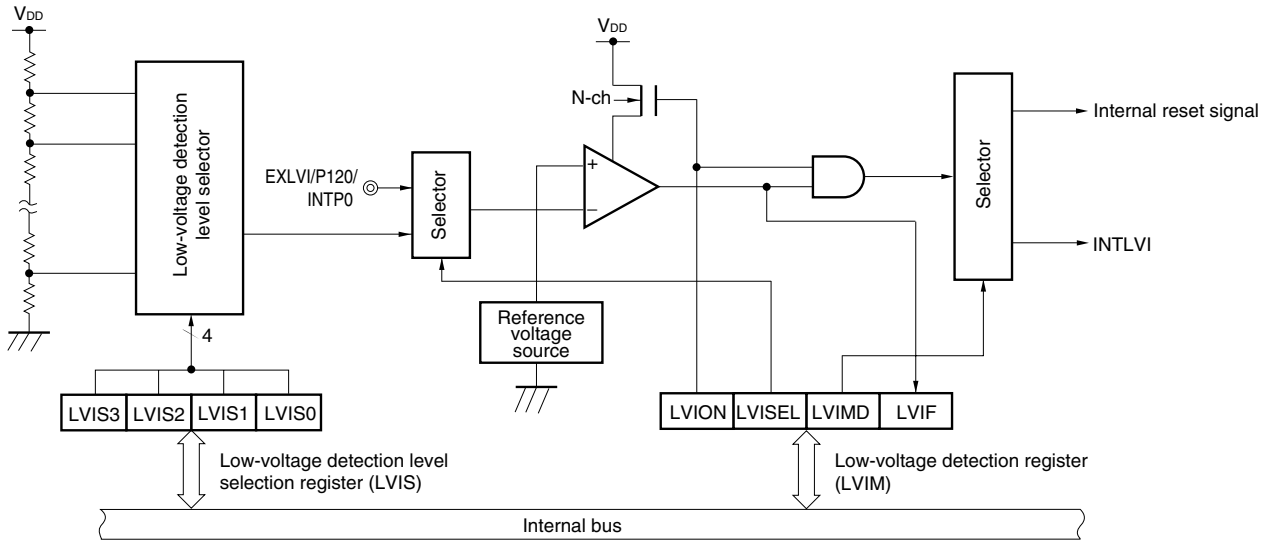
Caution Be sure to clear bits 6 and 7 of EGPCTL0 and EGNCTL0, and bits 4 to 7 of EGPCTL1 and EGNCTL1 to 0 in the 44-pin products of 78K0/KC2-L.

Remark n = 0 to 5, 8 to 11: 44-pin products of 78K0/KC2-L

22.2 Configuration of Low-Voltage Detector

The block diagram of the low-voltage detector is shown in Figure 22-1.

Figure 22-1. Block Diagram of Low-Voltage Detector



Remark EXLVI/P120/INTP0 is mounted only on 78K0/KB2-L and 78K0/KC2-L.

22.3 Registers Controlling Low-Voltage Detector

The low-voltage detector is controlled by the following registers.

- Low-voltage detection register (LVIM)
- Low-voltage detection level select register (LVIS)
- Port mode register 12 (PM12)

(1) Low-voltage detection register (LVIM)

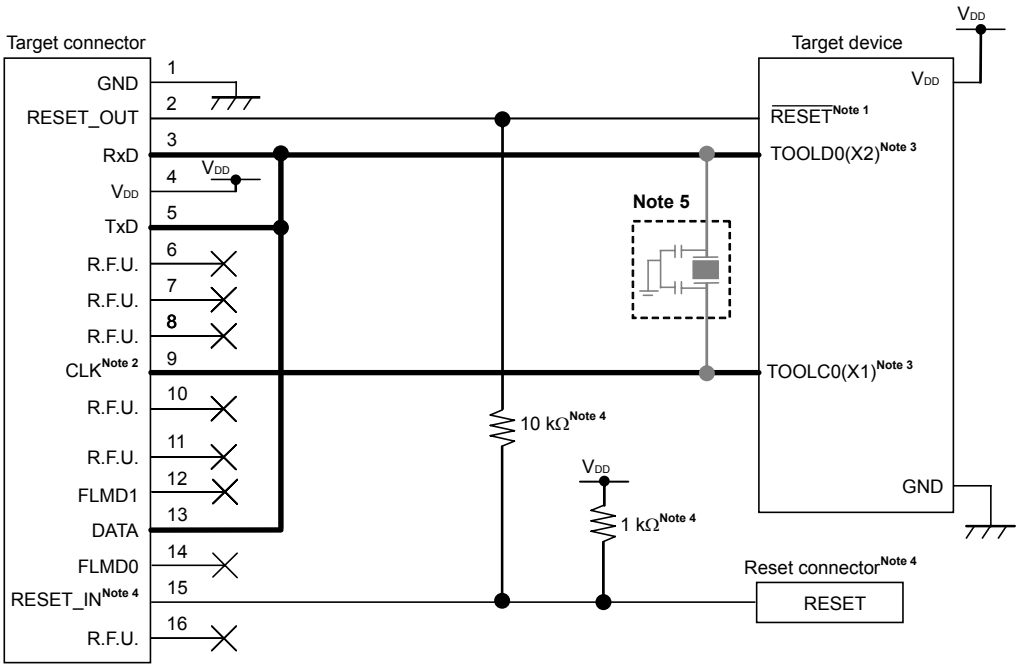
This register sets low-voltage detection and the operation mode.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

The generation of a reset signal other than an LVI reset clears this register to 00H.

<R> **Figure 26-1. Connection Example of QB-MINI2 and 78K0/Ix2 Microcontrollers (2/3)**

(2) When using the TOOLC0 and TOOLD0 pins (with X1/X2 oscillator is used, both debugging and programming are performed)



Notes 1. If there are capacitance elements such as capacitors, on-chip debugging might not operate normally.

2. A clock signal provided on the 78K0-OCD board, a 4, 8, or 16 MHz clock signal generated in QB-MINI2, or the clock signal generated by the internal high-speed oscillator of the device can be used for the clock signal of the target device during on-chip debugging.
Only the internal high-speed oscillator of the device can be used during flash programming.

3. During on-chip debugging, the settings specified by the user program are ignored, because these pins are used as pins dedicated to on-chip debugging. However, if the pins are specified as input pins, the pins must be processed (because they are left open when QB-MINI2 is not connected.)

4. This connection is designed assuming that the reset signal is output from the N-ch open-drain buffer (output resistance: 100 Ω or less). For details, refer to **4.1.3 Connection of reset pin** of QB-MINI2 On-Chip Debug Emulator with Programming Function (18371E).

5. Never connect an oscillation circuit to the 78K0-OCD board during on-chip debugging and flash programming.
To prevent an oscillation circuit from not oscillating due to wiring capacitance when the target device operates (when QB-MINI2 is not connected), also consider countermeasures such as disconnecting the oscillation circuit from the target connectors by setting the jumpers.
A program that was downloaded using the debugger does not operate when QB-MINI2 is not connected.

Caution The bold lines in the figure (TOOLD0 and TOOLC0) must be designed so that the device pins are less than 30 mm from the QB-MINI2 connectors or the paths must be shielded by connecting them to GND.

CHAPTER 27 INSTRUCTION SET

This chapter lists each instruction set of the 78K0/Kx2-L microcontrollers in table form. For details of each operation and operation code, refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

27.1 Conventions Used in Operation List

27.1.1 Operand identifiers and specification methods

Operands are written in the "Operand" column of each instruction in accordance with the specification method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more methods, select one of them. Uppercase letters and the symbols #, !, $ and [ ] are keywords and must be written as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to write the #, !, $, and [ ] symbols.

For operand register identifiers r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for specification.

Table 27-1. Operand Identifiers and Specification Methods

Identifier	Specification Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol[Note]
sfrp	Special function register symbol (16-bit manipulatable register even addresses only)[Note]
saddr	FE20H to FF1FH Immediate data or labels
saddrp	FE20H to FF1FH Immediate data or labels (even address only)
addr16	0000H to FFFFH Immediate data or labels (Only even addresses for 16-bit data transfer instructions)
addr11	0800H to 0FFFH Immediate data or labels
addr5	0040H to 007FH Immediate data or labels (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
RBn	RB0 to RB3

Note Addresses from FFD0H to FFDFH cannot be accessed with these operands.

Remark For special function register symbols, refer to **Tables 3-6 to 3-9 Special Function Register List**.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
Call/return	**CALL**	!addr16	3	7	–	(SP – 1) ← (PC + 3)H, (SP – 2) ← (PC + 3)L, PC ← addr16, SP ← SP – 2	
	CALLF	!addr11	2	5	–	(SP – 1) ← (PC + 2)H, (SP – 2) ← (PC + 2)L, PC15 – 11 ← 00001, PC10 – 0 ← addr11, SP ← SP – 2	
	CALLT	[addr5]	1	6	–	(SP – 1) ← (PC + 1)H, (SP – 2) ← (PC + 1)L, PCH ← (addr5 + 1), PCL ← (addr5), SP ← SP – 2	
	BRK		1	6	–	(SP – 1) ← PSW, (SP – 2) ← (PC + 1)H, (SP – 3) ← (PC + 1)L, PCH ← (003FH), PCL ← (003EH), SP ← SP – 3, IE ← 0	
	RET		1	6	–	PCH ← (SP + 1), PCL ← (SP), SP ← SP + 2	
	RETI		1	6	–	PCH ← (SP + 1), PCL ← (SP), PSW ← (SP + 2), SP ← SP + 3	R R R
	RETB		1	6	–	PCH ← (SP + 1), PCL ← (SP), PSW ← (SP + 2), SP ← SP + 3	R R R
Stack manipulate	**PUSH**	PSW	1	2	–	(SP – 1) ← PSW, SP ← SP – 1	
		rp	1	4	–	(SP – 1) ← rpH, (SP – 2) ← rpL, SP ← SP – 2	
	POP	PSW	1	2	–	PSW ← (SP), SP ← SP + 1	R R R
		rp	1	4	–	rpH ← (SP + 1), rpL ← (SP), SP ← SP + 2	
	MOVW	SP, #word	4	–	10	SP ← word	
		SP, AX	2	–	8	SP ← AX	
		AX, SP	2	–	8	AX ← SP	
Unconditional branch	**BR**	!addr16	3	6	–	PC ← addr16	
		$addr16	2	6	–	PC ← PC + 2 + jdisp8	
		AX	2	8	–	PCH ← A, PCL ← X	
Conditional branch	**BC**	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if CY = 1	
	BNC	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if CY = 0	
	BZ	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if Z = 1	
	BNZ	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if Z = 0	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (fCPU) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

<R> **DC Characteristics (4/8) (78K0/KA2-L (25 pins, 32 pins))**

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P02, P31 to P37, P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V			−3.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−2.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			−1.0	mA
		Total of P02, P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V			−9.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−7.5	mA
			1.8 V ≤ V_{DD} < 2.7 V			−3.0	mA
		Total of P00, P01, P31 to P37	4.0 V ≤ V_{DD} ≤ 5.5 V			−24.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−19.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			−8.0	mA
		Total of P00 to P02, P31 to P37, P60, P61[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			−50.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−29.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			−15.0	mA
	I_{OH2}	Per pin for P20 to P27, P70 to P72	AV_{REF} = V_{DD}			−0.1	mA
Output current, low[Note 2]	I_{OL1}	Per pin for P00 to P02, P31 to P37	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Total of P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			2.0	mA
		Total of P02, P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V			38.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			6.0	mA
		Total of P00, P01, P31 to P37	4.0 V ≤ V_{DD} ≤ 5.5 V			45.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			16.0	mA
		Per pin for P00 to P02, P31 to P37, P60, P61[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			65.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			50.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			29.0	mA
	I_{OL2}	Per pin for P20 to P27, P70 to P72	AV_{REF} = V_{DD}			0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} to an output pin.

2. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

3. Specification under conditions where the duty factor is 70% (time for which current is output is 0.7 × t and time for which current is not output is 0.3 × t, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of I_{OH} is n%: Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where the duty factor is 50%, I_{OH} = −20.0 mA

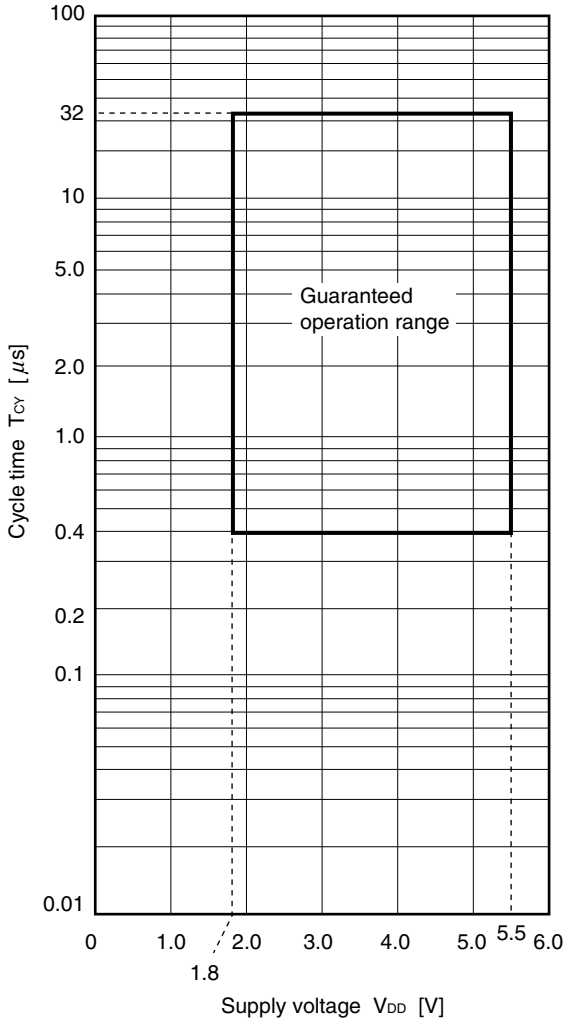
Total output current of pins = (−20.0 × 0.7)/(50 × 0.01) = −28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

T_{CY} vs. V_{DD} (Main System Clock Operation, RMC = 56H (Low Power Consumption Mode))



AC Timing Test Points