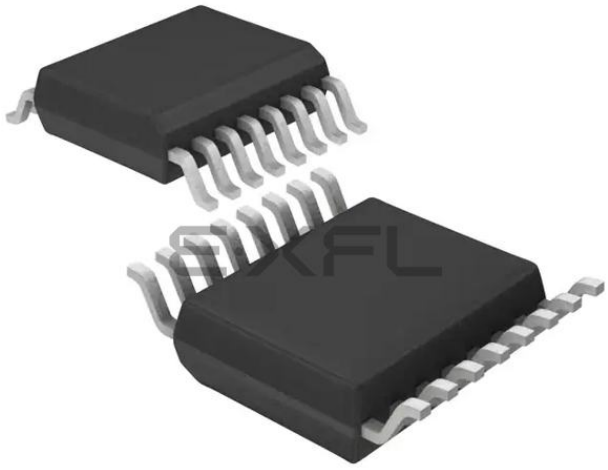
Renesas Electronics America Inc - UPD78F0552MA-FAA-AX Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	9
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0552ma-faa-ax

○ Timer

- 16-bit timer/event counter … PPG output, capture input, external event counter input
- 8-bit timer H … PWM output
- 8-bit timer/event counter 5 … PWM output, external event counter input
- Watchdog timer … Operable with low-speed internal oscillation clock
- Real-time counter … Available to count up in year, month, week, day, hour, minute, and second units

Item / Products	16-bit timer/event counter	8-bit timer	Watchdog timer	Real-time counter
78K0/KY2-L (16 pins)	1 ch	Timer H: 1 ch Timer 5: 1 ch	1 ch	–
78K0/KA2-L (20 pins)				
<R> 78K0/KA2-L (25 pins)				
<R> 78K0/KA2-L (32 pins)				
78K0/KB2-L (30 pins)		Timer H: 2 ch Timer 5: 2 ch		
<R> 78K0/KC2-L (40 pins)				1 ch
78K0/KC2-L (44 pins)				
78K0/KC2-L (48 pins)				

○ Serial interface

- UART … Asynchronous 2-wire serial interface
- IICA … Clock synchronous 2-wire serial interface, multimaster supported, standby can be released upon address match in slave mode
- CSI … Clock synchronous 3-wire serial interface

Item / Products	UART	IIC	CSI
78K0/KY2-L (16 pins)	1 ch	1 ch	–
78K0/KA2-L (20 pins)			
<R> 78K0/KA2-L (25 pins)			1 ch (CSI11[Note])
<R> 78K0/KA2-L (32 pins)			
78K0/KB2-L (30 pins)			1 ch (CSI10)
<R> 78K0/KC2-L (40 pins)			2 ch (CSI10, CSI11)
78K0/KC2-L (44 pins)			
78K0/KC2-L (48 pins)			2 ch (CSI10, CSI11[Note])

Note Can control by an enabled signal, when using CSI11 in the slave mode.

○ 10-bit resolution A/D conversion

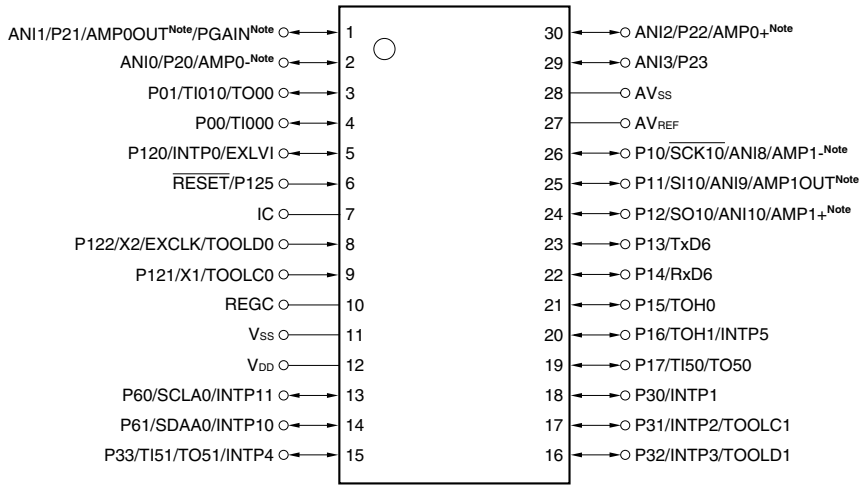
- 78K0/KY2-L: 4 ch
- <R> 78K0/KA2-L (20 pins): 6 ch, 78K0/KA2-L (25 pins): 7 ch
- <R> 78K0/KA2-L (32 pins): 11 ch
- 78K0/KB2-L: 7 ch
- <R> 78K0/KC2-L (40 pins): 10 ch, 78K0/KC2-L (44 pins, 48 pins): 11 ch

○ Operational amplifier (products with operational amplifier only)

- 78K0/KY2-L, 78K0/KA2-L: 1 ch
- 78K0/KB2-L, 78K0/KC2-L: 2 ch

1.3.3 78K0/KB2-L

- 30-pin plastic SSOP (7.62 mm (300))



AMP0- Note, AMP0+ Note,		P20 to P23 :	Port 2
AMP1- Note, AMP1+ Note :	Amplifier Input	P30 to P33 :	Port 3
AMP0OUT Note,		P60, P61 :	Port 6
AMP1OUT Note :	Amplifier Output	P120 to P122, P125 :	Port 12
PGAIN Note :	Programmable Gain	REGC :	Regulator Capacitance
	Amplifier Input	RESET :	Reset
ANI0 to ANI3,		RxD6 :	Receive Data
ANI8 to ANI10 :	Analog Input	SCLA0, SCK10 :	Serial Clock Input/Output
AVREF :	Analog Reference	SDAA0 :	Serial Data Input/Output
	Voltage	SI10 :	Serial Data Input
AVSS :	Analog Ground	SO10 :	Serial Data Output
EXCLK :	External Clock Input	TI000, TI010, TI50, TI51 :	Timer Input
	(Main System Clock)	TO00, TO50, TO51,	
EXLVI :	External potential Input	TOH0, TOH1 :	Timer Output
	for Low-voltage detector	TOOLC0, TOOLC1 :	Clock Input for Tool
IC :	Internally Connected	TOOLD0, TOOLD1 :	Data Input/Output for Tool
INTP0 to INTP5,		TxD6 :	Transmit Data
INTP10, INTP11 :	External Interrupt Input	VDD :	Power Supply
P00, P01 :	Port 0	VSS :	Ground
P10 to P17 :	Port 1	X1, X2 :	Crystal Oscillator
			(Main System Clock)

Note μPD78F0576, 78F0577, 78F0578 (products with operational amplifier) only

Cautions 1. Leave the IC (Internally Connected) pin open.
2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).
3. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, and ANI3/P23 are set in the analog input mode, P10/ANI8/AMP1-/SCK10, P11/ANI9/AMP1OUT/SI10, and P12/ANI10/AMP1+/SO10 are set in the digital input mode after release of reset.
4. RESET/P125 immediately after release of reset is set in the external reset input.

3.3 Instruction Address Addressing

An instruction address is determined by contents of the program counter (PC) and is normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to PC and branched by the following addressing (for details of instructions, refer to the **78K/0 Series Instructions User's Manual (U12326E)**).

3.3.1 Relative addressing

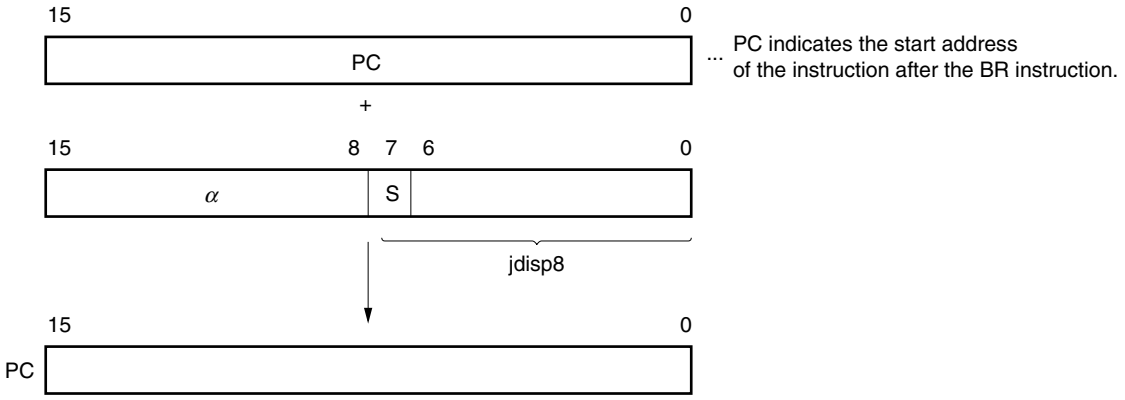
[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (−128 to +127) and bit 7 becomes a sign bit.

In other words, relative addressing consists of relative branching from the start address of the following instruction to the −128 to +127 range.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, all bits of α are 0.
When S = 1, all bits of α are 1.

4.2.1 Port 0

<R>

78K0/KY2-L (μPD78F057x)	78K0/KA2-L (μPD78F056x)			78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)		
16 Pins	20 Pins	25 Pins	32 Pins	30 Pins	40 Pins	44 Pins	48 Pins
P00/TI000/ INTP0	P00/TI000/ INTP0	P00/TI000/ INTP0(/TOH1) (/TI51)	–	P00/TI000	P00/TI000	P00/TI000	P00/TI000
P01/TO00/ TI010	P01/TO00/ TI010	–	P01/TO00/ TI010	P01/TO00/ TI010	P01/TO00/ TI010	P01/TO00 /TI010	P01/TO00/ TI010
–	–	P02/$\overline{\text{SSI11}}$/ INTP5	P02/$\overline{\text{SSI11}}$/ INTP5	–	–	–	P02/INTP7

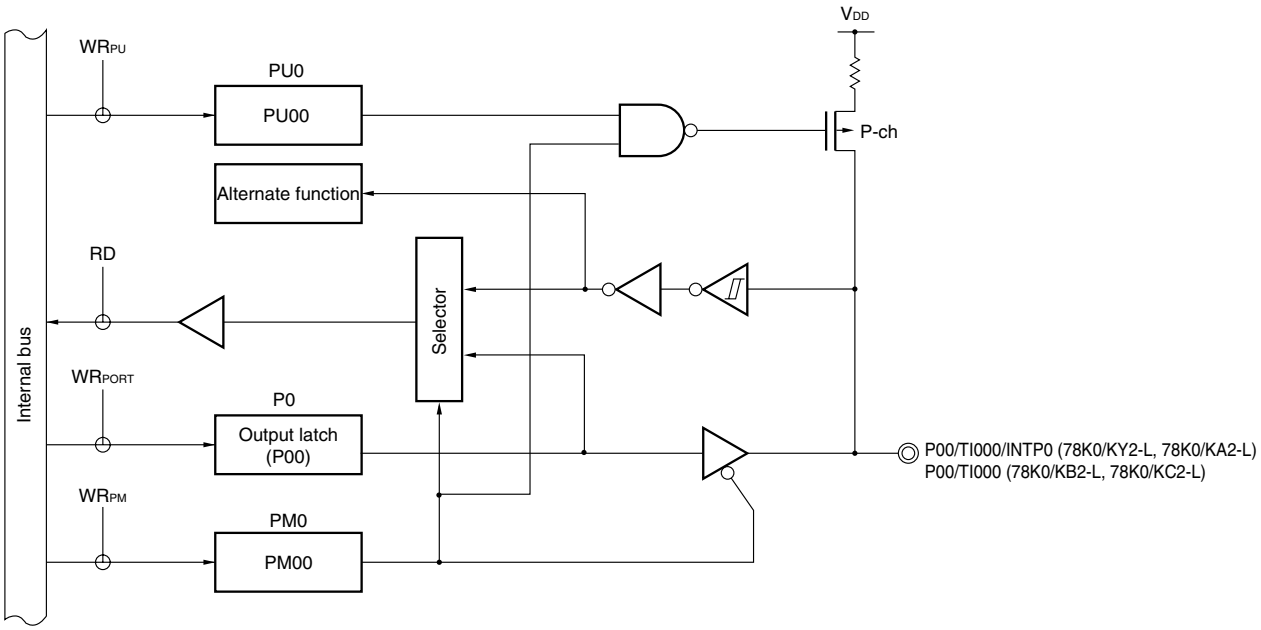
Port 0 is an I/O port with an output latch. Port 0 can be set to the input mode or output mode in 1-bit units using port mode register 0 (PM0). When the P00 to P02 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 0 (PU0).

This port can also be used for timer I/O, external interrupt request input, and chip select input of serial interface. The timer I/O can be assigned to P00 of the 78K0/KA2-L (25-pin products) by setting the port alternate switch control register (MUXSEL).

Reset signal generation sets port 0 to input mode.

Figures 4-1 to 4-3 show block diagrams of port 0.

Figure 4-1. Block Diagram of P00



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

(1) Example of setting procedure when oscillating the X1 clock

<1> Setting P121/X1 and P122/X2/EXCLK pins and selecting X1 clock or external clock (OSCCTL register)
When EXCLK is cleared to 0 and OSCSEL is set to 1, the mode is switched from port mode to X1 oscillation mode.

EXCLK	OSCSEL	Operation Mode of High-Speed System Clock Pin	P121/X1 Pin	P122/X2/EXCLK Pin
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	

<2> Controlling oscillation of X1 clock (MOC register)
If MSTOP is cleared to 0, the X1 oscillator starts oscillating.

<3> Waiting for the stabilization of the oscillation of X1 clock
Check the OSTC register and wait for the necessary time.
During the wait time, other software processing can be executed with the internal high-speed oscillation clock.

Cautions 1. Do not change the value of EXCLK and OSCSEL while the X1 clock is operating.
2. Set the X1 clock after the supply voltage has reached the operable voltage of the clock to be used (refer to CHAPTER 28 ELECTRICAL SPECIFICATIONS).

(2) Example of setting procedure when using the external main system clock

<1> Setting P121/X1 and P122/X2/EXCLK pins and selecting operation mode (OSCCTL register)
When EXCLK and OSCSEL are set to 1, the mode is switched from port mode to external clock input mode.

EXCLK	OSCSEL	Operation Mode of High-Speed System Clock Pin	P121/X1 Pin	P122/X2/EXCLK Pin
1	1	External clock input mode	Input port	External clock input

<2> Controlling external main system clock input (MOC register)
When MSTOP is cleared to 0, the input of the external main system clock is enabled.

Cautions 1. Do not change the value of EXCLK and OSCSEL while the external main system clock is operating.
2. Set the external main system clock after the supply voltage has reached the operable voltage of the clock to be used (refer to CHAPTER 28 ELECTRICAL SPECIFICATIONS).

(3) Example of setting procedure when using high-speed system clock as CPU clock and peripheral hardware clock

<1> Setting high-speed system clock oscillation[Note]
(Refer to **5.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

Note The setting of <1> is not necessary when high-speed system clock is already operating.

6.5 Special Use of TM00

6.5.1 Rewriting CR010 during TM00 operation

In principle, rewriting CR000 and CR010 of the 78K0/Kx2-L microcontrollers when they are used as compare registers is prohibited while TM00 is operating (TMC003 and TMC002 = other than 00).

However, the value of CR010 can be changed, even while TM00 is operating, using the following procedure if CR010 is used for PPG output and the duty factor is changed. (When changing the value of CR010 to a smaller value than the current one, rewrite it immediately after its value matches the value of TM00. When changing the value of CR010 to a larger value than the current one, rewrite it immediately after the values of CR000 and TM00 match. If the value of CR010 is rewritten immediately before a match between CR010 and TM00, or between CR000 and TM00, an unexpected operation may be performed.).

Procedure for changing value of CR010

<1> Disable interrupt INTTM010 (TMMK010 = 1).
<2> Disable reversal of the timer output when the value of TM00 matches that of CR010 (TOC004 = 0).
<3> Change the value of CR010.
<4> Wait for one cycle of the count clock of TM00.
<5> Enable reversal of the timer output when the value of TM00 matches that of CR010 (TOC004 = 1).
<6> Clear the interrupt flag of INTTM010 (TMIF010 = 0) to 0.
<7> Enable interrupt INTTM010 (TMMK010 = 0).

Remark For TMIF010 and TMMK010, refer to **CHAPTER 17 INTERRUPT FUNCTIONS**.

6.5.2 Setting LVS00 and LVR00

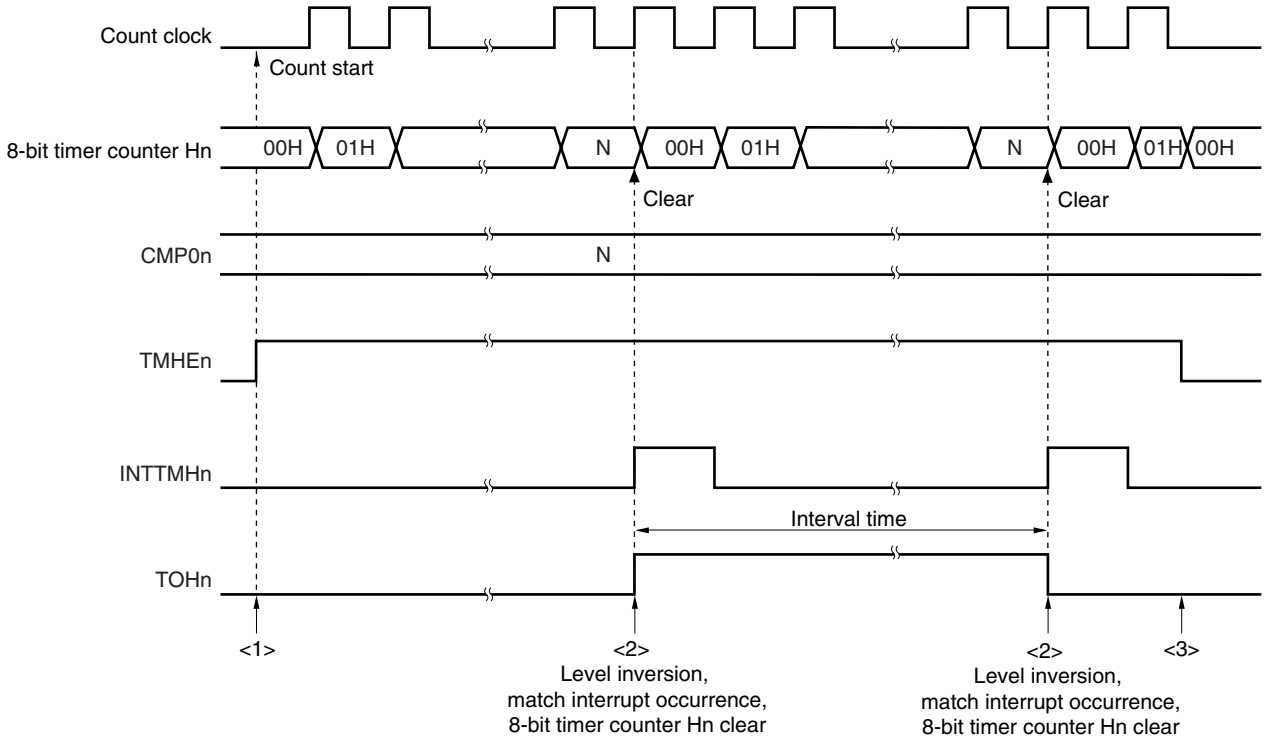
(1) Usage of LVS00 and LVR00

LVS00 and LVR00 are used to set the default value of the TO00 output and to invert the timer output without enabling the timer operation (TMC003 and TMC002 = 00). Clear LVS00 and LVR00 to 00 (default value: low-level output) when software control is unnecessary.

LVS00	LVR00	Timer Output Status
0	0	Not changed (low-level output)
0	1	Cleared (low-level output)
1	0	Set (high-level output)
1	1	Setting prohibited

Figure 8-13. Timing of Interval Timer/Square-Wave Output Operation (1/2)

(a) Basic operation (Operation When 01H ≤ CMP0n ≤ FEH)



<1> The count operation is enabled by setting the TMHEn bit to 1. The count clock starts counting no more than 1 clock after the operation is enabled.

<2> When the value of the 8-bit timer counter Hn matches the value of the CMP0n register, the value of the timer counter is cleared, and the level of the TOHn output is inverted. In addition, the INTTMHn signal is output at the rising edge of the count clock.

<3> If the TMHEn bit is cleared to 0 while timer H is operating, the INTTMHn signal and TOHn output are set to the default level. If they are already at the default level before the TMHEn bit is cleared to 0, then that level is maintained.

Remarks 1. 01H ≤ N ≤ FEH

2. 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

When using P20/ANI0/AMP0-, P21/ANI1/AMP0OUT/PGAIN, and P22/ANI2/AMP0+, set the registers according to the pin function to be used (refer to **Tables 13-4** and **13-5**).

Table 13-4. Setting Functions of P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins

ADPC0 Register	PM2 Register	OPAMP0E bit	ADS Register (n = 0, 2)	P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins
Analog input selection	Input mode	0	Selects ANIn.	Analog input (to be converted into digital signals)
			Does not select ANIn.	Analog input (not to be converted into digital signals)
		1	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Operational amplifier input
	Output mode	–	–	Setting prohibited
Digital I/O selection	Input mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital input
	Output mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital output

Remark ADPC0: A/D port configuration register 0
PM2: Port mode register 2
OPAMP0E: Bit 7 of operational amplifier 0 control register (AMP0M)
ADS: Analog input channel specification register

(3) Asynchronous serial interface transmission status register 6 (ASIF6)

This register indicates the status of transmission by serial interface UART6. It includes two status flag bits (TXBF6 and TXSF6).

Transmission can be continued without disruption even during an interrupt period, by writing the next data to the TXB6 register after data has been transferred from the TXB6 register to the TXS6 register.

This register is read-only by an 8-bit memory manipulation instruction.

Reset signal generation, or clearing bit 7 (POWER6) or bit 6 (TXE6) of ASIM6 to 0 clears this register to 00H.

Figure 14-7. Format of Asynchronous Serial Interface Transmission Status Register 6 (ASIF6)

Address: FF55H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASIF6	0	0	0	0	0	0	TXBF6	TXSF6

TXBF6	Transmit buffer data flag
0	If POWER6 = 0 or TXE6 = 0, or if data is transferred to transmit shift register 6 (TXS6)
1	If data is written to transmit buffer register 6 (TXB6) (if data exists in TXB6)

TXSF6	Transmit shift register data flag
0	If POWER6 = 0 or TXE6 = 0, or if the next data is not transferred from transmit buffer register 6 (TXB6) after completion of transfer
1	If data is transferred from transmit buffer register 6 (TXB6) (if data transmission is in progress)

Cautions 1. To transmit data continuously, write the first transmit data (first byte) to the TXB6 register. Be sure to check that the TXBF6 flag is "0". If so, write the next transmit data (second byte) to the TXB6 register. If data is written to the TXB6 register while the TXBF6 flag is "1", the transmit data cannot be guaranteed.

2. To initialize the transmission unit upon completion of continuous transmission, be sure to check that the TXSF6 flag is "0" after generation of the transmission completion interrupt, and then execute initialization. If initialization is executed while the TXSF6 flag is "1", the transmit data cannot be guaranteed.

(4) Clock selection register 6 (CKSR6)

This register selects the base clock of serial interface UART6.

CKSR6 can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Remark CKSR6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1).

Figure 15-5. Format of IICA Control Register 0 (IICACTL0) (4/4)

SPT0	Stop condition trigger
0	Stop condition is not generated.
1	Stop condition is generated (termination of master device's transfer).

Cautions concerning set timing
- For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the waiting period when ACKE0 has been cleared to 0 and slave has been notified of final reception.
- For master transmission: A stop condition cannot be generated normally during the acknowledge period. Therefore, set it during the wait period that follows output of the ninth clock.
- Cannot be set to 1 at the same time as start condition trigger (STT0).
- The SPT0 bit can be set to 1 only when in master mode.
- When the WTIM0 bit has been cleared to 0, if the SPT0 bit is set to 1 during the wait period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock. The WTIM0 bit should be changed from 0 to 1 during the wait period following the output of eight clocks, and the SPT0 bit should be set to 1 during the wait period that follows the output of the ninth clock.
- Setting the SPT0 bit to 1 and then setting it again before it is cleared to 0 is prohibited.

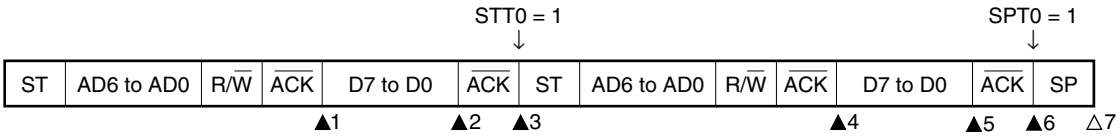
Condition for clearing (SPT0 = 0)	Condition for setting (SPT0 = 1)
• Cleared by loss in arbitration • Automatically cleared after stop condition is detected • Cleared by LREL0 = 1 (exit from communications) • When IICE0 = 0 (operation stop) • Reset	• Set by instruction

Caution When bit 3 (TRC0) of the IICA status register 0 (IICAS0) is set to 1 (transmission status), bit 5 (WREL0) of the IICACTL0 register is set to 1 during the ninth clock and wait is canceled, after which the TRC0 bit is cleared (reception status) and the SDAA0 line is set to high impedance. Release the wait performed while the TRC0 bit is 1 (transmission status) by writing to the IICA shift register.

Remark Bit 0 (SPT0) becomes 0 when it is read after data setting.

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

(i) When WTIM0 = 0

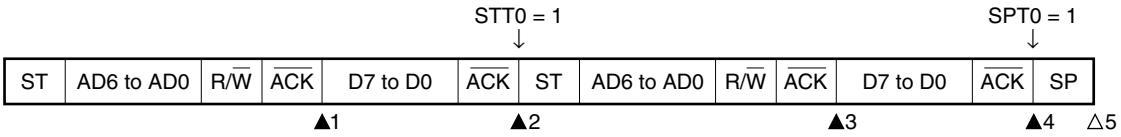


▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 1000×000B (Sets WTIM0 to 1)[Note 1]
▲3: IICAS0 = 1000××00B (Clears WTIM0 to 0[Note 2], sets STT0 to 1)
▲4: IICAS0 = 1000×110B
▲5: IICAS0 = 1000×000B (Sets WTIM0 to 1)[Note 3]
▲6: IICAS0 = 1000××00B (Sets SPT0 to 1)
△7: IICAS0 = 00000001B

Notes 1. To generate a start condition, set WTIM0 to 1 and change the timing for generating the INTIICA0 interrupt request signal.
2. Clear WTIM0 to 0 to restore the original setting.
3. To generate a stop condition, set WTIM0 to 1 and change the timing for generating the INTIICA0 interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1

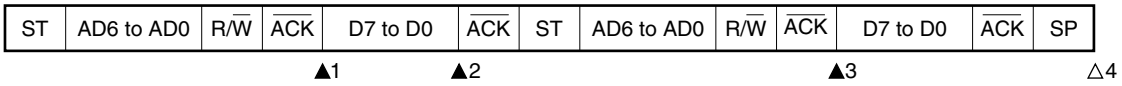


▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 1000××00B (Sets STT0 to 1)
▲3: IICAS0 = 1000×110B
▲4: IICAS0 = 1000××00B (Sets SPT0 to 1)
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(d) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, does not match address (= not extension code))

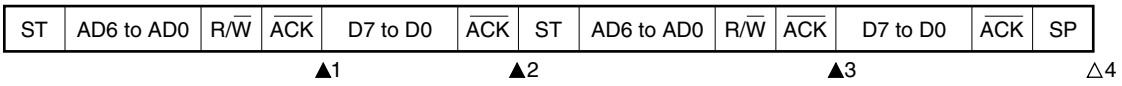


▲1 ▲2 ▲3 △4

▲1: IICAS0 = 0001×110B
▲2: IICAS0 = 0001×000B
▲3: IICAS0 = 00000110B
△4: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, does not match address (= not extension code))



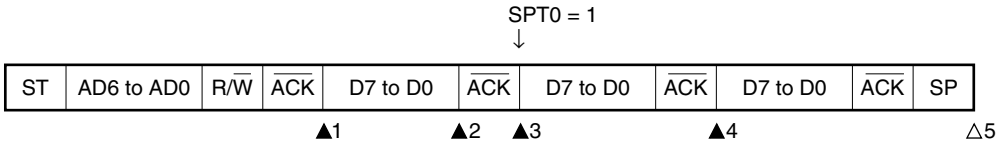
▲1 ▲2 ▲3 △4

▲1: IICAS0 = 0001×110B
▲2: IICAS0 = 0001××00B
▲3: IICAS0 = 00000110B
△4: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(h) When arbitration loss occurs due to low-level data when attempting to generate a stop condition

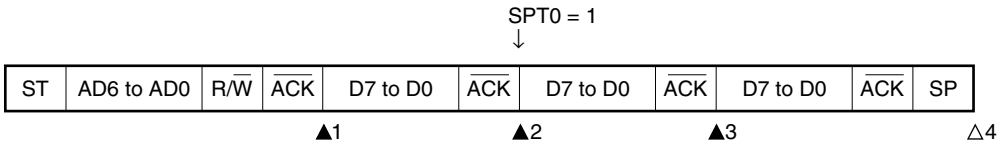
(i) When WTIM0 = 0



▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 1000×000B (Sets WTIM0 to 1)
▲3: IICAS0 = 1000×100B (Clears WTIM0 to 0)
▲4: IICAS0 = 01000100B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1



▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 1000×100B (Sets SPT0 to 1)
▲3: IICAS0 = 01000100B
△4: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

- Serial operation mode register 11 (CSIM11)

Address: FF88H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CSIM11	CSIE11	TRMD11	SSE11	DIR11	0	0	0	CSOT11

CSIE11	Operation control in 3-wire serial I/O mode
0	Disables operation[Note 1] and asynchronously resets the internal circuit[Note 2].

Notes 1. To use P62/SO11, P60/$\overline{\text{SCK11}}$/SCLA0, and P42/$\overline{\text{SSI11}}$/PCL/INTP6 as general-purpose ports when CSISEL = 0, set CSIM11 in the default status (00H).
To use P120/SO11/INTP0/EXLVI, P40/$\overline{\text{SCK11}}$/RTCCL/RTCDIV, and P42/$\overline{\text{SSI11}}$/PCL/INTP6 as general-purpose ports when CSISEL = 1, set CSIM11 in the default status (00H).
To use P37/SO11, P35/$\overline{\text{SCK11}}$, and P02/$\overline{\text{SSI11}}$/INTP5 as general-purpose ports when CSISEL = 1, set CSIM11 in the default status (00H).

2. Bit 0 (CSOT11) of CSIM11 and serial I/O shift register 11 (SIO11) are reset.

16.4.2 3-wire serial I/O mode

The 3-wire serial I/O mode is used for connecting peripheral ICs and display controllers with a clocked serial interface.

In this mode, communication is executed by using three lines: the serial clock ($\overline{\text{SCK1n}}$), serial output (SO1n), and serial input (SI1n) lines.

(1) Registers used

- Serial operation mode register 1n (CSIM1n)
- Serial clock selection register 1n (CSIC1n)
- Port mode register x (PMx)
- Port register x (Px)

The basic procedure of setting an operation in the 3-wire serial I/O mode is as follows.

<1> Set the CSIC1n register (refer to **Figures 16-6** and **16-7**).
<2> Set bits 4 to 6 (DIR1n, SSE11 (serial interface CSI11 only), and TRMD1n) of the CSIM1n register (refer to **Figures 16-4** and **16-5**).
<3> Set bit 7 (CSIE1n) of the CSIM1n register to 1. → Transmission/reception is enabled.
<4> Write data to transmit buffer register 1n (SOTB1n). → Data transmission/reception is started.
Read data from serial I/O shift register 1n (SIO1n). → Data reception is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

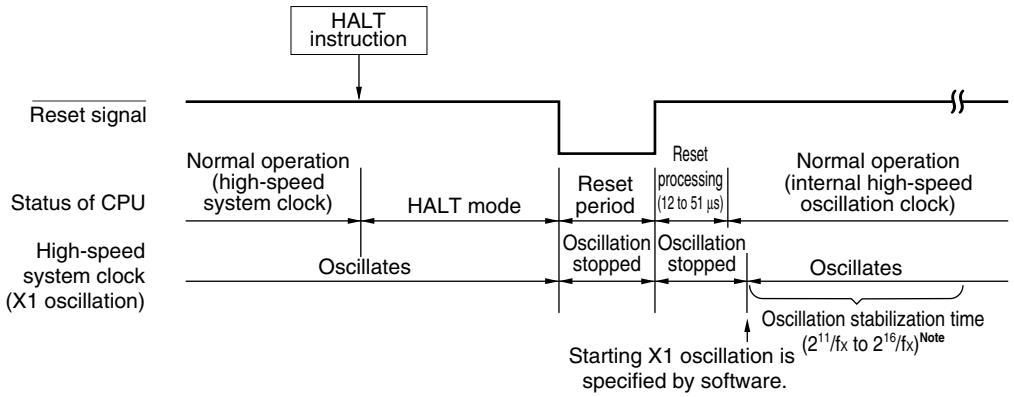
Remark 78K0/KA2-L (25, 32-pin products): n = 0, x = 0, 3
78K0/KB2-L: n = 0, x = 1
78K0/KC2-L: n = 0, 1, x = 1, 4, 6, 12

(b) Release by reset signal generation

When the reset signal is generated, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

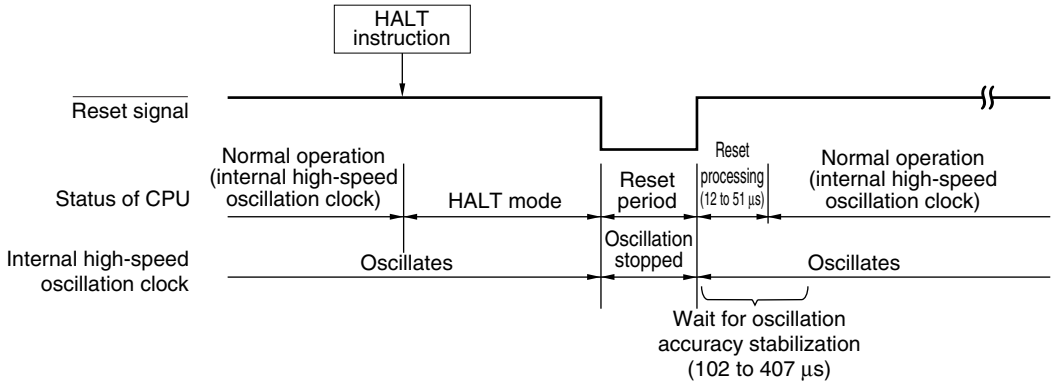
Figure 19-4. HALT Mode Release by Reset (1/2)

(1) When high-speed system clock is used as CPU clock



Note Oscillation stabilization time is not required when using the external main system clock (f_{EXCLK}) as the high-speed system clock.

(2) When internal high-speed oscillation clock is used as CPU clock



Remark fx: X1 clock oscillation frequency

CHAPTER 20 RESET FUNCTION

The reset function is mounted onto all 78K0/Kx2-L microcontroller products.

The following four operations are available to generate a reset signal.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
(4) Internal reset by comparison of supply voltage of the low-voltage detector (LVI) or input voltage from external input pin (EXLVI pin), and detection voltage

External and internal resets start program execution from the address at 0000H and 0001H when the reset signal is generated.

A reset is applied when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POC and LVI circuit voltage detection, and each item of hardware is set to the status shown in Tables 20-1 and 20-2. Each pin is high impedance during reset signal generation or during the oscillation stabilization time just after a reset release.

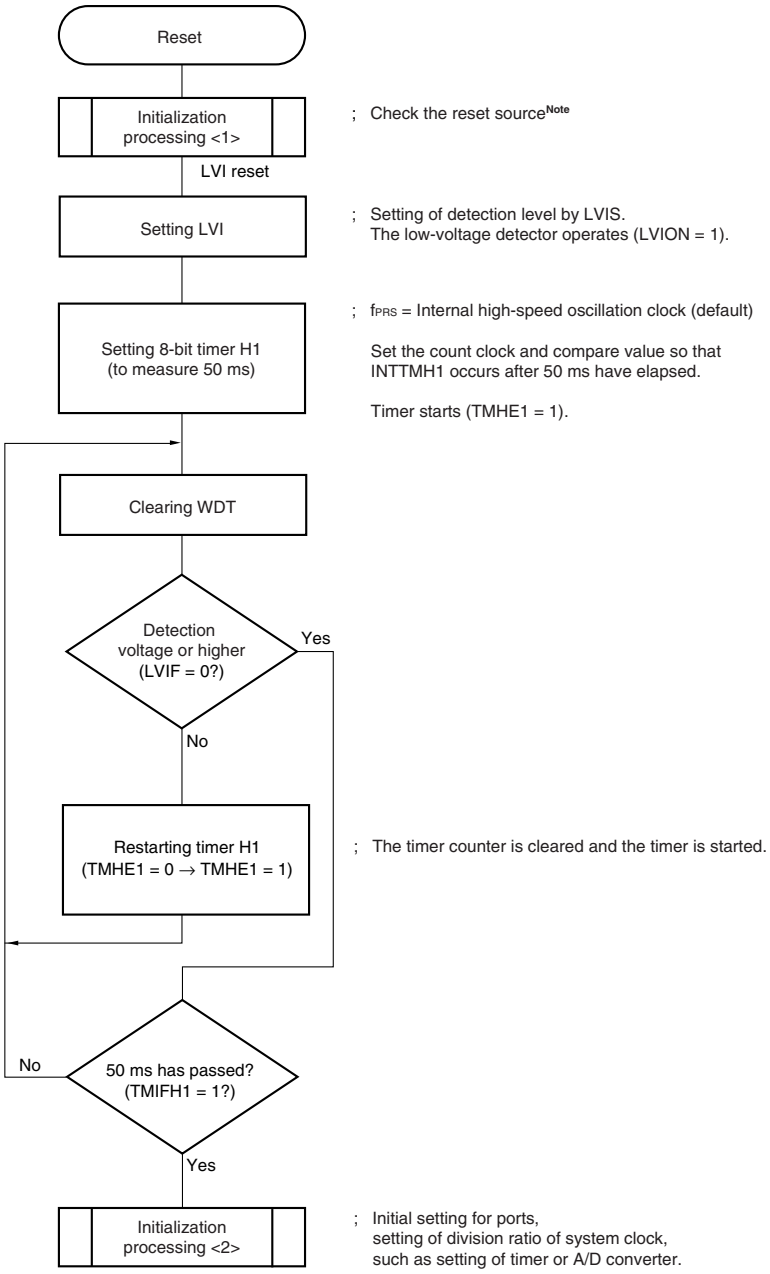
When a low level is input to the $\overline{\text{RESET}}$ pin, the device is reset. It is released from the reset status when a high level is input to the $\overline{\text{RESET}}$ pin and program execution is started with the internal high-speed oscillation clock after reset processing. A reset by the watchdog timer is automatically released, and program execution starts using the internal high-speed oscillation clock (refer to **Figures 20-2** to **20-4**) after reset processing. Reset by POC and LVI circuit power supply detection is automatically released when $V_{DD} \geq V_{POR}$ or $V_{DD} \geq V_{LVI}$ after the reset, and program execution starts using the internal high-speed oscillation clock (refer to **CHAPTER 21 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 22 LOW-VOLTAGE DETECTOR**) after reset processing.

Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.
(If an external reset is effected upon power application, the period during which the supply voltage is outside the operating range (V_{DD} < 1.8 V) is not counted in the 10 μs. However, the low-level input may be continued before POC is released.)
2. During reset signal generation, the X1 clock, XT1 clock[Note], internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input and external subsystem clock[Note] input become invalid.
3. When the STOP mode is released by a reset, the RAM contents in the STOP mode are held during reset input. However, because SFR is initialized, the port pins become high-impedance.

Note 78K0/KC2-L only

Figure 22-11. Example of Software Processing After Reset Release (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of LVI detection voltage



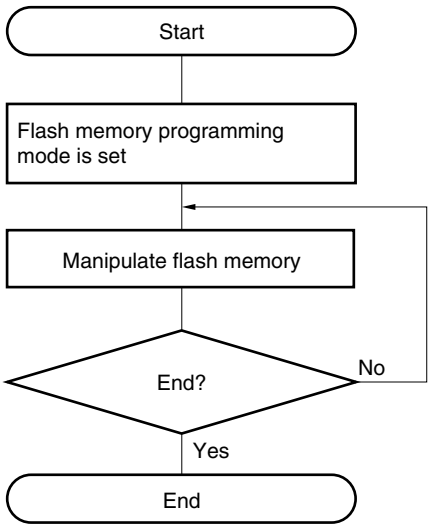
Note A flowchart is shown on the next page.

25.5 Programming Method

25.5.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

Figure 25-6. Flash Memory Manipulation Procedure



25.5.2 Flash memory programming mode

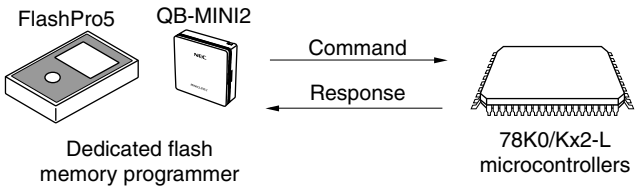
To rewrite the contents of the flash memory by using the dedicated flash memory programmer, set the 78K0/Kx2-L microcontrollers in the flash memory programming mode. The system switches to the flash memory programming mode once the dedicated flash memory programmer is connected and communication starts.

Change the mode by using a jumper when writing the flash memory on-board.

25.5.3 Communication commands

The 78K0/Kx2-L microcontrollers communicate with the dedicated flash memory programmer by using commands. The signals sent from the flash memory programmer to the 78K0/Kx2-L microcontrollers are called commands, and the signals sent from the 78K0/Kx2-L microcontrollers to the dedicated flash memory programmer are called response.

Figure 25-7. Communication Commands



The flash memory control commands of the 78K0/Kx2-L microcontrollers are listed in the table below. All these commands are issued from the programmer and the 78K0/Kx2-L microcontrollers perform processing corresponding to the respective commands.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(7) LVI

(T_A = –40 to +85°C, $V_{PDR} \le V_{DD} \le 5.5$ V, V_{SS} =0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.12	4.22	4.32	V
		V_{LVI1}		3.97	4.07	4.17	V
		V_{LVI2}		3.82	3.92	4.02	V
		V_{LVI3}		3.66	3.76	3.86	V
		V_{LVI4}		3.51	3.61	3.71	V
		V_{LVI5}		3.35	3.45	3.55	V
		V_{LVI6}		3.20	3.30	3.40	V
		V_{LVI7}		3.05	3.15	3.25	V
		V_{LVI8}		2.89	2.99	3.09	V
		V_{LVI9}		2.74	2.84	2.94	V
		V_{LVI10}		2.58	2.68	2.78	V
		V_{LVI11}		2.43	2.53	2.63	V
		V_{LVI12}		2.28	2.38	2.48	V
		V_{LVI13}		2.12	2.22	2.32	V
		V_{LVI14}		2.00	2.07	2.14	V
		V_{LVI15}		1.81	1.91	2.01	V
	External input pin[Note 1]	EXLVI	EXLVI < V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
	Supply voltage when power supply voltage is turned on	V_{DDLVI}	When LVI default start function enabled is set (LVISTART = 1)	1.81	1.91	2.01	V
Minimum pulse width		t_{LW}		200			μs
Detection delay time						200	μs
Operation stabilization wait time[Note 2]		t_{LWAIT}				10	μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 15

LVI Circuit Timing