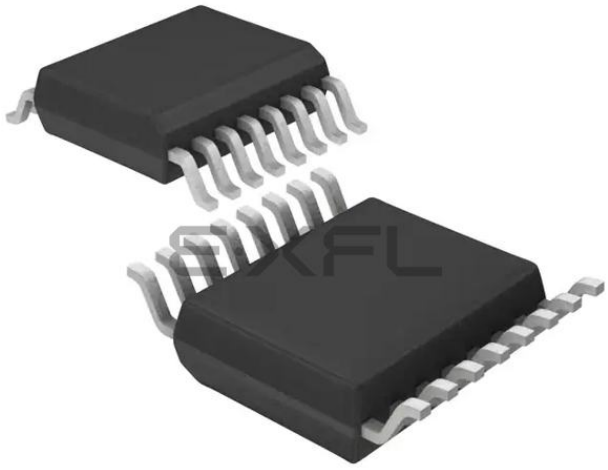
Renesas Electronics America Inc - UPD78F0555MA-FAA-AX Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

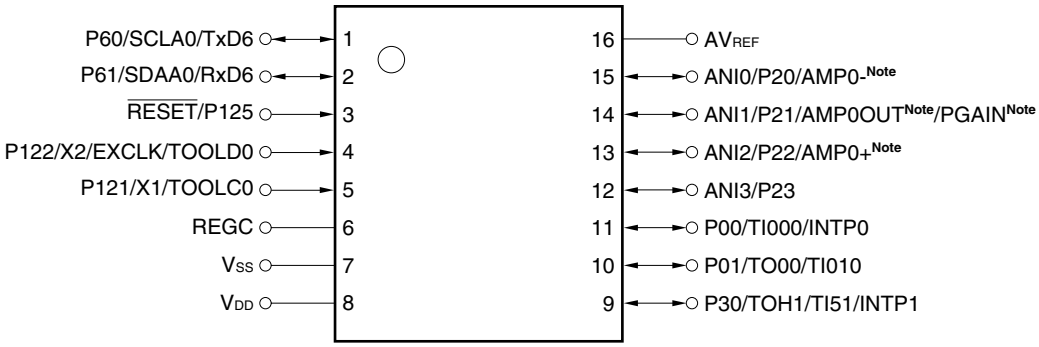
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	9
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0555ma-faa-ax

1.3 Pin Configuration (Top View)

1.3.1 78K0/KY2-L

- 16-pin plastic SSOP (5.72 mm (225))



AMP0-Note, AMP0+Note:	Amplifier Input	P121, P122, P125 :	Port 12
AMP0OUTNote:	Amplifier Output	REGC :	Regulator Capacitance
PGAINNote:	Programmable Gain	RESET :	Reset
	Amplifier Input	RxD6 :	Receive Data
ANI0 to ANI3 :	Analog Input	SCLA0 :	Serial Clock Input/Output
AVREF :	Analog Reference	SDAA0 :	Serial Data Input/Output
	Voltage	TI000, TI010, TI51 :	Timer Input
EXCLK :	External Clock Input	TO00, TOH1 :	Timer Output
	(Main System Clock)	TOOLC0 :	Clock Input for Tool
INTP0, INTP1 :	External Interrupt	TOOLD0 :	Data Input/Output for Tool
	Input	TxD6 :	Transmit Data
P00, P01 :	Port 0	VDD :	Power Supply
P20 to P23 :	Port 2	VSS :	Ground
P30 :	Port 3	X1, X2 :	Crystal Oscillator
P60, P61 :	Port 6		(Main System Clock)

Note μPD78F0555, 78F0556, 78F0557 (products with operational amplifier) only

Cautions 1. VSS functions alternately as the ground potential of the A/D converter. Be sure to connect VSS to a stabilized GND (= 0 V).

2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

3. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, and ANI3/P23 are set in the analog input mode after release of reset.

4. RESET/P125 immediately after release of reset is set in the external reset input.

<R>

Figure 2-1. Pin I/O Circuit List (4/4)

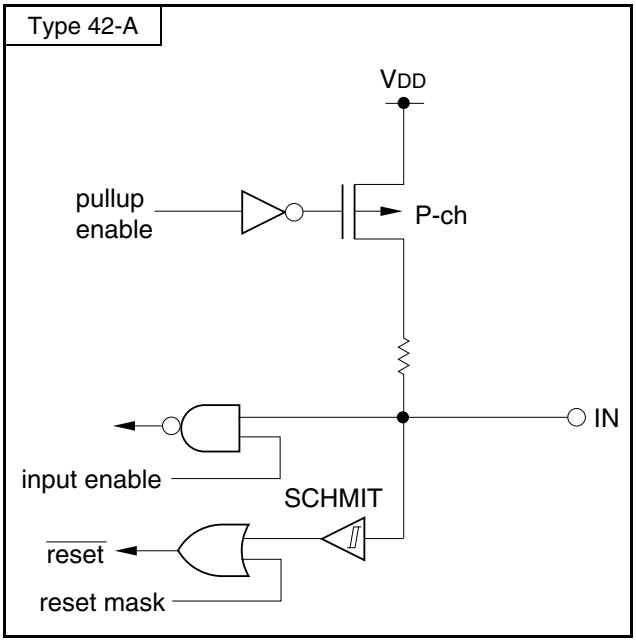


Table 4-2. Port Functions (78K0/KY2-L)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000/INTP0
P01				TO00/TI010
P20	I/O	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0/AMP0-Note
P21				ANI1/AMP0OUTNote/ PGAINNote
P22				ANI2/AMP0+Note
P23				ANI3
P30	I/O	Port 3. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOH1/TI51/INTP1
P60	I/O	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Input can be set to SMBus input buffer in 1-bit units. Output can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCLA0/TxD6
P61				SDAA0/RxD6
P121	Input	Port 12. 3-bit input-only port. For only P125, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	X1/TOOLC0
P122				X2/EXCLK/TOOLD0
P125			Reset input	$\overline{\text{RESET}}$

Note μPD78F0555, 78F0556, and 78F0557 (products with operational amplifier) only

Figure 4-48. Format of A/D Port Configuration Register 0, 1 (ADPC0, ADPC1) (2/2)

(e) 78K0/KB2-L

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	ADPCS3	ADPCS2	ADPCS1	ADPCS0

Address: FF2FH After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC1	0	0	0	0	0	ADPCS10	ADPCS9	ADPCS8

(f) 78K0/KC2-L (40-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	ADPCS6	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

Address: FF2FH After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC1	0	0	0	0	0	ADPCS10	ADPCS9	ADPCS8

(g) 78K0/KC2-L (44-pin and 48-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	ADPCS7	ADPCS6	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

Address: FF2FH After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC1	0	0	0	0	0	ADPCS10	ADPCS9	ADPCS8

ADPCSn	Digital I/O or analog I/O selection (n = 0 to 10)
0	Analog I/O
1	Digital I/O

Cautions 1. Set the pin set to analog input to the input mode by using port mode register 1, 2, and 7 (PM1, PM2, and PM7).

2. If data is written to ADPC0 and ADPC1, a wait cycle is generated. Do not write data to ADPC0 and ADPC1 when the peripheral hardware clock is stopped. For details, refer to CHAPTER 31 CAUTIONS FOR WAIT.

4.6 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P10 is an output port, P11 to P17 are input ports (all pin statuses are high level), and the port latch value of port 1 is 00H, if the output of output port P10 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 1 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the 78K0/Kx2-L microcontrollers.

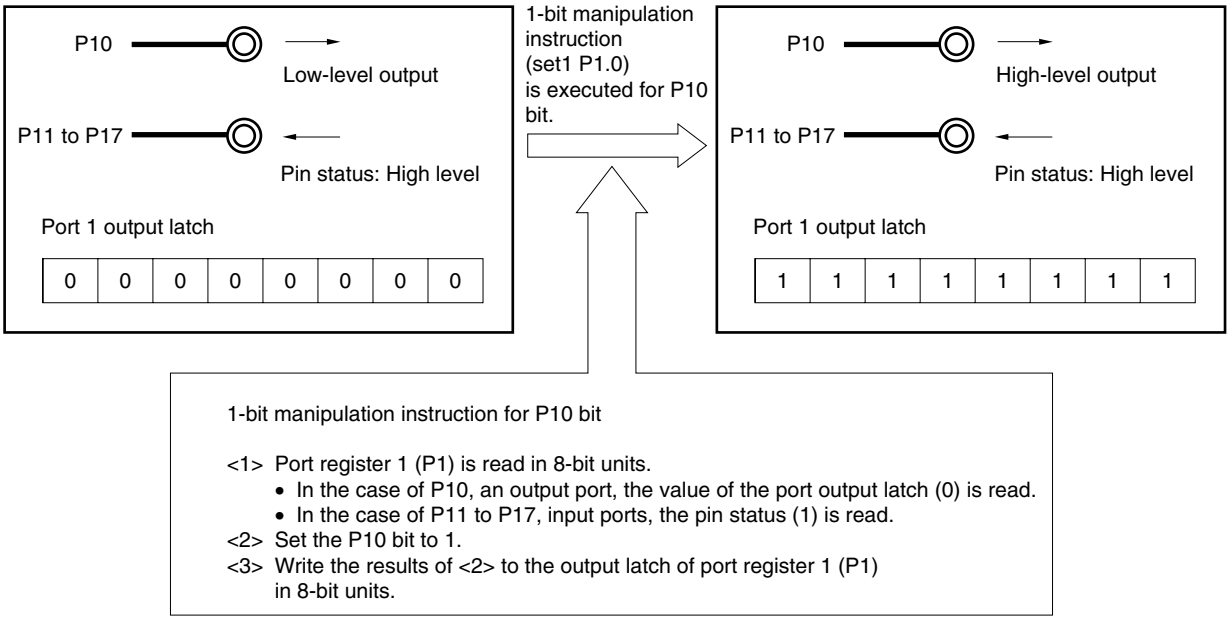
<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P10, which is an output port, is read, while the pin statuses of P11 to P17, which are input ports, are read. If the pin statuses of P11 to P17 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 4-50 1-Bit Manipulation Instruction (P10)



Remark The following instructions are 1-bit manipulation instructions.

- MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1

<2> Setting the high-speed system clock as the main system clock (MCM register)

When XSEL and MCM0 are set to 1, the high-speed system clock is supplied as the main system clock and peripheral hardware clock.

XSEL	MCM0	Selection of Main System Clock and Clock Supplied to Peripheral Hardware	
		Main System Clock (f_{XP})	Peripheral Hardware Clock (f_{PRS})
1	1	High-speed system clock (f_{XH})	High-speed system clock (f_{XH})

Caution If the high-speed system clock is selected as the main system clock, a clock other than the high-speed system clock cannot be set as the peripheral hardware clock.

<3> Setting the main system clock as the CPU clock and selecting the division ratio (PCC register)

When CSS is cleared to 0, the main system clock is supplied to the CPU. To select the CPU clock division ratio, use PCC0, PCC1, and PCC2.

CSS	PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
0	0	0	0	f_{XP}
	0	0	1	f_{XP}/2 (default)
	0	1	0	$f_{XP}/2^2$
	0	1	1	$f_{XP}/2^3$
	1	0	0	$f_{XP}/2^4$
	Other than above			Setting prohibited

(4) Example of setting procedure when stopping the high-speed system clock

The high-speed system clock can be stopped in the following two ways.

- Executing the STOP instruction and stopping the X1 oscillation (disabling clock input if the external clock is used)
- Setting MSTOP to 1 and stopping the X1 oscillation (disabling clock input if the external clock is used)

(a) To execute a STOP instruction

<1> Setting to stop peripheral hardware

Stop peripheral hardware that cannot be used in the STOP mode (for peripheral hardware that cannot be used in STOP mode, refer to **CHAPTER 19 STANDBY FUNCTION**).

<2> Setting the X1 clock oscillation stabilization time after standby release

When the CPU is operating on the X1 clock, set the value of the OSTS register before the STOP instruction is executed.

<3> Executing the STOP instruction

When the STOP instruction is executed, the system is placed in the STOP mode and X1 oscillation is stopped (the input of the external clock is disabled).

CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00

<R>

Item	78K0/KY2-L (μPD78F055x)	78K0/KA2-L (μPD78F056x)			78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)
	16 Pins	20 Pins	25 Pins	32 Pins	30 Pins	40, 44, 48 Pins
16-bit timer/event counter 00	√	√	√	√	√	√
Timer I/O pin	input: 1, output: 1 or input: 2	input: 1, output: 1 or input: 2	input: 1, output: none	input: 1 or output 1 or input: 2 or input: 1, output: 1	input: 1, output: 1 or input: 2	input: 1, output: 1 or input: 2

Remark √: Mounted, –: Not mounted

6.1 Functions of 16-Bit Timer/Event Counter 00

16-bit timer/event counter 00 is mounted onto all 78K0/Kx2-L microcontroller products.

16-bit timer/event counter 00 has the following functions.

(1) Interval timer

16-bit timer/event counter 00 generates an interrupt request at the preset time interval.

(2) Square-wave output

16-bit timer/event counter 00 can output a square wave with any selected frequency.

(3) External event counter

16-bit timer/event counter 00 can measure the number of pulses of an externally input signal.

(4) One-shot pulse output

16-bit timer event counter 00 can output a one-shot pulse whose output pulse width can be set freely.

(5) PPG output

16-bit timer/event counter 00 can output a rectangular wave whose frequency and output pulse width can be set freely.

(6) Pulse width measurement

16-bit timer/event counter 00 can measure the pulse width of an externally input signal.

(2) Operation in clear & start mode entered by TI000 pin valid edge input
(CR000: compare register, CR010: capture register)

Figure 6-25. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register)

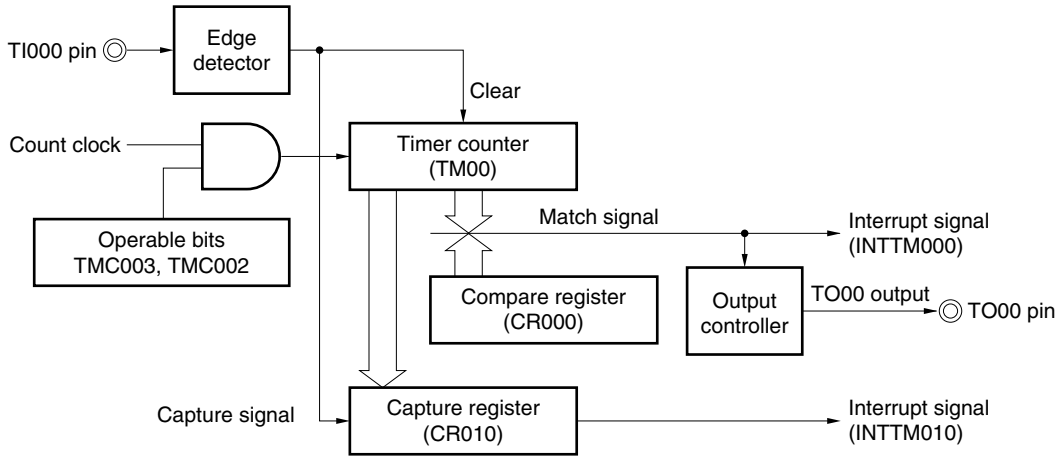
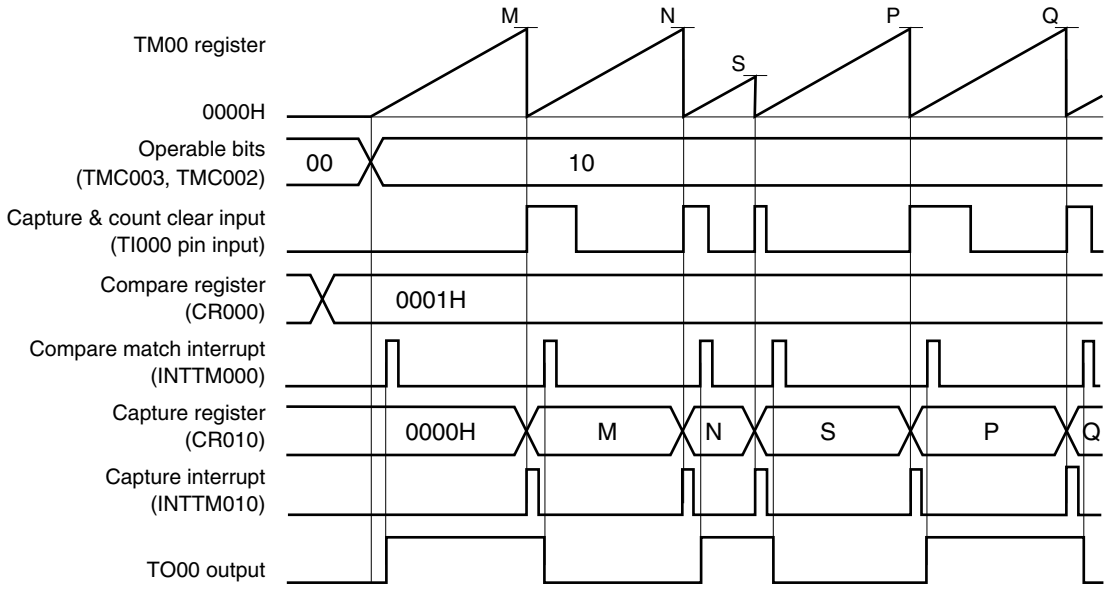


Figure 6-26. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (1/2)

(a) TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 08H, CR000 = 0001H

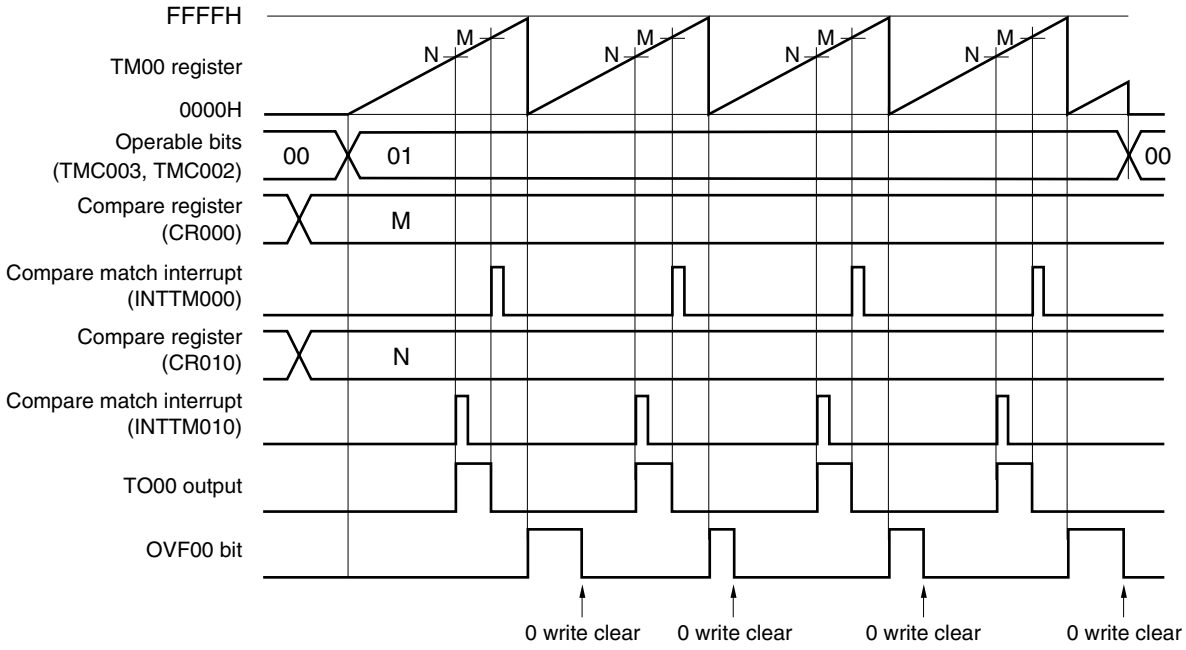


This is an application example where the TO00 output level is inverted when the count value has been captured & cleared.

The count value is captured to CR010 and TM00 is cleared (to 0000H) when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0001H, a compare match interrupt signal (INTTM000) is generated, and the TO00 output level is inverted.

Figure 6-34. Timing Example of Free-Running Timer Mode
(CR000: Compare Register, CR010: Compare Register)

• TOC00 = 13H, PRM00 = 00H, CRC00 = 00H, TMC00 = 04H



This is an application example where two compare registers are used in the free-running timer mode.

The TO00 output level is reversed each time the count value of TM00 matches the set value of CR000 or CR010. When the count value matches the register value, the INTTM000 or INTTM010 signal is generated.

(2) Free-running timer mode operation
(CR000: compare register, CR010: capture register)

Figure 6-35. Block Diagram of Free-Running Timer Mode
(CR000: Compare Register, CR010: Capture Register)

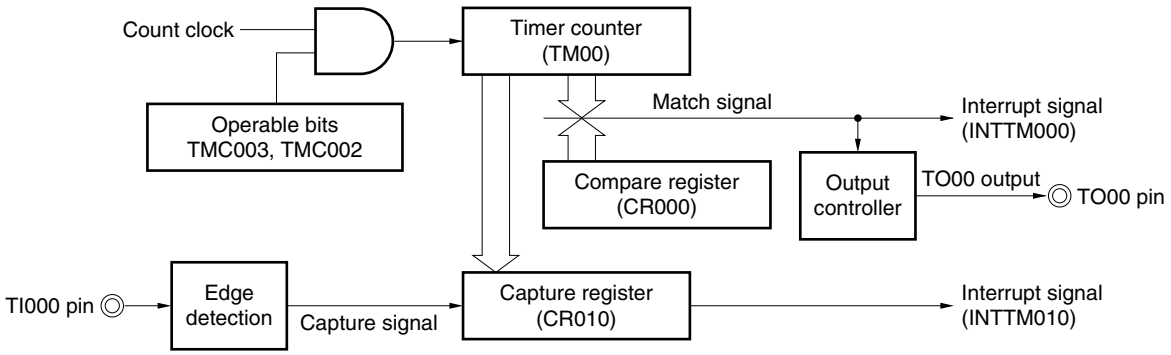


Figure 7-10. Format of 8-Bit Timer Mode Control Register 51 (TMC51) (2/2)

(b) 78K0/KB2-L, 78K0/KC2-L

Address: FF43H After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC51	TCE51	TMC516	0	0	LVS51	LVR51	TMC511	TOE51

TCE51	TM51 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC516	TM51 operating mode selection
0	Mode in which clear & start occurs on a match between TM51 and CR51
1	PWM (free-running) mode

LVS51	LVR51	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO51 output: low)
1	0	Timer output F/F set (1) (default value of TO51 output: high)
1	1	Setting prohibited

TMC511	In other modes (TMC516 = 0)	In PWM mode (TMC516 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

TOE51	Timer output control
0	Output disabled (TO51 output is low level)
1	Output enabled

Note Bits 2 and 3 are write-only.

Cautions 1. The settings of LVS51 and LVR51 are valid in other than PWM mode.

2. Perform <1> to <4> below in the following order, not at the same time.

<1> Set TMC511, TMC516: Operation mode setting

<2> Set TOE51 to enable output: Timer output enable

<3> Set LVS51, LVR51 (refer to Caution 1): Timer F/F setting

<4> Set TCE51

3. When TCE51 = 1, setting the other bits of TMC51 is prohibited.

4. The actual TO51/TI51/P33/INTP4 pin output is determined depending on PM33 and P33 besides TO51 output.

Remarks 1. In PWM mode, PWM output is made inactive by clearing TCE51 to 0.

2. If LVS51 and LVR51 are read, the value is 0.

3. The values of the TMC516, LVS51, LVR51, TMC511, and TOE51 bits are reflected at the TO51 output regardless of the value of TCE51.

<R>**(3) Port alternate switch control register (MUXSEL) (78K0/KA2-L (25-pin) only)**

MUXSEL of 78K0/KA2-L (25-pin products) assigns TOH1, TI51, TI000, and INTP0 pins. By default, INTP0 and TI000 are assigned to P00, while TI51 and TOH1 have no assignment setting.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears MUXSEL to 00H.

Figure 7-11. Format of Port Alternate Switch Control Register (MUXSEL)

Address: FF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
MUXSEL	0	INTP0SEL0	0	TM00SEL0	TM5SEL1	TM5SEL0	TMHSEL1	TMHSEL0

TM5SEL1	TM5SEL0	8-bit timer 51 input (TI51) pin function assignment
0	0	No TI51 function assignment.
0	1	Assign TI51 to the P34 pin as the alternate function.
1	0	Assign TI51 to the P00 pin as the alternate function.
1	1	Setting prohibited

<R>**(4) Port mode registers 0, 1, 3 (PM0, PM1, PM3)**

These registers set port 0, 1, and 3 input/output in 1-bit units.

PM0, PM1, and PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

• 78K0/KY2-L, 78K0/KA2-L (20-pin products)

When using the P30/TI51/TOH1/INTP1 pin for timer input, set PM30 to 1. The output latches of P30 at this time may be 0 or 1.

• 78K0/KA2-L (25-pin products)

When using the P34/TI51/TOH1/INTP4 pin for timer input, set PM34 to 1. The output latches of P34 at this time may be 0 or 1.

When using the P00/TI51/TOH1/INTP0/TI000 pin for timer input, set PM00 to 1. The output latches of P00 at this time may be 0 or 1.

• 78K0/KB2-L, 78K0/KC2-L

When using the P17/TO50/TI50 and P33/TO51/TI51/INTP4 pins for timer output, clear PM17 and PM33 and the output latches of P17 and P33 to 0.

When using the P17/TO50/TI50 and P33/TO51/TI51/INTP4 pins for timer input, set PM17 and PM33 to 1. The output latches of P17 and P33 at this time may be 0 or 1.

The peripheral functions used in the LIN communication operation are shown below.

<Peripheral functions used>

- External interrupt (INTP0); wakeup signal detection
  Use: Detects the wakeup signal edges and detects start of communication.
- 16-bit timer/event counter 00 (TI000); baud rate error detection
  Use: Detects the baud rate error (measures the TI000 input edge interval in the capture mode) by detecting the sync field (SF) length and divides it by the number of bits.
- Serial interface UART6

14.2 Configuration of Serial Interface UART6

Serial interface UART6 includes the following hardware.

Table 14-1. Configuration of Serial Interface UART6

Item	Configuration
Registers	Receive buffer register 6 (RXB6) Receive shift register 6 (RXS6) Transmit buffer register 6 (TXB6) Transmit shift register 6 (TXS6)
Control registers	Asynchronous serial interface operation mode register 6 (ASIM6) Asynchronous serial interface reception error status register 6 (ASIS6) Asynchronous serial interface transmission status register 6 (ASIF6) Clock selection register 6 (CKSR6) Baud rate generator control register 6 (BRGC6) Asynchronous serial interface control register 6 (ASICL6) Input switch control register (ISC) Port mode register 1 (PM1), port mode register 6 (PM6)Note 1 Port register 1 (P1), port register 6 (P6)Note 1 Port output mode register 6 (POM6) Note 2

Notes 1. 78K0/KY2-L, 78K0/KA2-L: Port mode register 6 (PM6), port register 6 (P6)
78K0/KB2-L, 78K0/KC2-L: Port mode register 1 (PM1), port register 1 (P1)

2. In the 78K0/KY2-L and 78K0/KA2-L, this register is used when using serial interface UART6.

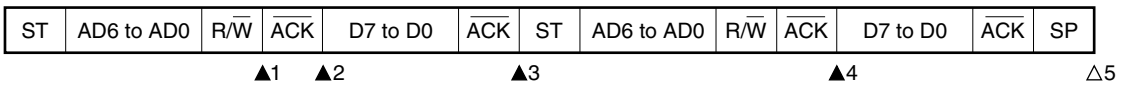
(d) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, does not match address (= not extension code))

▲1: IICAS0 = 00100010B
▲2: IICAS0 = 00100000B
▲3: IICAS0 = 00000110B
△4: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, does not match address (= not extension code))



▲1: IICAS0 = 00100010B
▲2: IICAS0 = 00100110B
▲3: IICAS0 = 00100×00B
▲4: IICAS0 = 00000110B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

16.2 Configuration of Serial Interfaces CSI10 and CSI11

Serial interfaces CSI10 and CSI11 include the following hardware.

Table 16-1. Configuration of Serial Interfaces CSI10 and CSI11

Item	Configuration
Controller	Transmit controller Clock start/stop controller & clock phase controller
Registers	Transmit buffer register 1n (SOTB1n) Serial I/O shift register 1n (SIO1n)
Control registers	Serial operation mode register 1n (CSIM1n) Serial clock selection register 1n (CSIC1n) Port alternate switch control register (MUXSEL) Port mode register x (PMx) Port register x (Px)

Remark 78K0/KA2-L (25 pins, 32 pins): n = 1, x = 0, 3
78K0/KB2-L: n = 0, x = 1
78K0/KC2-L: n = 0, 1, x = 1, 4, 6, 12

Figure 16-1. Block Diagram of Serial Interface CSI10 (78K0/KB2-L and 78K0/KC2-L)

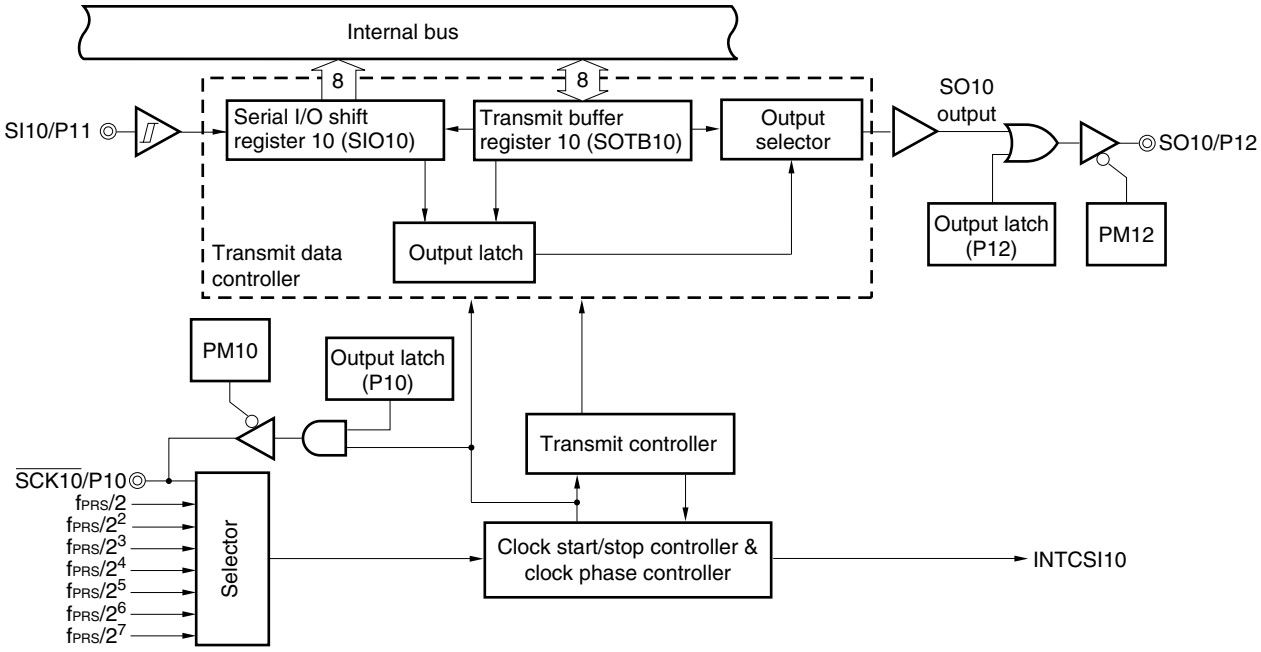


Figure 20-2. Timing of Reset by $\overline{\text{RESET}}$ Input

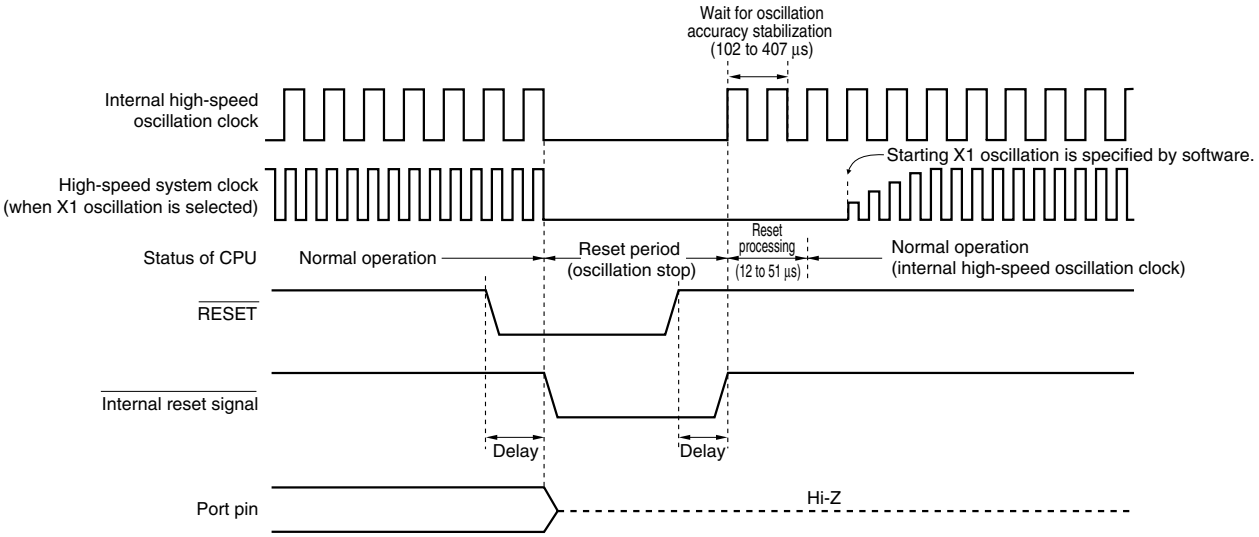
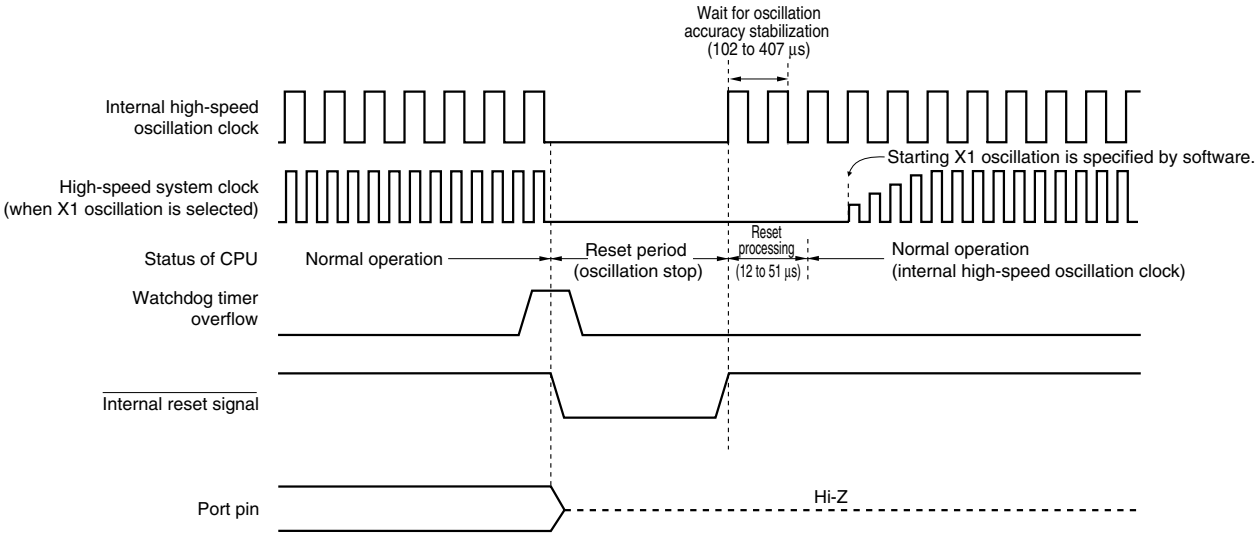


Figure 20-3. Timing of Reset Due to Watchdog Timer Overflow



Caution A watchdog timer internal reset resets the watchdog timer.

Table 20-2. Hardware Statuses After Reset Acknowledgment (4/4)

Hardware		Status After Reset Acknowledgment[Note 1]
Reset function	Reset control flag register (RESF)	00H[Note 2]
Low-voltage detector	Low-voltage detection register (LVIM)	00H[Note 2]
	Low-voltage detection level selection register (LVIS)	00H[Note 2]
Interrupt	Request flag registers 0L, 0H, 1L, 1H (IF0L, IF0H, IF1L, IF1H)	00H
	Mask flag registers 0L, 0H, 1L, 1H (MK0L, MK0H, MK1L, MK1H)	FFH
	Priority specification flag registers 0L, 0H, 1L, 1H (PR0L, PR0H, PR1L, PR1H)	FFH
	External interrupt rising edge enable registers 0, 1 (EGPCTL0, EGPCTL1)	00H
	External interrupt falling edge enable registers 0, 1 (EGNCTL0, EGNCTL1)	00H
Regulator	Regulator mode control register (RMC)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

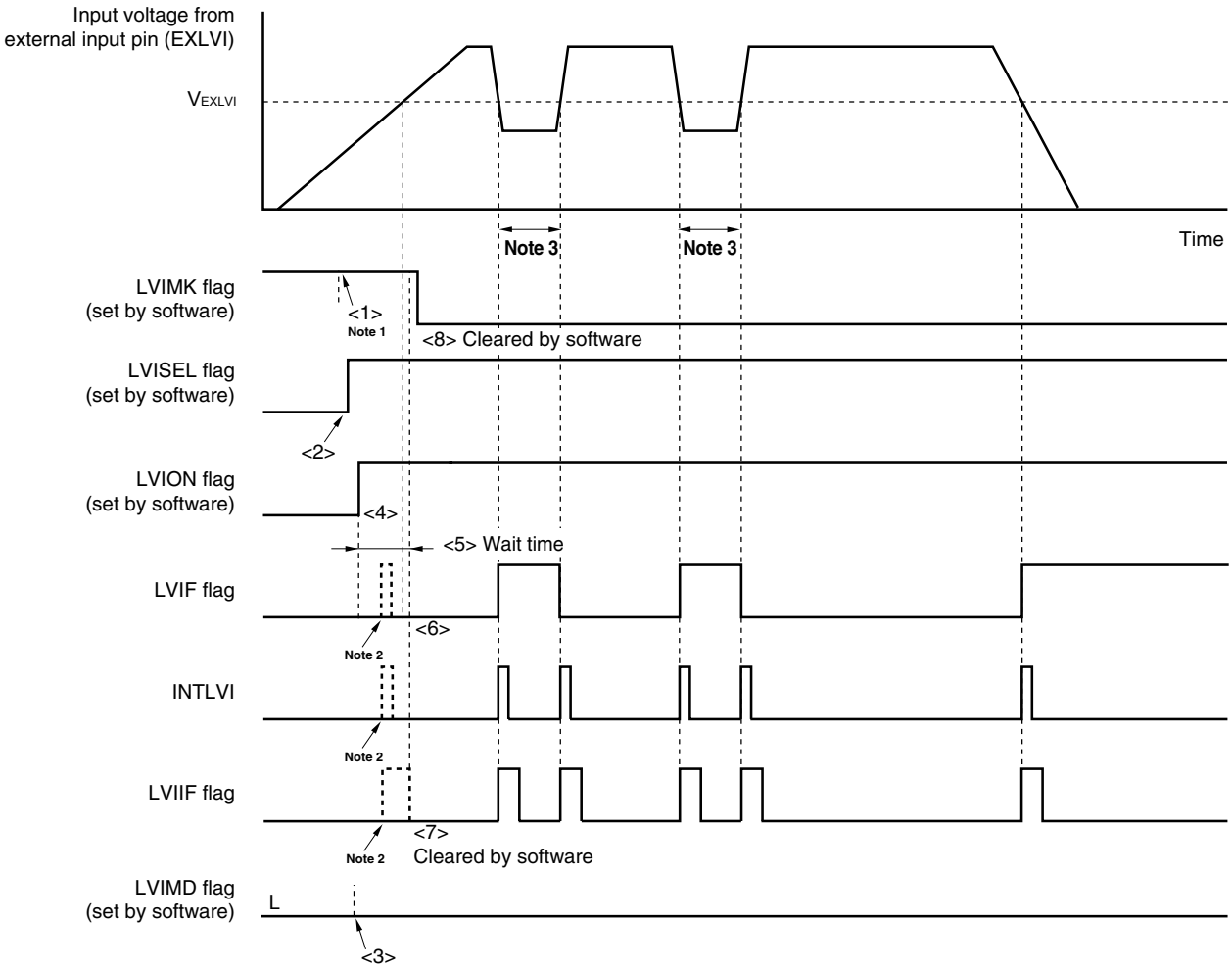
2. These values vary depending on the reset source.

<R>

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI (Except Reset by LVI Default Start Function)	Reset by LVI Default Start Function
RESF	WDTRF flag	Cleared (0)	Cleared (0)	Set (1)	Held	Cleared (0)
	LVIRF flag			Held	Set (1)	
LVIM		Cleared (00H)	Cleared (00H)	Cleared (00H)	Held	Cleared (00H)
LVIS						

Remark The special function registers (SFRs) mounted depend on the product. Refer to **3.2.3 Special function registers (SFRs)**.

Figure 22-10. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVI operation is disabled when the input voltage of external input pin (EXLVI) is less than or equal to the detection voltage (V_{EXLVI}), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

Remark <1> to <8> in Figure 22-10 above correspond to <1> to <8> in the description of "When starting operation" in **22.4.2 (2) When detecting level of input voltage from external input pin (EXLVI)**.

Table 25-9. Processing Time for Each Command When PG-FP5 Is Used (Reference) (2/3)

(1) 78K0/KY2-L, 78K0/KA2-L (2/2)

(c) Products with internal ROMs of the 16 KB: μPD78F0552, 78F0557, 78F0562, 78F0567

Command of PG-FP5	Port: UART-Internal-OSC (Internal high-speed oscillation clock (f_{IH}: 8 MHz (typ.)), Speed: 500,000 bps
Signature	0.5 s (typ.)
Blankcheck	0.5 s (typ.)
Erase	1 s (typ.)
Program	2.5 s (typ.)
Verify	1.5 s (typ.)
E.P.V	2.5 s (typ.)
Checksum	1 s (typ.)
Security	0.5 s (typ.)

(2) 78K0/KB2-L, 78K0/KC2-L (1/2)

(a) Products with internal ROMs of the 8 KB: μPD78F0571, 78F0576, 78F0581, 78F0586

Command of PG-FP5	Port: UART-Internal-OSC (Internal high-speed oscillation clock (f_{IH}: 8 MHz (typ.)), Speed: 500,000 bps
Signature	0.5 s (typ.)
Blankcheck	1 s (typ.)
Erase	1 s (typ.)
Program	1.5 s (typ.)
Verify	1 s (typ.)
E.P.V	1.5 s (typ.)
Checksum	1 s (typ.)
Security	1 s (typ.)

Caution When executing boot swapping, do not use the E.P.V. command with the dedicated flash memory programmer.

Table 26-1. On-Chip Debug Security ID

Address	On-Chip Debug Security ID
0085H to 008EH	Any ID code of 10 bytes
1085H to 108EH	

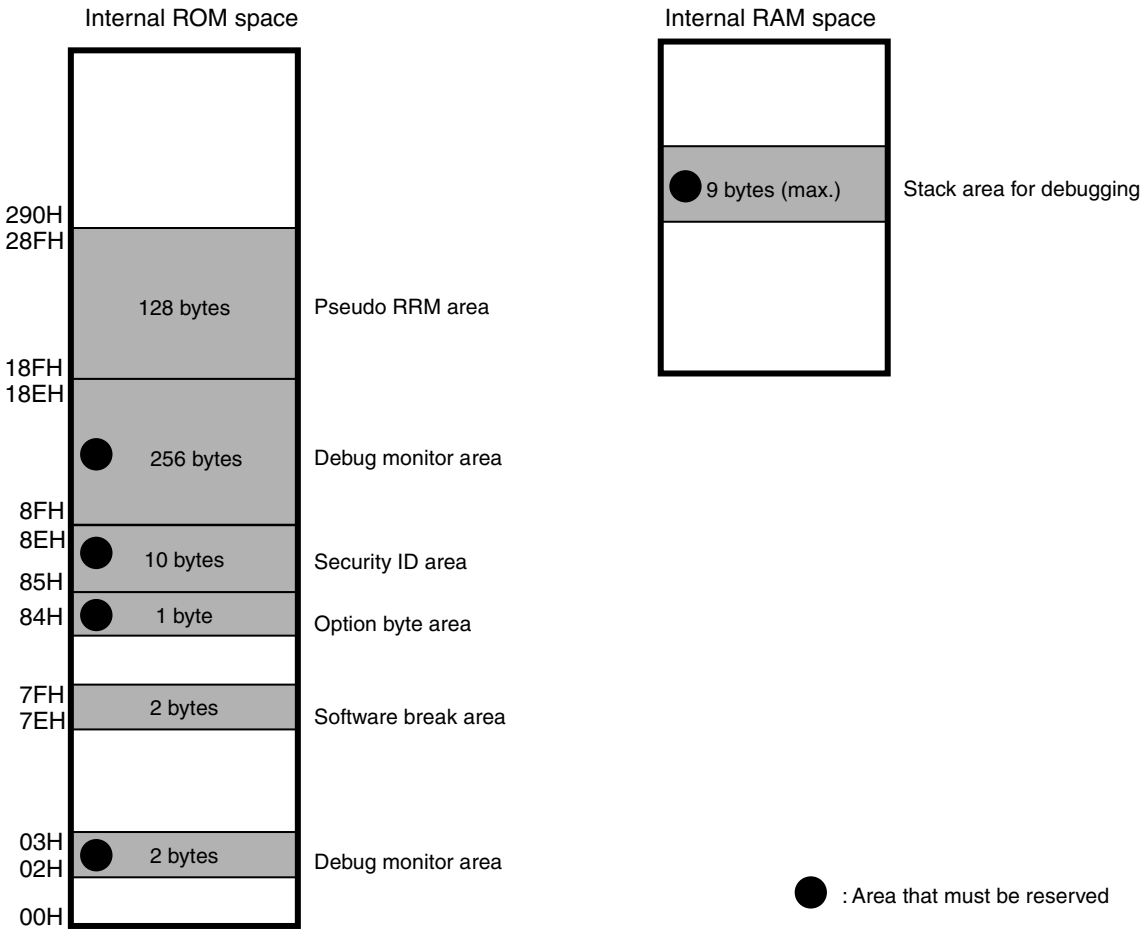
26.3 Securing of User Resources

QB-MINI2 uses the user memory spaces (shaded portions in Figure 26-2) to implement communication with the target device, or each debug functions. The areas marked with a dot (•) are always used for debugging, and other areas are used for each debug function used.

These areas can be secured by using user programs or the linker option.

For details on the securing of these areas, refer to the **QB-MINI2 On-Chip Debug Emulator with Programming Function User's Manual (U18371E)**.

Figure 26-2. Reserved Area Used by QB-MINI2



(4/4)

Page	Description	Classification
CHAPTER 25 FLASH MEMORY		
p.712	Change of **Remark** in **25.8 Flash Memory Programming by Self Programming**	(e)
CHAPTER 26 ON-CHIP DEBUG FUNCTION		
p.718	Addition of **Caution 2** in **26.1 Connecting QB-MINI2 to 78K0/Kx2-L Microcontrollers**	(c)
p.720	Addition of **Figure 26-1. Connection Example of QB-MINI2 and 78K0/Ix2 Microcontrollers (2/3)**	(c)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents