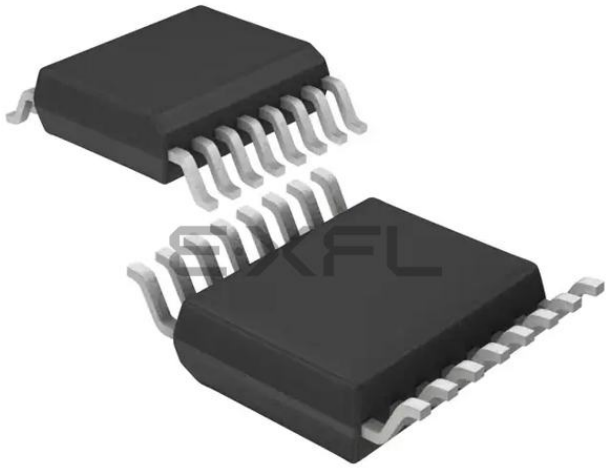
Renesas Electronics America Inc - UPD78F0556MA-FAA-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	9
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0556ma-faa-ax

<R>1.2 Ordering Information

[Part Number]

μPD78F05 x y ΔΔ - ××× -AX

	Semiconductor	
-AX	Lead-free	Product contains no lead in any area (Terminal finish is Ni/Pd/Au plating)

x	ΔΔ - ×××	Package Type
5	MA-FAA	16-pin plastic SSOP (5.72 mm (225))
6	MC-CAA	20-pin plastic SSOP (7.62 mm (300))
	FC-2N2	25-pin plastic FLGA (3x3)
	K8-3B4	32-pin plastic WQFN (5x5)
7	MC-CAB	30-pin plastic SSOP (7.62 mm (300))
8	K8-4B4	40-pin plastic WQFN (6x6)
	GB-GAF	44-pin plastic LQFP (10x10)
	GA-GAM	48-pin plastic LQFP (fine pitch) (7x7)

y	Flash Memory Capacity	High-speed RAM Capacity	Operational amplifier
0	4 KB	384 bytes	Not mounted
1	8 KB	512 bytes	
2	16 KB	768 bytes	
3	32 KB	1 KB	
5	4 KB	384 bytes	Mounted
6	8 KB	512 bytes	
7	16 KB	768 bytes	
8	32 KB	1 KB	

	Product Type
F	Flash memory version

[Example of Part Number]

μPD78F05 5 0 MA-FAA -AX

- Lead-free
- 16-pin plastic SSOP (5.72 mm)
- High-speed RAM: 384 bytes, flash memory: 4 KB, operational amplifier: not mounted
- Flash memory version

(e) SO10

This is a serial data output pin of serial interface CSI10.

(f) $\overline{\text{SCK10}}$

This is a serial clock I/O pin of serial interface CSI10.

(g) RxD6

This is a serial data input pin of serial interface UART6.

(h) TxD6

This is a serial data output pin of serial interface UART6.

(i) TI50

This is a pin for inputting an external count clock to 8-bit timer/event counter 50.

(j) TO50

This is a timer output pin of 8-it timer/event counter 50.

(k) TOH0, TOH1

These are a timer output pins of 8-bit timers H0 and H1.

(l) INTP5

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

2.2.3 P20 to P27 (port 2)

P20 to P27 function as an I/O port. These pins also function as pins for A/D converter analog input, operational amplifier I/O, and PGA input.

<R>

78K0/KY2-L (μPD78F055x)	78K0/KA2-L (μPD78F056x)			78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)		
16 Pins	20 Pins	25 Pins	32 Pins	30 Pins	40 Pins	44 Pins	48 Pins
P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note
P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote
P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note
P23/ANI3	P23/ANI3	P23/ANI3	P23/ANI3	P23/ANI3	P23/ANI3	P23/ANI3	P23/ANI3
–	P24/ANI4	P24/ANI4	P24/ANI4	–	P24/ANI4	P24/ANI4	P24/ANI4
–	P25/ANI5	P25/ANI5	P25/ANI5	–	P25/ANI5	P25/ANI5	P25/ANI5
–	–	P26/ANI6	P26/ANI6	–	P26/ANI6	P26/ANI6	P26/ANI6
–	–	–	P27/ANI7	–	–	P27/ANI7	P27/ANI7

Note Products with operational amplifier only

The following operation modes can be specified in 1-bit units.

Table 3-9. Special Function Register List: 78K0/KB2-L (3/5)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF4CH to FF4EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF4FH	ISC	0	0	0	0	0	0	ISC1	ISC0	R/W	√	√	–	00H	463
FF50H	ASIM6	<POWER6>	<TXE6>	<RXE6>	PS61	PS60	CL6	SL6	ISRM6	R/W	√	√	–	01H	454
FF51H FF52H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF53H	ASIS6	0	0	0	0	0	PE6	FE6	OVE6	R	–	√	–	00H	457
FF54H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF55H	ASIF6	0	0	0	0	0	0	TXBF6	TXSF6	R	–	√	–	00H	458
FF56H	CKSR6	0	0	0	0	TPS63	TPS62	TPS61	TPS60	R/W	–	√	–	00H	458
FF57H	BRGC6	MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60	R/W	–	√	–	FFH	460
FF58H	ASICL6	<SBRF6>	<SBRT6>	SBTT6	SBL62	SBL61	SBL60	DIR6	TXDLV6	R/W	√	√	–	16H	461
FF59H to FF5FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF60H	AMP0M[Note]	<OPAMP0E>	<PGAEN>	0	0	0	0	AMP0VG1	AMP0VG0	R/W	√	√	–	00H	436
FF61H	AMP1M[Note]	<OPAMP1E>	0	0	0	0	0	0	0	R/W	√	√	–	00H	436
FF62H to FF68H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF69H	TMHMD0	<TMHE0>	CKS02	CKS01	CKS00	TMMD01	TMMD00	<TOLEV0>	<TOEN0>	R/W	√	√	–	00H	339
FF6AH	TCL50	0	0	0	0	0	TCL502	TCL501	TCL500	R/W	√	√	–	00H	318
FF6BH	TMC50	<TCE50>	TMC506	0	0	<LVS50>	<LVR50>	TMC501	<TOE50>	R/W	√	√	–	00H	320
FF6CH	TMHMD1	<TMHE1>	CKS12	CKS11	CKS10	TMMD11	TMMD10	<TOLEV1>	<TOEN1>	R/W	√	√	–	00H	339
FF6DH	TMCYC1	0	0	0	0	0	RMC1	NRZB1	<NRZ1>	R/W	√	√	–	00H	343
FF6EH to FF7FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF80H	CSIM10	<CSIE10>	TRMD10	0	DIR10	0	0	0	CSOT10	R/W	√	√	–	00H	566
FF81H	CSIC10	0	0	0	CKP10	DAP10	CKS102	CKS101	CKS100	R/W	√	√	–	00H	569
FF82H FF83H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF84H	SOTB10	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	565

Note These registers are incorporated only in products with operational amplifier.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

(3) Example of setting procedure when using the subsystem clock as the CPU clock

<1> Setting subsystem clock oscillation[Note]

(Refer to **5.6.3 (1) Example of setting procedure when oscillating the XT1 clock** and **(2) Example of setting procedure when using the external subsystem clock**.)

Note The setting of <1> is not necessary when while the subsystem clock is operating.

<2> Switching the CPU clock (PCC register)

When CSS is set to 1, the subsystem clock is supplied to the CPU.

CSS	PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
1	0	0	0	f_{SUB}
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
	Other than above			Setting prohibited

(4) Example of setting procedure when stopping the subsystem clock

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the subsystem clock.

When CLS = 1, the subsystem clock is supplied to the CPU, so change the CPU clock to a clock other than the subsystem clock.

CLS	MCS	CPU Clock Status
0	0	Internal high-speed oscillation clock
0	1	High-speed system clock
1	×	Subsystem clock

<2> Stopping the subsystem clock (OSCCTL register)

When OSCSELS is cleared to 0, XT1 oscillation is stopped (the input of the external clock is disabled).

Cautions 1. Be sure to confirm that CLS = 0 when clearing OSCSELS to 0. In addition, stop the watch timer if it is operating on the subsystem clock.

2. The subsystem clock oscillation cannot be stopped using the STOP instruction.

Figure 6-5. Format of 16-Bit Timer Mode Control Register 00 (TMC00)

Address: FFBAH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
TMC00	0	0	0	0	TMC003	TMC002	TMC001	OVF00

TMC003	TMC002	Operation enable of 16-bit timer/event counter 00
0	0	Disables 16-bit timer/event counter 00 operation. Stops supplying operating clock. Clears 16-bit timer counter 00 (TM00).
0	1	Free-running timer mode
1	0	Clear & start mode entered by TI000 pin valid edge input[Note]
1	1	Clear & start mode entered upon a match between TM00 and CR000

TMC001	Condition to reverse timer output (TO00)
0	• Match between TM00 and CR000 or match between TM00 and CR010
1	• Match between TM00 and CR000 or match between TM00 and CR010 • Trigger input of TI000 pin valid edge

OVF00	TM00 overflow flag
Clear (0)	Clears OVF00 to 0 or TMC003 and TMC002 = 00
Set (1)	Overflow occurs.
OVF00 is set to 1 when the value of TM00 changes from FFFFH to 0000H in all the operation modes (free-running timer mode, clear & start mode entered by TI000 pin valid edge input, and clear & start mode entered upon a match between TM00 and CR000). It can also be set to 1 by writing 1 to OVF00.	

Note The TI000 pin valid edge is set by bits 5 and 4 (ES010, ES000) of prescaler mode register 00 (PRM00).

(2) Capture/compare control register 00 (CRC00)

CRC00 is the register that controls the operation of CR000 and CR010.

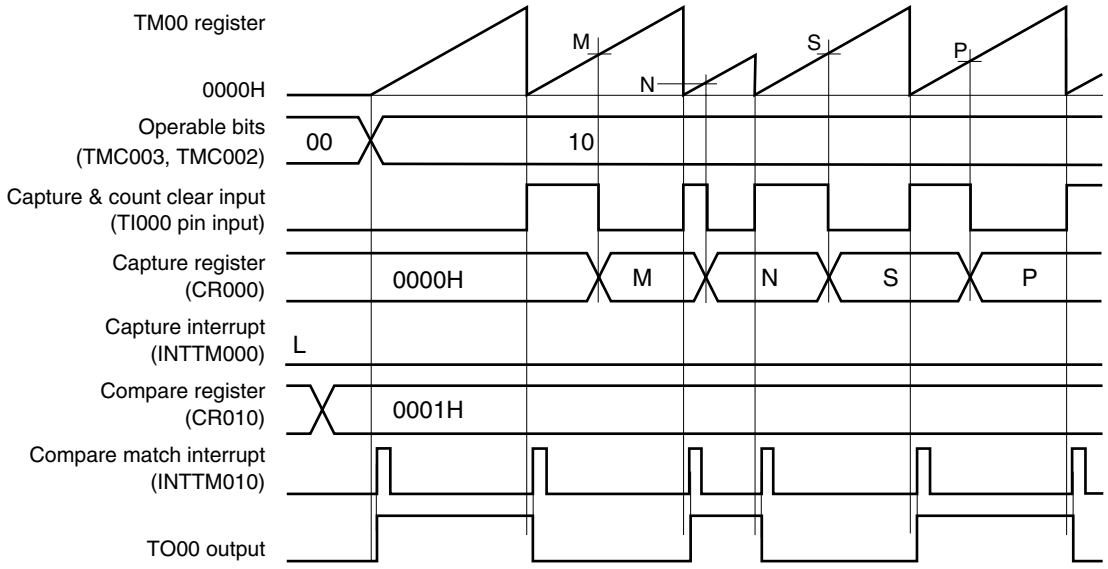
Changing the value of CRC00 is prohibited during operation (when TMC003 and TMC002 = other than 00).

CRC00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CRC00 to 00H.

Figure 6-28. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register) (1/2)

(a) TOC00 = 13H, PRM00 = 10H, CRC00 = 03H, TMC00 = 08H, CR010 = 0001H



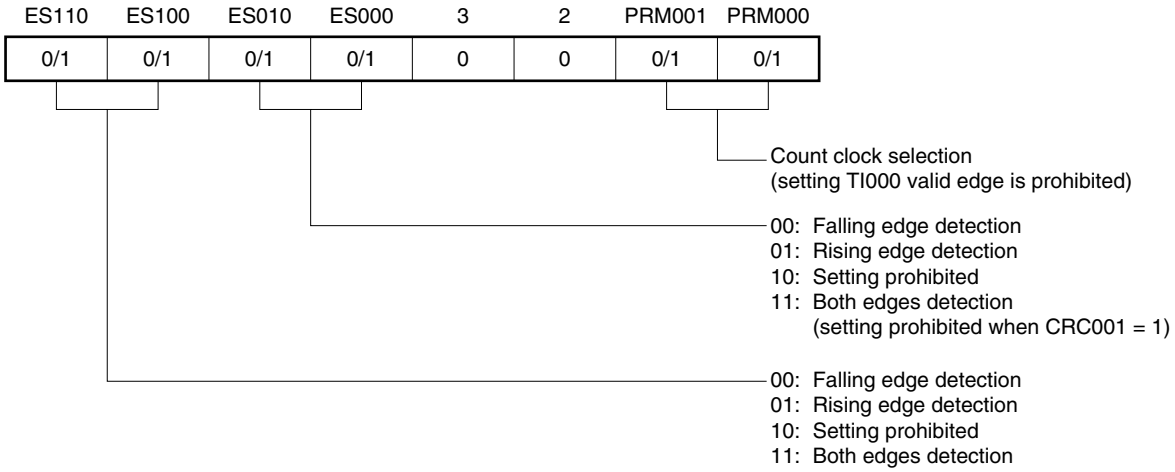
This is an application example where the TO00 output level is to be inverted when the count value has been captured & cleared.

TM00 is cleared at the rising edge detection of the TI000 pin and it is captured to CR000 at the falling edge detection of the TI000 pin.

When bit 1 (CRC001) of capture/compare control register 00 (CRC00) is set to 1, the count value of TM00 is captured to CR000 in the phase reverse to that of the signal input to the TI000 pin, but the capture interrupt signal (INTTM000) is not generated. However, the INTTM000 signal is generated when the valid edge of the TI010 pin is detected. Mask the INTTM000 signal when it is not used.

Figure 6-39. Example of Register Settings in Free-Running Timer Mode (2/2)

(d) Prescaler mode register 00 (PRM00)



(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM000) is generated. The count value of TM00 is not cleared.

To use this register as a capture register, select either the TI000 or TI010 pin input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR000.

(g) 16-bit capture/compare register 010 (CR010)

When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM010) is generated. The count value of TM00 is not cleared.

When this register is used as a capture register, the TI000 pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR010.

(12) Reading of 16-bit timer counter 00 (TM00)

TM00 can be read without stopping the actual counter, because the count values captured to the buffer are fixed when it is read. The buffer, however, may not be updated when it is read immediately before the counter counts up, because the buffer is updated at the timing the counter counts up.

Figure 6-59. 16-bit Timer Counter 00 (TM00) Read Timing

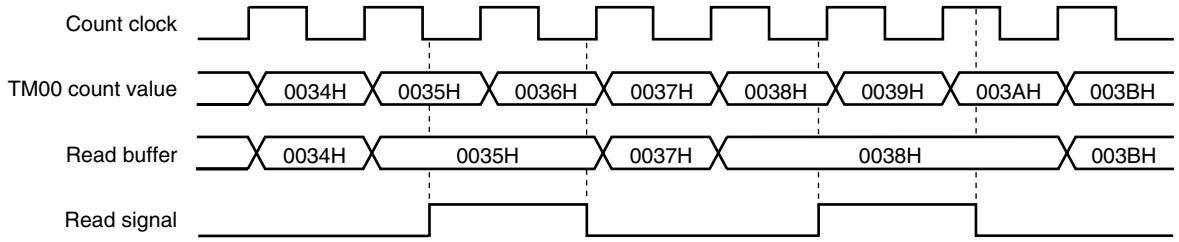


Figure 7-10. Format of 8-Bit Timer Mode Control Register 51 (TMC51) (2/2)

(b) 78K0/KB2-L, 78K0/KC2-L

Address: FF43H After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC51	TCE51	TMC516	0	0	LVS51	LVR51	TMC511	TOE51

TCE51	TM51 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC516	TM51 operating mode selection
0	Mode in which clear & start occurs on a match between TM51 and CR51
1	PWM (free-running) mode

LVS51	LVR51	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO51 output: low)
1	0	Timer output F/F set (1) (default value of TO51 output: high)
1	1	Setting prohibited

TMC511	In other modes (TMC516 = 0)	In PWM mode (TMC516 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

TOE51	Timer output control
0	Output disabled (TO51 output is low level)
1	Output enabled

Note Bits 2 and 3 are write-only.

Cautions 1. The settings of LVS51 and LVR51 are valid in other than PWM mode.

2. Perform <1> to <4> below in the following order, not at the same time.

<1> Set TMC511, TMC516: Operation mode setting

<2> Set TOE51 to enable output: Timer output enable

<3> Set LVS51, LVR51 (refer to Caution 1): Timer F/F setting

<4> Set TCE51

3. When TCE51 = 1, setting the other bits of TMC51 is prohibited.

4. The actual TO51/TI51/P33/INTP4 pin output is determined depending on PM33 and P33 besides TO51 output.

Remarks 1. In PWM mode, PWM output is made inactive by clearing TCE51 to 0.

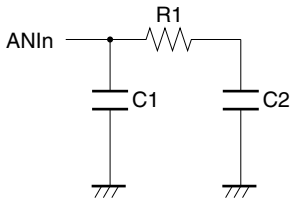
2. If LVS51 and LVR51 are read, the value is 0.

3. The values of the TMC516, LVS51, LVR51, TMC511, and TOE51 bits are reflected at the TO51 output regardless of the value of TCE51.

(11) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 12-24. Internal Equivalent Circuit of ANIn Pin



<R> **Table 12-9. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)**

AV_{REF}	Mode	R1	C1	C2
4.0 V ≤ AV_{REF} ≤ 5.5 V	Standard	5.2 kΩ	8 pF	6.3 pF
	High-speed 2	7.8 kΩ		
	High-speed 1	5.2 kΩ		
2.7 V ≤ AV_{REF} < 4.0 V	Standard	18.6 kΩ		
	High-speed 2	7.8 kΩ		
1.8 V ≤ AV_{REF} < 4.0 V	Low-voltage	169.8 kΩ		

Remarks 1. The resistance and capacitance values shown in Table 12-9 are not guaranteed values.

2. n = 0 to 10 (it depends on products)

Figure 13-8. Format of Port Mode Register 2 (PM2)

(a) 78K0/KY2-L

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

Caution Be sure to set bits 4 to 7 of PM2 to 1.

<R>**(b) 78K0/KA2-L**

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27 Note 1	PM26 Note 2	PM25	PM24	PM23	PM22	PM21	PM20

Notes 1. 32-pin products only

2. 25-pin and 32-pin products only

(c) 78K0/KB2-L

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

<R>**(d) 78K0/KC2-L**

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27 Note	PM26	PM25	PM24	PM23	PM22	PM21	PM20

Note 44-pin and 48-pin products only

PM2n	P2n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(d) Continuous transmission

The next transmit data can be written to transmit buffer register 6 (TXB6) as soon as transmit shift register 6 (TXS6) has started its shift operation. Consequently, even while the INTST6 interrupt is being serviced after transmission of one data frame, data can be continuously transmitted and an efficient communication rate can be realized. In addition, the TXB6 register can be efficiently written twice (2 bytes) without having to wait for the transmission time of one data frame, by reading bit 0 (TXSF6) of asynchronous serial interface transmission status register 6 (ASIF6) when the transmission completion interrupt has occurred.

To transmit data continuously, be sure to reference the ASIF6 register to check the transmission status and whether the TXB6 register can be written, and then write the data.

Cautions 1. The TXBF6 and TXSF6 flags of the ASIF6 register change from "10" to "11", and to "01" during continuous transmission. To check the status, therefore, do not use a combination of the TXBF6 and TXSF6 flags for judgment. Read only the TXBF6 flag when executing continuous transmission.

2. When the device is use in LIN communication operation, the continuous transmission function cannot be used. Make sure that asynchronous serial interface transmission status register 6 (ASIF6) is 00H before writing transmit data to transmit buffer register 6 (TXB6).

TXBF6	Writing to TXB6 Register
0	Writing enabled
1	Writing disabled

Caution To transmit data continuously, write the first transmit data (first byte) to the TXB6 register. Be sure to check that the TXBF6 flag is "0". If so, write the next transmit data (second byte) to the TXB6 register. If data is written to the TXB6 register while the TXBF6 flag is "1", the transmit data cannot be guaranteed.

The communication status can be checked using the TXSF6 flag.

TXSF6	Transmission Status
0	Transmission is completed.
1	Transmission is in progress.

Cautions 1. To initialize the transmission unit upon completion of continuous transmission, be sure to check that the TXSF6 flag is "0" after generation of the transmission completion interrupt, and then execute initialization. If initialization is executed while the TXSF6 flag is "1", the transmit data cannot be guaranteed.

2. During continuous transmission, the next transmission may complete before execution of INTST6 interrupt servicing after transmission of one data frame. As a countermeasure, detection can be performed by developing a program that can count the number of transmit data and by referencing the TXSF6 flag.

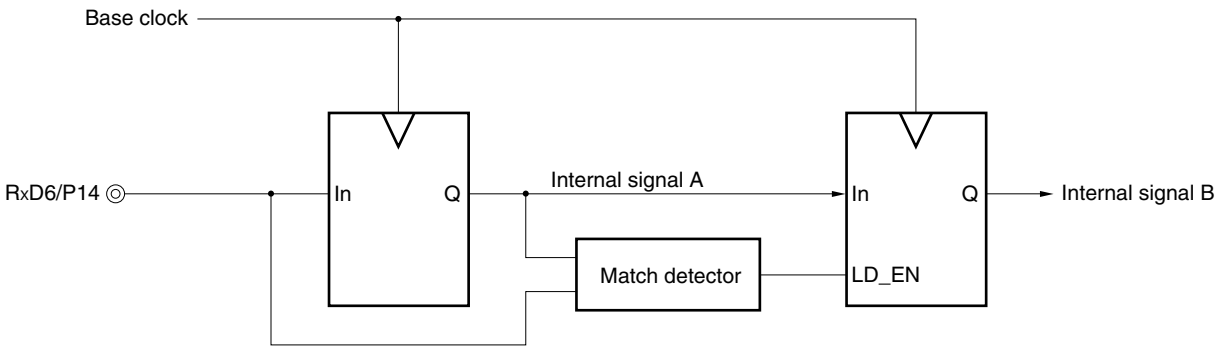
(g) Noise filter of receive data

The RxD6 signal is sampled with the base clock output by the prescaler block.

If two sampled values are the same, the output of the match detector changes, and the data is sampled as input data.

Because the circuit is configured as shown in Figure 14-23, the internal processing of the reception operation is delayed by two clocks from the external signal status.

Figure 14-23. Noise Filter Circuit



(h) SBF transmission

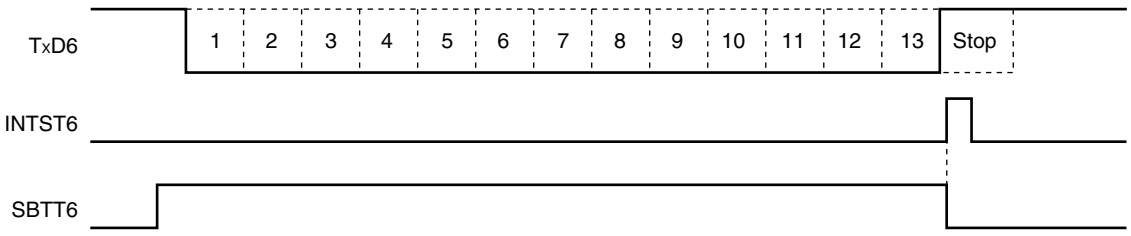
When the device is use in LIN communication operation, the SBF (Synchronous Break Field) transmission control function is used for transmission. For the transmission operation of LIN, refer to **Figure 14-1 LIN Transmission Operation**.

When bit 7 (POWER6) of asynchronous serial interface mode register 6 (ASIM6) is set to 1, the TxD6 pin outputs high level. Next, when bit 6 (TXE6) of ASIM6 is set to 1, the transmission enabled status is entered, and SBF transmission is started by setting bit 5 (SBTT6) of asynchronous serial interface control register 6 (ASICL6) to 1.

Thereafter, a low level of bits 13 to 20 (set by bits 4 to 2 (SBL62 to SBL60) of ASICL6) is output. Following the end of SBF transmission, the transmission completion interrupt request (INTST6) is generated and SBTT6 is automatically cleared. Thereafter, the normal transmission mode is restored.

Transmission is suspended until the data to be transmitted next is written to transmit buffer register 6 (TXB6), or until SBTT6 is set to 1.

Figure 14-24. SBF Transmission



Remark TxD6: TxD6 pin (output)
INTST6: Transmission completion interrupt request
SBTT6: Bit 5 of asynchronous serial interface control register 6 (ASICL6)

(i) SBF reception

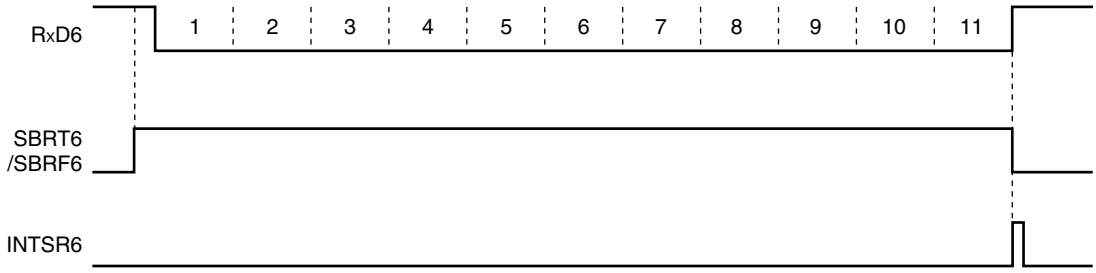
When the device is used in LIN communication operation, the SBF (Synchronous Break Field) reception control function is used for reception. For the reception operation of LIN, refer to **Figure 14-2 LIN Reception Operation**.

Reception is enabled when bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and then bit 5 (RXE6) of ASIM6 is set to 1. SBF reception is enabled when bit 6 (SBRT6) of asynchronous serial interface control register 6 (ASICL6) is set to 1. In the SBF reception enabled status, the RxD6 pin is sampled and the start bit is detected in the same manner as the normal reception enable status.

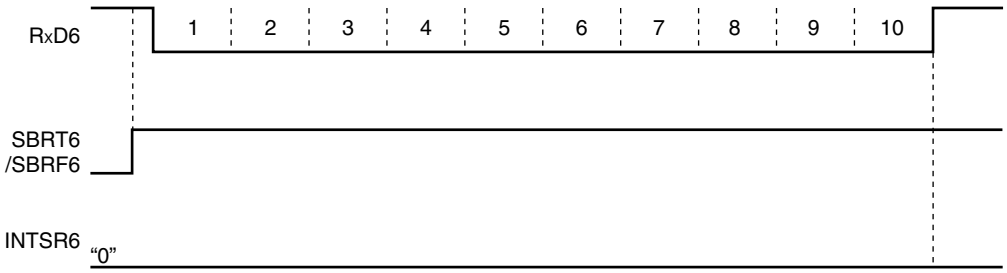
When the start bit has been detected, reception is started, and serial data is sequentially stored in the receive shift register 6 (RXS6) at the set baud rate. When the stop bit is received and if the width of SBF is 11 bits or more, a reception completion interrupt request (INTSR6) is generated as normal processing. At this time, the SBRF6 and SBRT6 bits are automatically cleared, and SBF reception ends. Detection of errors, such as OVE6, PE6, and FE6 (bits 0 to 2 of asynchronous serial interface reception error status register 6 (ASIS6)) is suppressed, and error detection processing of UART communication is not performed. In addition, data transfer between receive shift register 6 (RXS6) and receive buffer register 6 (RXB6) is not performed, and the reset value of FFH is retained. If the width of SBF is 10 bits or less, an interrupt does not occur as error processing after the stop bit has been received, and the SBF reception mode is restored. In this case, the SBRF6 and SBRT6 bits are not cleared.

Figure 14-25. SBF Reception

1. Normal SBF reception (stop bit is detected with a width of more than 10.5 bits)



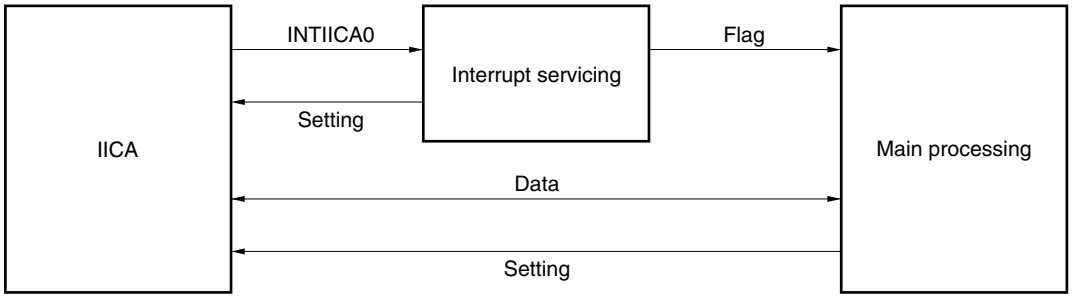
2. SBF reception error (stop bit is detected with a width of 10.5 bits or less)



Remark RxD6: RxD6 pin (input)
SBRT6: Bit 6 of asynchronous serial interface control register 6 (ASICL6)
SBRF6: Bit 7 of ASICL6
INTSR6: Reception completion interrupt request

Basically, the slave operation is event-driven. Therefore, processing by the INTIICA0 interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICA0 interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICA0.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

<2> Ready flag

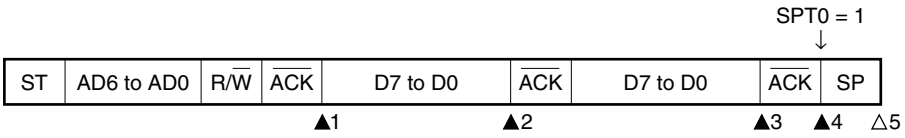
This flag indicates that data communication is enabled. Its function is the same as the INTIICA0 interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as the TRC0 bit.

(c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

(i) When WTIM0 = 0

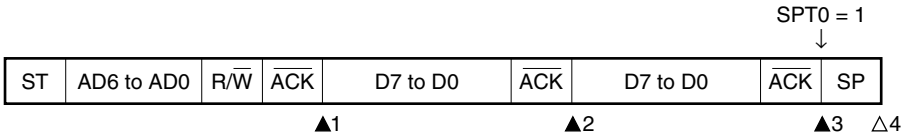


▲1: IICAS0 = 1010×110B
▲2: IICAS0 = 1010×000B
▲3: IICAS0 = 1010×000B (Sets WTIM0 to 1)[Note]
▲4: IICAS0 = 1010××00B (Sets SPT0 to 1)
△5: IICAS0 = 00000001B

Note To generate a stop condition, set WTIM0 to 1 and change the timing for generating the INTIICA0 interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1



▲1: IICAS0 = 1010×110B
▲2: IICAS0 = 1010×100B
▲3: IICAS0 = 1010××00B (Sets SPT0 to 1)
△4: IICAS0 = 00001001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(5) SO1n output (refer to Figures 16-1 to 16-3)

The status of the SO1n output is as follows depending on the setting of CSIE1n, TRMD1n, DAP1n, and DIR1n.

Table 16-3. SO1n Output Status

CSIE1n	TRMD1n	DAP1n	DIR1n	SO1n Output[Note 1]
CSIE1n = 0[Note 2]	TRMD1n = 0[Note 2]	–	–	Low level output[Note 2]
	TRMD1n = 1[Note 3]	DAP1n = 0	–	Low level output
		DAP1n = 1	DIR1n = 0	Value of bit 7 of SOTB1n
			DIR1n = 1	Value of bit 0 of SOTB1n
CSIE1n = 1	TRMD1n = 0	–	–	Low level output
	TRMD1n = 1	–	–	Transmission data[Note 4]

Notes 1. The actual output of the SO10 or SO11 pin is determined according to the port mode register and the port register corresponding to SO10 or SO11, as well as the SO1n output.

2. This is a status after reset.

3. To use the SO11 pin as general-purpose port, set CSIC11 in the default status (00H).

4. After transmission has been completed, the SO1n pin holds the output value of the last bit of transmission data.

Caution If a value is written to CSIE1n, TRMD1n, DAP1n, and DIR1n, the output value of SO1n changes.

Remark 78K0/KA2-L (25, 32-pin products): n = 1
78K0/KB2-L: n = 0
78K0/KC2-L: n = 0, 1

17.4 Interrupt Servicing Operations

17.4.1 Maskable interrupt acknowledgment

A maskable interrupt becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request (when the ISP flag is reset to 0).

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 17-4 below.

For the interrupt request acknowledgment timing, refer to **Figures 17-26** and **17-27**.

Table 17-4. Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time[Note]
When ××PR = 0	7 clocks	32 clocks
When ××PR = 1	8 clocks	33 clocks

Note If an interrupt request is generated just before a divide instruction, the wait time becomes longer.

Remark 1 clock: $1/f_{CPU}$ (f_{CPU}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

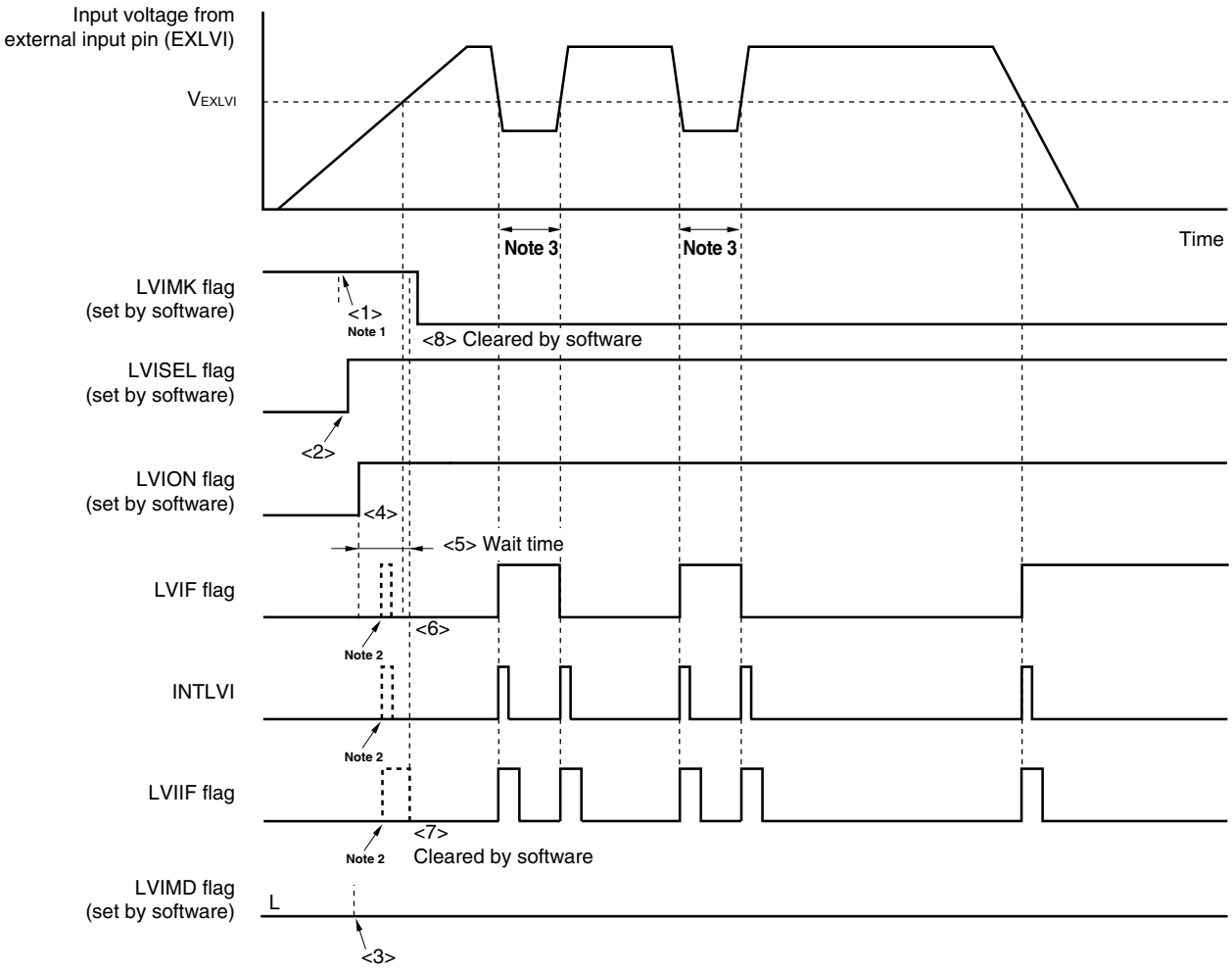
An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

Figure 17-25 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP flag. The vector table data determined for each interrupt request is the loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

Figure 22-10. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

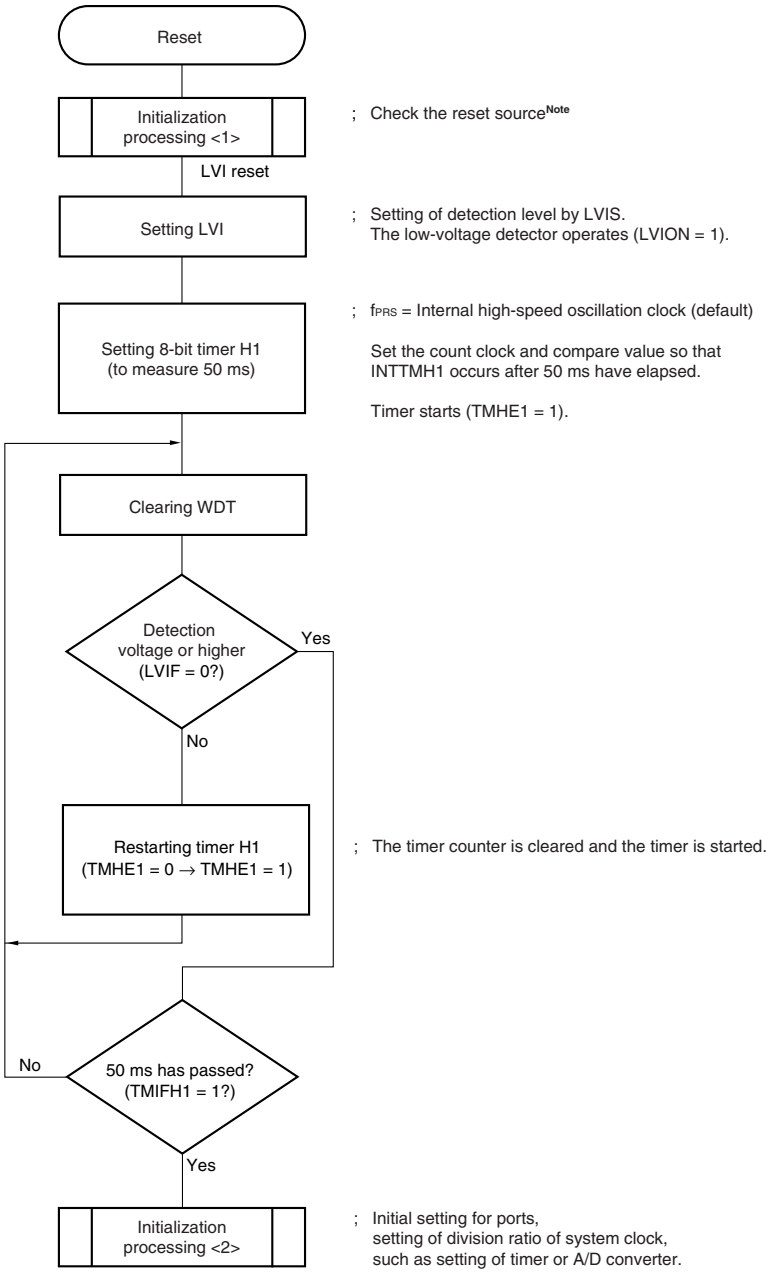
2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVI operation is disabled when the input voltage of external input pin (EXLVI) is less than or equal to the detection voltage (V_{EXLVI}), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

Remark <1> to <8> in Figure 22-10 above correspond to <1> to <8> in the description of "When starting operation" in **22.4.2 (2) When detecting level of input voltage from external input pin (EXLVI)**.

Figure 22-11. Example of Software Processing After Reset Release (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of LVI detection voltage



Note A flowchart is shown on the next page.