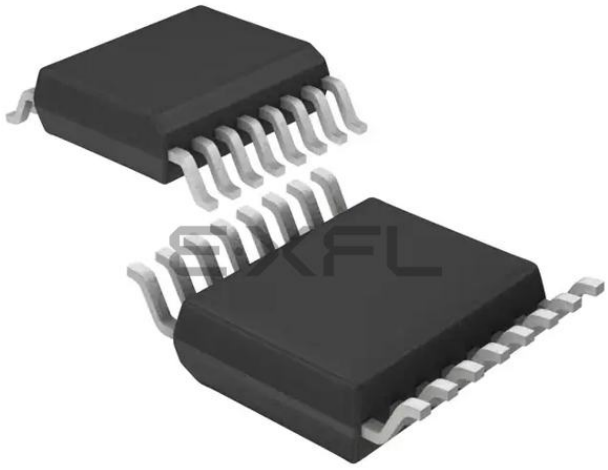
Renesas Electronics America Inc - UPD78F0557MA-FAA-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	9
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0557ma-faa-ax

Table 3-7. Special Function Register List: 78K0/KA2-L (20-pin products) (1/4)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF00H	P0	0	0	0	0	0	0	P01	P00	R/W	√	√	–	00H	172
FF01H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF02H	P2	0	0	P25	P24	P23	P22	P21	P20	R/W	√	√	–	00H	172
FF03H	P3	0	0	0	0	0	P32	P31	P30	R/W	√	√	–	00H	172
FF04H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF05H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF06H	P6	0	0	0	0	0	0	P61	P60	R/W	√	√	–	00H	172
FF07H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF08H	AD ADCRL	–	–	–	–	–	–	–	–	R	–	√	–	00H	411
FF09H	CR	0	0	0	0	0	0	–	–	R	–	–	√	0000H	410
FF0AH	RXB6	–	–	–	–	–	–	–	–	R	–	√	–	FFH	452
FF0BH	TXB6	–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	453
FF0CH	P12	0	0	P125	0	0	P122	P121	0	R	√	√	–	00H	172
FF0DH	ADCRH	–	–	–	–	–	–	–	–	R	–	√	–	00H	411
FF0EH	ADS	0	<ADOAS> Note	0	0	0	<ADS2>	<ADS1>	<ADS0>	R/W	√	√	–	00H	412, 439
FF0FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF10H	TM00	–	–	–	–	–	–	–	–	R	–	–	√	0000H	243
FF11H		–	–	–	–	–	–	–	–						
FF12H	CR000	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	244
FF13H		–	–	–	–	–	–	–	–						
FF14H	CR010	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	244
FF15H		–	–	–	–	–	–	–	–						
FF16H to FF19H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF1AH	CMP01	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	338
FF1BH	CMP11	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	338
FF1CH to FF1EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF1FH	TM51	–	–	–	–	–	–	–	–	R	–	√	–	00H	317
FF20H	PM0	1	1	1	1	1	1	PM01	PM00	R/W	√	√	–	FFH	167, 256
FF21H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF22H	PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20	R/W	√	√	–	FFH	167, 415, 440
FF23H	PM3	1	1	1	1	1	PM32	PM31	PM30	R/W	√	√	–	FFH	167, 324, 345
FF24H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF25H	–	–	–	–	–	–	–	–	–		–	–	–	–	–

Note This bit is incorporated only in products with operational amplifier.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

3.4.8 Based indexed addressing

[Function]

The B or C register contents specified in an instruction word are added to the contents of the base register, that is, the HL register pair in the register bank specified by the register bank select flag (RBS0 and RBS1), and the sum is used to address the memory. Addition is performed by expanding the B or C register contents as a positive number to 16 bits. A carry from the 16th bit is ignored.

This addressing can be carried out for all of the memory spaces.

[Operand format]

Identifier	Description
–	[HL + B], [HL + C]

[Description example]

MOV A, [HL +B]; when selecting B register

Operation code	1	0	1	0	1	0	1	1

[Illustration]

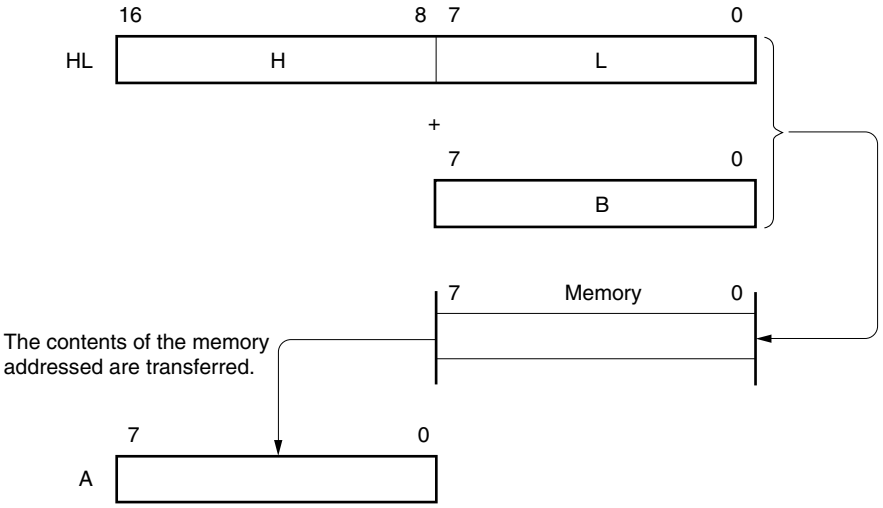
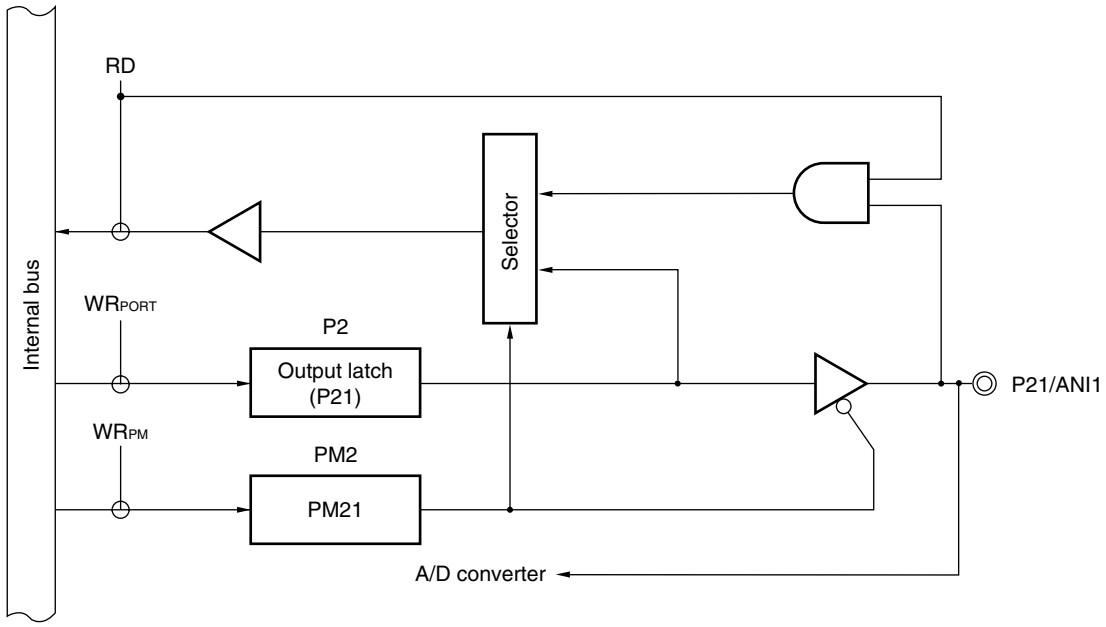
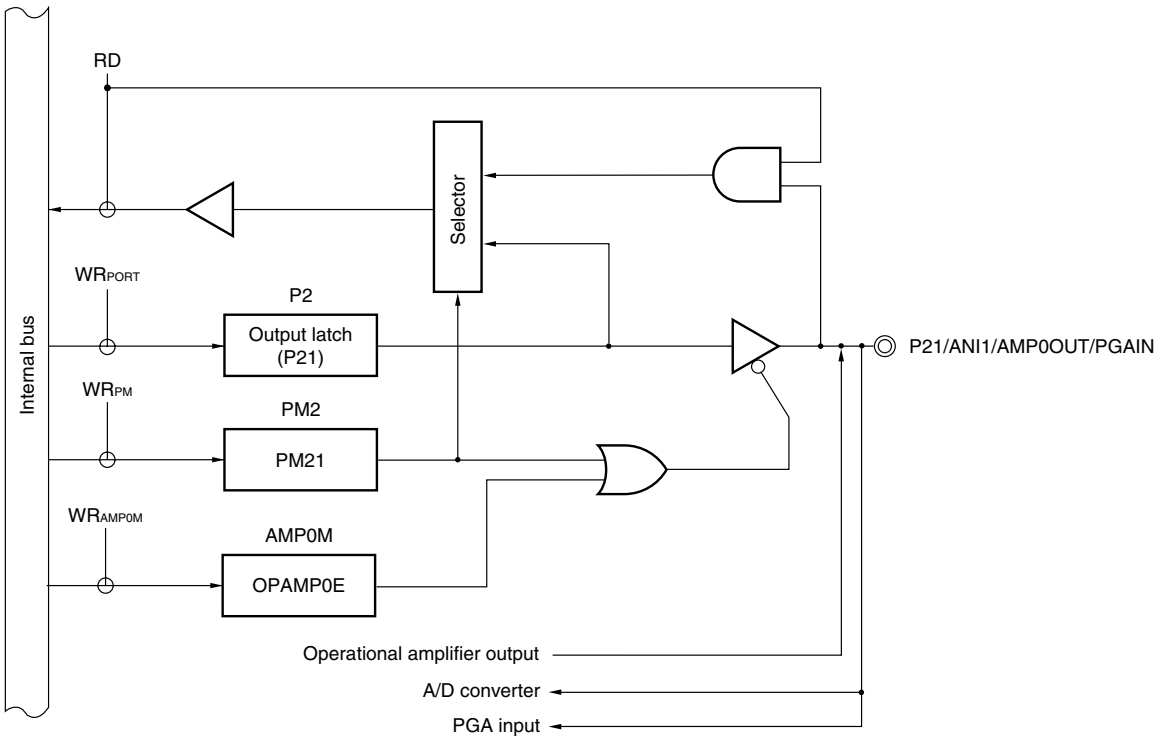


Figure 4-12. Block Diagram of P21

(1) Products without operational amplifier



<R> **(2) Products with operational amplifier**



P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Remark PGA: Programmable Gain Amplifier

Figure 4-36. Format of Port Register (78K0/KA2-L (20-pin products))

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	0	0	0	0	0	P01	P00	FF00H	00H (output latch)	R/W
P2	0	0	P25Note 1	P24Note 1	P23Note 1	P22Note 1	P21Note 1	P20Note 1	FF02H	00H (output latch)	R/W
P3	0	0	0	0	0	P32	P31	P30	FF03H	00H (output latch)	R/W
P6	0	0	0	0	0	0	P61	P60	FF06H	00H (output latch)	R/W
P12	0	0	P125	0	0	P122Note 2	P121Note 2	0	FF0CH	00H	R

Pmn	m = 0, 2, 3, 6, 12; n = 0 to 5	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Notes 1. If this pin is set as an analog input and to input mode, do not access the output latch.

2. “0” is always read from the output latch of the pin in the X1 oscillation mode or external clock input mode.

<R>

Figure 4-44. Format of Pull-up Resistor Option Register (78K0/KC2-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	0	0	0	0	PU02 Note 1	PU01	PU00	FF30H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	FF31H	00H	R/W
PU3	0	0	0	0	PU33	PU32	PU31	PU30	FF33H	00H	R/W
PU4 Note 2	0	0	0	0	0	PU42 Note 1	PU41 Note 2	PU40 Note 2	FF34H	00H	R/W
PU6	0	0	0	0	PU63 Note 2	PU62	PU61	PU60	FF36H	00H	R/W
PU7	0	0	PU75 Note 1	PU74 Note 1	PU73	PU72	PU71	PU70	FF37H	00H	R/W
PU12	0	0	PU125	0	0	0	0	PU120	FF3CH	20H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3, 4, 6, 7, 12; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Notes 1. 48-pin products only

2. 44-pin and 48-pin products only

(4) Port input mode register 6 (PIM6)

This register sets the input buffer of P60 and P61 in 1-bit units.

When using an input compliant with the SMBus specifications in I^2C communication, set PIM60 and PIM61 to 1.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 4-45. Format of Port Input Mode Register 6 (PIM6)

Address: FF3EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM6	0	0	0	0	0	0	PIM61	PIM60

PIM6n	P6n pin input buffer selection (n = 0, 1)
0	Normal input (Schmitt) buffer
1	SMBus input buffer

<R> **Table 4-18. Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KC2-L) (3/3)**

Pin Name	Alternate Function		MUXSEL	PM××	P××
	Function Name	I/O			
P61	SDAA0[Notes 1, 2]	I/O	–	0	1
	SI11	Input	CSISEL = 0	1	×
	INTP10	Input	–	1	×
P62	SO11	Output	CSISEL = 0	0	0
	INTP9	Input	–	1	×
P63[Note 3]	INTP8[Note 3]	Input	–	1	×
P70 to P73, P74[Note 4], P75[Note 4]	KR0 to KR3, KR4[Note 4], KR5[Note 4]	Input	–	1	×
P120	INTP0	Input	–	1	×
	EXLVI	Input	–	1	×
	(SO11)[Note 3]	Output	CSISEL = 1	0	0
P121	X1[Note 5]	–	–	×	×
	TOOLC0	Input	–	×	×
P122	X2[Note 5]	–	–	×	×
	EXCLK[Note 5]	Input	–	×	×
	TOOLD0	I/O	–	×	×
P123	XT1[Note 5]	–	–	×	×
P124	XT2[Note 5]	–	–	×	×
	EXCLKS[Note 5]	Input	–	×	×
P125	$\overline{\text{RESET}}$[Note 6]	Input	–	×	×

Notes 1. During I^2C communication, set SCLA0 and SDAA0 to N-ch open drain output (V_{DD} tolerance) mode by using POM6 register (refer to **4.3 (5) Port output mode register 6 (POM6)**).

2. When using an input compliant with the SMBus specifications in I^2C communication, select the SMBus input buffer by using PIM6 register (refer to **4.3 (4) Port input mode register 6 (PIM6)**).

3. 44-pin and 48-pin products only

4. 48-pin products only

5. When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK) or subsystem clock (EXCLKS), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using OSCCTL register (for details, refer to **5.3 (1) Clock operation mode select register (OSCCTL)** and **(3) Setting of operation mode for subsystem clock pin**). The reset value of OSCCTL is 00H (all of the P121 to P124 pins are Input port pins).

6. Clear RSTM bit (bit 5 of RSTMASK register) to 0 when using P125 as an external reset input ($\overline{\text{RESET}}$).

Remarks 1. ×: Don't care
PM××: Port mode register
P××: Port output latch

2. Functions in parentheses ( ) can be assigned by setting MUXSEL register.

Table 5-6. CPU Clock Transition and SFR Register Setting Examples (2/4)

(4) CPU clock changing from internal high-speed oscillation clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL[Note]	MCM0
(B) → (C) (X1 clock)	0	1	0	Must be checked	1	1
(B) → (C) (external main system clock)	1	1	0	Must not be checked	1	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Note The value of this flag can be changed only once after a reset release. This setting is not necessary if it has already been set.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (refer to CHAPTER 28 ELECTRICAL SPECIFICATIONS).

(5) CPU clock changing from internal high-speed oscillation clock (B) to subsystem clock (D)[Note]

Note 78K0/KC2-L only

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	XTSTART	EXCLKS	OSCSELS	Waiting for Oscillation Stabilization	CSS
(B) → (D) (XT1 clock)	0	0	1	Necessary	1
	1	×	×		
(B) → (D) (external subsystem clock)	0	1	1	Unnecessary	1

Unnecessary if the CPU is operating with the subsystem clock

Remarks 1. (A) to (I) in Table 5-6 correspond to (A) to (I) in Figures 5-18 and 5-19.

2. EXCLK, OSCSEL, EXCLKS, OSCSELS: Bits 7 to 4 of the clock operation mode select register (OSCCTL)
MSTOP: Bit 7 of the main OSC control register (MOC)
XSEL, MCM0: Bits 2 and 0 of the main clock mode register (MCM)
XTSTART, CSS: Bits 6 and 4 of the processor clock control register (PCC)
×: Don't care

Table 5-6. CPU Clock Transition and SFR Register Setting Examples (3/4)

(6) CPU clock changing from high-speed system clock (C) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	RSTOP	RSTS	MCM0
(C) → (B)	0	Confirm this flag is 1.	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

(7) CPU clock changing from high-speed system clock (C) to subsystem clock (D)[Note]

Note 78K0/KC2-L only

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	XTSTART	EXCLKS	OSCSELS	Waiting for Oscillation Stabilization	CSS
(C) → (D) (XT1 clock)	0	0	1	Necessary	1
	1	×	×		
(C) → (D) (external subsystem clock)	0	1	1	Unnecessary	1

Unnecessary if the CPU is operating with the subsystem clock

(8) CPU clock changing from subsystem clock (D) to internal high-speed oscillation clock (B)[Note]

Note 78K0/KC2-L only

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	RSTOP	RSTS	MCM0	CSS
(D) → (B)	0	Confirm this flag is 1.	0	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

↑

Unnecessary if XSEL is 0

Remarks 1. (A) to (I) in Table 5-6 correspond to (A) to (I) in Figure 5-18 and 5-19.

2. MCM0: Bit 0 of the main clock mode register (MCM)
EXCLKS, OSCSELS: Bits 5 and 4 of the clock operation mode select register (OSCCTL)
RSTS, RSTOP: Bits 7 and 0 of the internal oscillation mode register (RCM)
XTSTART, CSS: Bits 6 and 4 of the processor clock control register (PCC)
×: Don't care

5.6.8 Time required for switchover of CPU clock and main system clock

By setting bits 0 to 2 (PCC0 to PCC2) and bit 4 (CSS) of the processor clock control register (PCC), the CPU clock can be switched (between the main system clock and the subsystem clock) and the division ratio of the main system clock can be changed.

The actual switchover operation is not performed immediately after rewriting to PCC; operation continues on the pre-switchover clock for several clocks (refer to **Tables 5-8** and **5-9**).

Whether the CPU is operating on the main system clock or the subsystem clock[Note] can be ascertained using bit 5 (CLS) of the PCC register.

Note 78K0/KC2-L only

Table 5-8. Time Required for Switchover of CPU Clock and Main System Clock Cycle Division Factor (78K0/KY2-L, 78K0/KA2-L, and 78K0/KB2-L)

Set Value Before Switchover			Set Value After Switchover														
PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0
			0	0	0	0	0	1	0	1	0	0	1	1	1	0	0
0	0	0				16 clocks			16 clocks			16 clocks			16 clocks		
0	0	1	8 clocks						8 clocks			8 clocks			8 clocks		
0	1	0	4 clocks			4 clocks						4 clocks			4 clocks		
0	1	1	2 clocks			2 clocks			2 clocks						2 clocks		
1	0	0	1 clock			1 clock			1 clock			1 clock					

Remark The number of clocks listed in Table 5-8 is the number of CPU clocks before switchover.

Table 5-9. Time Required for Switchover of CPU Clock and Main System Clock Cycle Division Factor (78K0/KC2-L)

Set Value Before Switchover				Set Value After Switchover																							
CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0	CSS	PCC2	PCC1	PCC0
				0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1	×	×	×
0	0	0	0					16 clocks				16 clocks				16 clocks				16 clocks				f_{XP}/f_{SUB} clocks			
	0	0	1	8 clocks								8 clocks				8 clocks				8 clocks				$f_{XP}/2f_{SUB}$ clocks			
	0	1	0	4 clocks				4 clocks								4 clocks				4 clocks				$f_{XP}/4f_{SUB}$ clocks			
	0	1	1	2 clocks				2 clocks				2 clocks								2 clocks				$f_{XP}/8f_{SUB}$ clocks			
	1	0	0	1 clock				1 clock				1 clock				1 clock								$f_{XP}/16f_{SUB}$ clocks			
1	×	×	×	2 clocks				2 clocks				2 clocks				2 clocks				2 clocks							

Caution Selection of the main system clock cycle division factor (PCC0 to PCC2) and switchover from the main system clock to the subsystem clock (changing CSS from 0 to 1) should not be set simultaneously.
Simultaneous setting is possible, however, for selection of the main system clock cycle division factor (PCC0 to PCC2) and switchover from the subsystem clock to the main system clock (changing CSS from 1 to 0).

Remark 1. The number of clocks listed in Table 5-9 is the number of CPU clocks before switchover.

(4) Prescaler mode register 00 (PRM00)

PRM00 is the register that sets the TM00 count clock and TI000 and TI010 pin input valid edges.

Rewriting PRM00 is prohibited during operation (when TMC003 and TMC002 = other than 00).

PRM00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears PRM00 to 00H.

Cautions 1. Do not apply the following setting when setting the PRM001 and PRM000 bits to 11 (to specify the valid edge of the TI000 pin as a count clock).

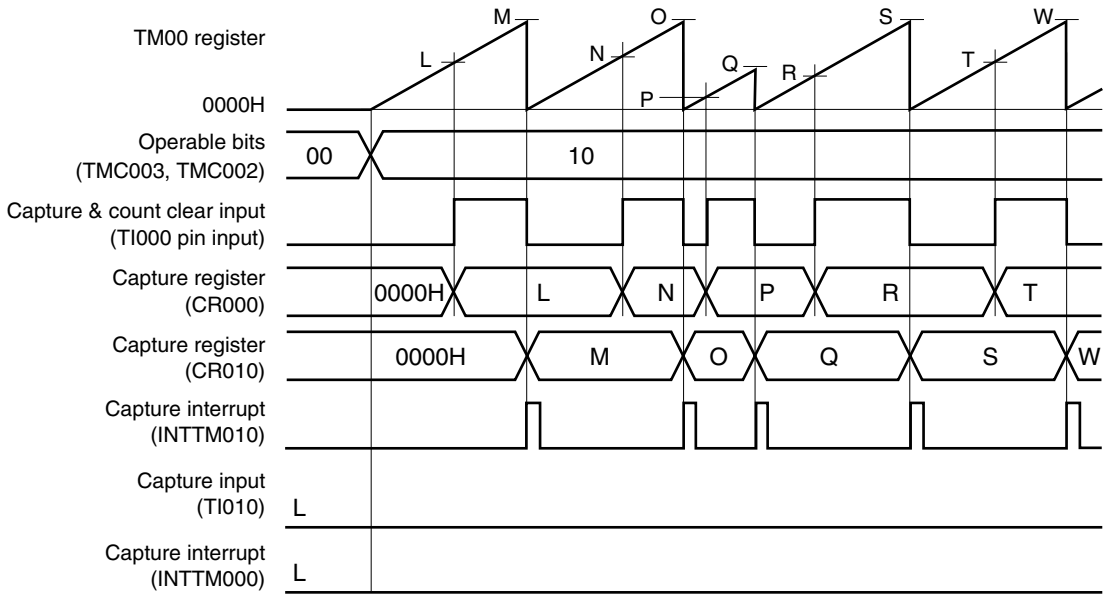
- **Clear & start mode entered by the TI000 pin valid edge**
- **Setting the TI000 pin as a capture trigger**

2. If the operation of the 16-bit timer/event counter 00 is enabled when the TI000 or TI010 pin is at high level and when the valid edge of the TI000 or TI010 pin is specified to be the rising edge or both edges, the high level of the TI000 or TI010 pin is detected as a rising edge. Note this when the TI000 or TI010 pin is pulled up. However, the rising edge is not detected when the timer operation has been once stopped and then is enabled again.

3. The valid edge of TI010 and timer output (TO00) cannot be used for the P01 pin at the same time. Select either of the functions.

Figure 6-30. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Capture Register) (3/3)

(c) TOC00 = 13H, PRM00 = 00H, CRC00 = 07H, TMC00 = 0AH



This is an application example where the pulse width of the signal input to the TI000 pin is measured.
By setting CRC00, the count value can be captured to CR000 in the phase reverse to the falling edge of the TI000 pin (i.e., rising edge) and to CR010 at the falling edge of the TI000 pin.
The high- and low-level widths of the input pulse can be calculated by the following expressions.

- High-level width = [CR010 value] – [CR000 value] × [Count clock cycle]
- Low-level width = [CR000 value] × [Count clock cycle]

If the reverse phase of the TI000 pin is selected as a trigger to capture the count value to CR000, the INTTM000 signal is not generated. Read the values of CR000 and CR010 to measure the pulse width immediately after the INTTM010 signal is generated.
However, if the valid edge specified by bits 6 and 5 (ES110 and ES100) of prescaler mode register 00 (PRM00) is input to the TI010 pin, the count value is not captured but the INTTM000 signal is generated. To measure the pulse width of the TI000 pin, mask the INTTM000 signal when it is not used.

6.4.6 PPG output operation

A square wave having a pulse width set in advance by CR010 is output from the TO00 pin as a PPG (Programmable Pulse Generator) signal during a cycle set by CR000 when bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 11 (clear & start upon a match between TM00 and CR000).

The pulse cycle and duty factor of the pulse generated as the PPG output are as follows.

- Pulse cycle = (Set value of CR000 + 1) × Count clock cycle
- Duty = (Set value of CR010 + 1) / (Set value of CR000 + 1)

Caution To change the duty factor (value of CR010) during operation, refer to 6.5.1 Rewriting CR010 during TM00 operation.

Remarks 1. For the setting of I/O pins, refer to **6.3 (6) Port mode register 0 (PM0)**.

2. For how to enable the INTTM000 signal interrupt, refer to **CHAPTER 17 INTERRUPT FUNCTIONS**.

Figure 6-41. Block Diagram of PPG Output Operation

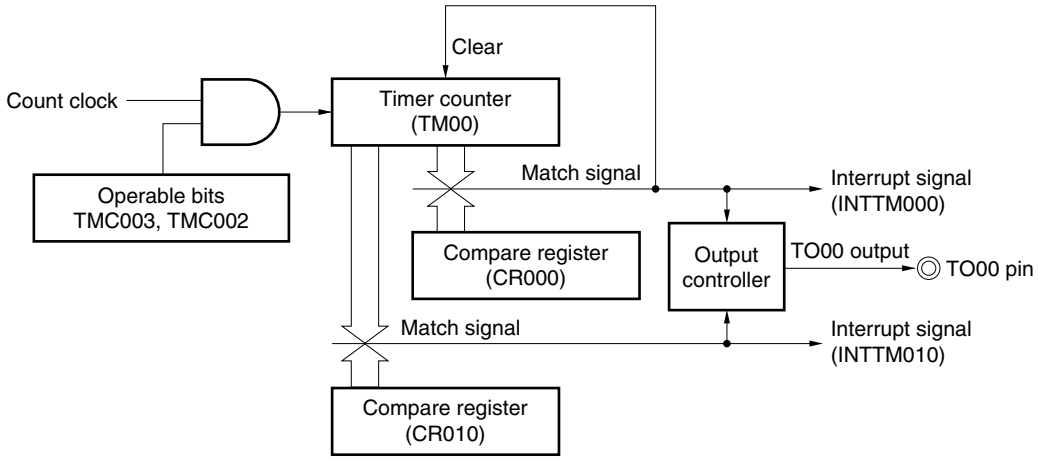
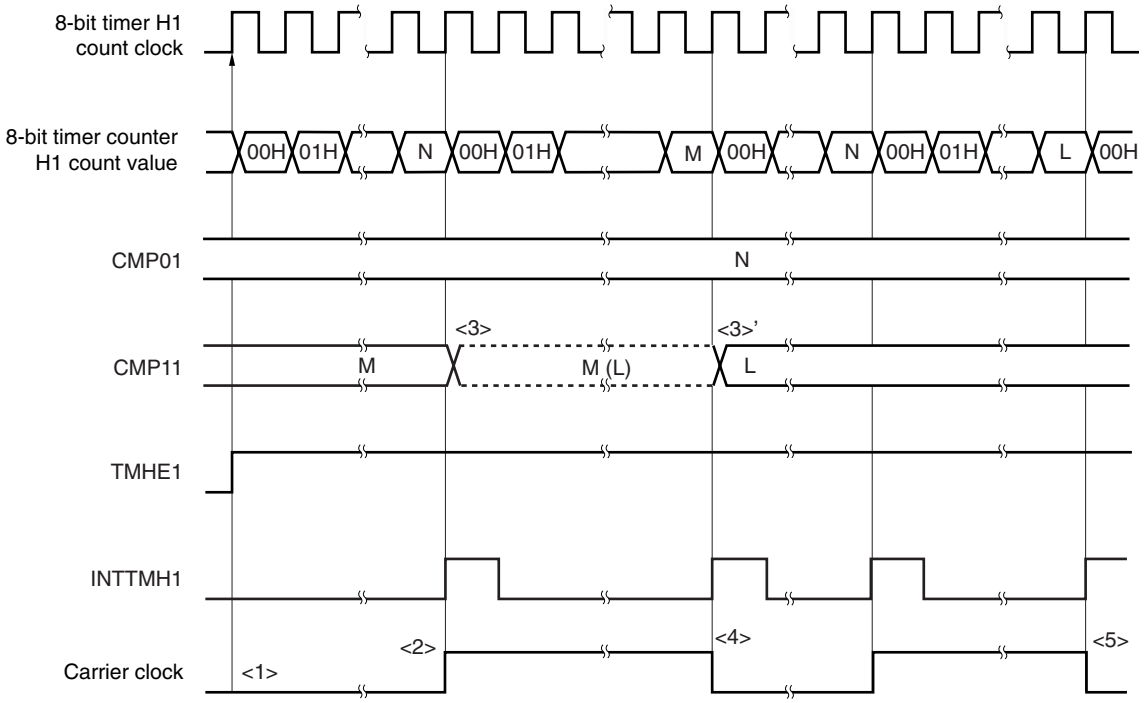


Figure 8-18. Carrier Generator Mode Operation Timing (3/3)

(c) Operation when CMP11 is changed



<1> When TMHE1 = 1 is set, the 8-bit timer H1 starts a count operation. At that time, the carrier clock remains default.

<2> When the count value of the 8-bit timer counter H1 matches the value of the CMP01 register, the INTTMH1 signal is output, the carrier signal is inverted, and the timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter H1 is changed from the CMP01 register to the CMP11 register.

<3> The CMP11 register is asynchronous to the count clock, and its value can be changed while the 8-bit timer H1 is operating. The new value (L) to which the value of the register is to be changed is latched. When the count value of the 8-bit timer counter H1 matches the value (M) of the CMP11 register before the change, the CMP11 register is changed (<3>').

However, it takes three count clocks or more since the value of the CMP11 register has been changed until the value is transferred to the register. Even if a match signal is generated before the duration of three count clocks elapses, the new value is not transferred to the register.

<4> When the count value of 8-bit timer counter H1 matches the value (M) of the CMP11 register before the change, the INTTMH1 signal is output, the carrier signal is inverted, and the timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter H1 is changed from the CMP11 register to the CMP01 register.

<5> The timing at which the count value of the 8-bit timer counter H1 and the CMP11 register value match again is indicated by the value after the change (L).

11.3 Registers Controlling Clock Output Controller

The following two registers are used to control the clock output controller.

- Clock output selection register (CKS)
- Port mode register 4 (PM4)

(1) Clock output selection register (CKS)

This register sets output enable/disable for clock output (PCL) and sets the output clock.

CKS is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CKS to 00H.

Figure 11-2. Format of Clock Output Selection Register (CKS) (48-pin products of 78K0/KC2-L)

Address: FF40H After reset: 00H R/W

Symbol	7	6	5	<4>	3	2	1	0
CKS	0	0	0	CLOE	CCS3	CCS2	CCS1	CCS0

CLOE	PCL output enable/disable specification
0	Clock division circuit operation stopped. PCL fixed to low level.
1	Clock division circuit operation enabled. PCL output enabled.

CCS3	CCS2	CCS1	CCS0	PCL output clock selection[Note 1]			
					f_{SUB} = 32.768 kHz	f_{PRS} = 4 MHz	f_{PRS} = 10 MHz
0	0	0	0	f_{PRS}[Note 2]	–	4 MHz	10 MHz
0	0	0	1	$f_{PRS}/2$		2 MHz	5 MHz
0	0	1	0	$f_{PRS}/2^2$		1 MHz	2.5 MHz
0	0	1	1	$f_{PRS}/2^3$		500 kHz	1.25 MHz
0	1	0	0	$f_{PRS}/2^4$		250 kHz	625 kHz
0	1	0	1	$f_{PRS}/2^5$		125 kHz	312.5 kHz
0	1	1	0	$f_{PRS}/2^6$		62.5 kHz	156.25 kHz
0	1	1	1	$f_{PRS}/2^7$		31.25 kHz	78.125 kHz
1	0	0	0	f_{SUB}	32.768 kHz	–	
Other than above				Setting prohibited			

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If internal high-speed oscillation clock frequency is set to 8 MHz (R4M8MSEL = 0) by option byte and the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{IH}) (XSEL = 0) when 1.8 V $\leq V_{DD} <$ 2.7 V, setting CCS3 = CCS2 = CCS1 = CCS0 = 0 (output clock of PCL: f_{PRS}) is prohibited.

Caution Set CCS3 to CCS0 while the clock output operation is stopped (CLOE = 0).

<R> **Figure 12-12. Format of Port Mode Register 7 (PM7) (78K0/KA2-L (32-pin products))**

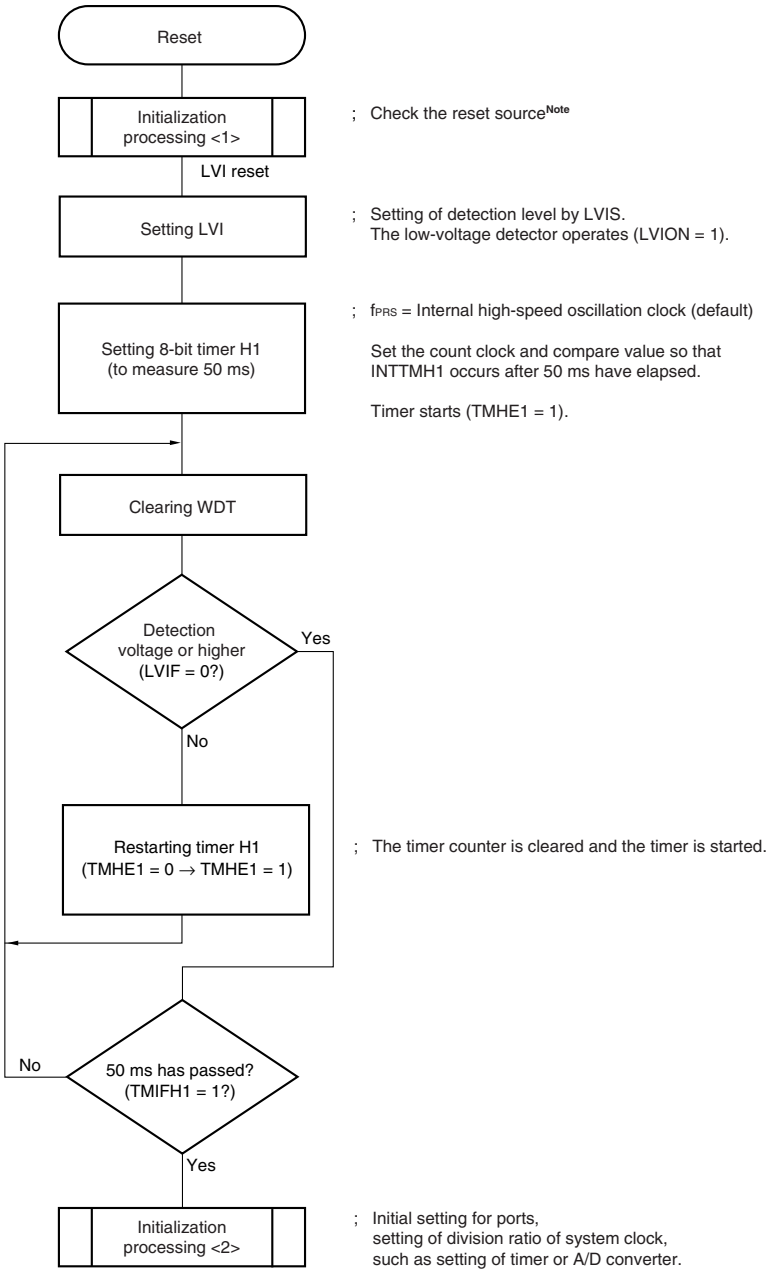
Address: FF27H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM7	1	1	1	1	1	PM72	PM71	PM70

PM7n	P7n pin I/O mode selection (n = 0 to 2)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 22-11. Example of Software Processing After Reset Release (1/2)

• If supply voltage fluctuation is 50 ms or less in vicinity of LVI detection voltage



Note A flowchart is shown on the next page.

25.4 Connection of Pins on Board

To write the flash memory on-board, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be handled as described below.

25.4.1 TOOL pins

The pins used for communication in flash memory programming mode are shown in the table below.

Table 25-3. Pins Used for Communication in Flash Memory Programming Mode

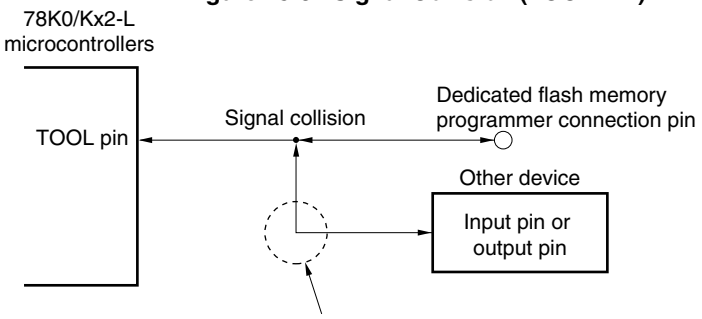
Pin Name	Connection of Pins
TOOLC0, TOOLC1	Connect this pin directly to the dedicated flash memory programmer or pull it down by connecting it to V_{SS} via a resistor (10 kΩ)
TOOLD0, TOOLD1	Connect this pin directly to the dedicated flash memory programmer or pull it up by connecting it to V_{DD} via a resistor (3 k to 10 kΩ)

To connect the dedicated flash memory programmer to the pins of a serial interface that is connected to another device on the board, care must be exercised so that signals do not collide or that the other device does not malfunction.

(1) Signal collision

If the dedicated flash memory programmer is connected to the TOOL pin that is connected to another device, signal collision takes place. To avoid this collision, either isolate the connection with the other device, or make the other device go into a high-impedance state.

Figure 25-3. Signal Collision (TOOL Pin)



In the flash memory programming mode, the signal of the other device collides with the signal of the dedicated flash programmer. Therefore, isolate the signal of the other device.

27.2 Operation List

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	**MOV**	r, #byte	2	4	–	r ← byte	
		saddr, #byte	3	6	7	(saddr) ← byte	
		sfr, #byte	3	–	7	sfr ← byte	
		A, r Note 3	1	2	–	A ← r	
		r, A Note 3	1	2	–	r ← A	
		A, saddr	2	4	5	A ← (saddr)	
		saddr, A	2	4	5	(saddr) ← A	
		A, sfr	2	–	5	A ← sfr	
		sfr, A	2	–	5	sfr ← A	
		A, !addr16	3	8	9	A ← (addr16)	
		!addr16, A	3	8	9	(addr16) ← A	
		PSW, #byte	3	–	7	PSW ← byte	× × ×
		A, PSW	2	–	5	A ← PSW	
		PSW, A	2	–	5	PSW ← A	× × ×
		A, [DE]	1	4	5	A ← (DE)	
		[DE], A	1	4	5	(DE) ← A	
		A, [HL]	1	4	5	A ← (HL)	
		[HL], A	1	4	5	(HL) ← A	
		A, [HL + byte]	2	8	9	A ← (HL + byte)	
		[HL + byte], A	2	8	9	(HL + byte) ← A	
		A, [HL + B]	1	6	7	A ← (HL + B)	
		[HL + B], A	1	6	7	(HL + B) ← A	
		A, [HL + C]	1	6	7	A ← (HL + C)	
		[HL + C], A	1	6	7	(HL + C) ← A	
	XCH	A, r Note 3	1	2	–	A ↔ r	
		A, saddr	2	4	6	A ↔ (saddr)	
		A, sfr	2	–	6	A ↔ (sfr)	
		A, !addr16	3	8	10	A ↔ (addr16)	
		A, [DE]	1	4	6	A ↔ (DE)	
		A, [HL]	1	4	6	A ↔ (HL)	
		A, [HL + byte]	2	8	10	A ↔ (HL + byte)	
		A, [HL + B]	2	8	10	A ↔ (HL + B)	
		A, [HL + C]	2	8	10	A ↔ (HL + C)	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

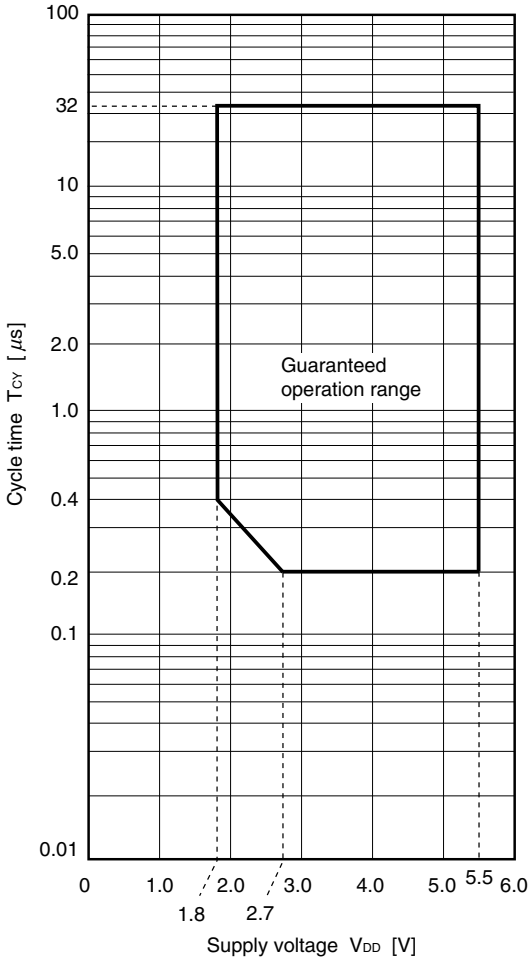
3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

T_{CY} vs. V_{DD} (Main System Clock Operation, RMC = 00H (Normal Power Mode))



(3/8)

Edition	Description	Chapter
2nd Edition	Modification of **Table 12-3 Setting Functions of P10/ANI8/AMP1-, P12/ANI10/AMP1+ Pins**	**CHAPTER 12 A/D CONVERTER**
	Modification of **Table 12-5 Setting Functions of P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins**	
	Deletion of **Caution 2** in **12.4.1 Basic operations of A/D converter**	
	Modification of description of setting methods and deletion of **Caution 2** in **12.4.3 (1) A/D conversion operation**	
	Modification of **Figure 13-1 Block Diagram of Operational Amplifier**	**CHAPTER 13 OPERATIONAL AMPLIFIERS**
	Addition of **Remark** to **Figure 13-2 Format of Operational Amplifier 0 Control Register (AMP0M) (Products with Operational Amplifier Only)**	
	Modification of **Figure 13-4 Format of A/D Port Configuration Register 0 (ADPC0)**	
	Modification of **Figure 13-5 Format of A/D Port Configuration Register 1 (ADPC1) (78K0/KB2-L and 78K0/KC2-L Only)**	
	Modification of **Table 13-2 Setting Functions of P10/ANI8/AMP1-, P12/ANI10/AMP1+ Pins**	
	Modification of **Table 13-4 Setting Functions of P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins**	
	Modification of **Remark** in **Figure 14-4 Block Diagram of Serial Interface UART6**	**CHAPTER 14 SERIAL INTERFACE UART6**
	Addition of **Note 3** to **Figure 14-8 Format of Clock Selection Register 6 (CKSR6)**	
	Modification of description in **14.3 (8) Port mode register 1 (PM1), port mode register 6 (PM6)**	
	Modification of **(1) 78K0/KY2-L and 78K0/KA2-L** in **Table 14-2 Relationship Between Register Settings and Pins**	
	Addition of **15.4.2 Setting transfer clock by using IICWL and IICWH registers**	**CHAPTER 15 SERIAL INTERFACE IICA**
	Modification of the mounted situation in the 78K0/KB2-L and 78K0/KC2-L	**CHAPTER 16 SERIAL INTERFACES CSI10 AND CSI11**
	Modification of description in **16.3 (4) Port mode registers 1, 4, 6, 12 (PM1, PM4, PM6, PM12)**	
	Modification of and addition of **Notes 3** and **4** to **Table 16-3 SO1n Output Status**	
	Modification of maskable interrupts (internal) in the 78K0/KB2-L and 78K0/KC2-L	**CHAPTER 17 INTERRUPT FUNCTIONS**
	Modification of **Table 17-1 Interrupt Source List (1/2)**	
	Modification of **Table 17-2 Flags Corresponding to Interrupt Request Sources (1/2)**	
	Modification of **Caution** in **Figure 17-4 Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (78K0/KB2-L)** to **Figure 17-6 Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (48-pin products of 78K0/KC2-L)**	
	Modification of **Caution** in **Figure 17-9 Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (78K0/KB2-L)** to **Figure 17-11 Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (48-pin products of 78K0/KC2-L)**	

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents