Renesas Electronics America Inc - UPD78F0560MC-CAA-AX Datasheet

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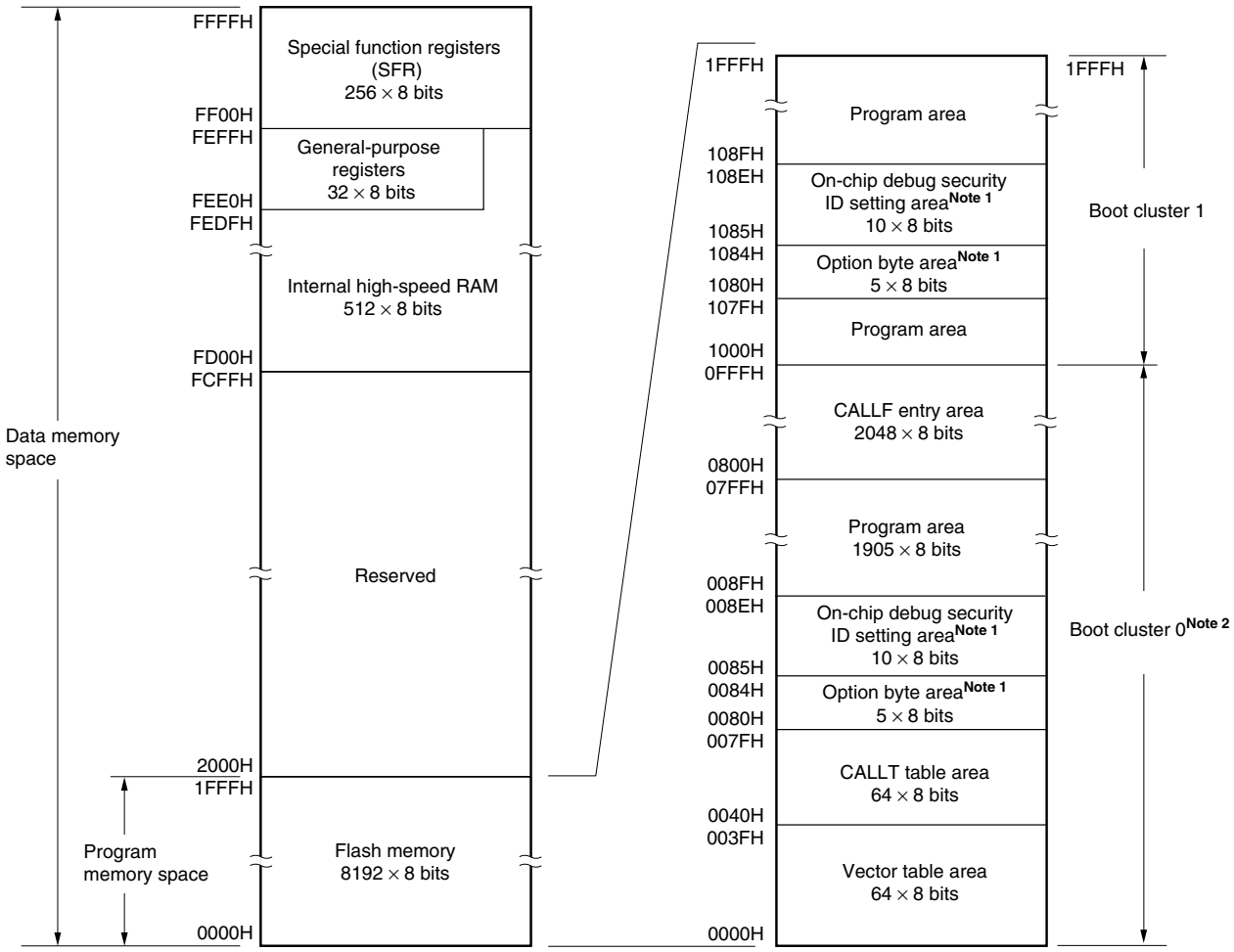
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0560mc-caa-ax

Figure 3-2. Memory Map (μPD78F0551, 78F0556, 78F0561, 78F0566, 78F0571, 78F0576, 78F0581, 78F0586)

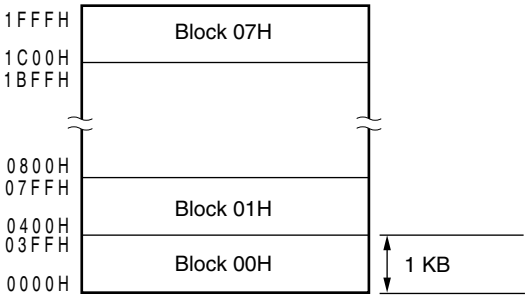


Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (refer to **25.6 Security Settings**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, refer to **Table 3-2 Correspondence Between Address Values and Block Numbers in Flash Memory**.



3.4.8 Based indexed addressing

[Function]

The B or C register contents specified in an instruction word are added to the contents of the base register, that is, the HL register pair in the register bank specified by the register bank select flag (RBS0 and RBS1), and the sum is used to address the memory. Addition is performed by expanding the B or C register contents as a positive number to 16 bits. A carry from the 16th bit is ignored.

This addressing can be carried out for all of the memory spaces.

[Operand format]

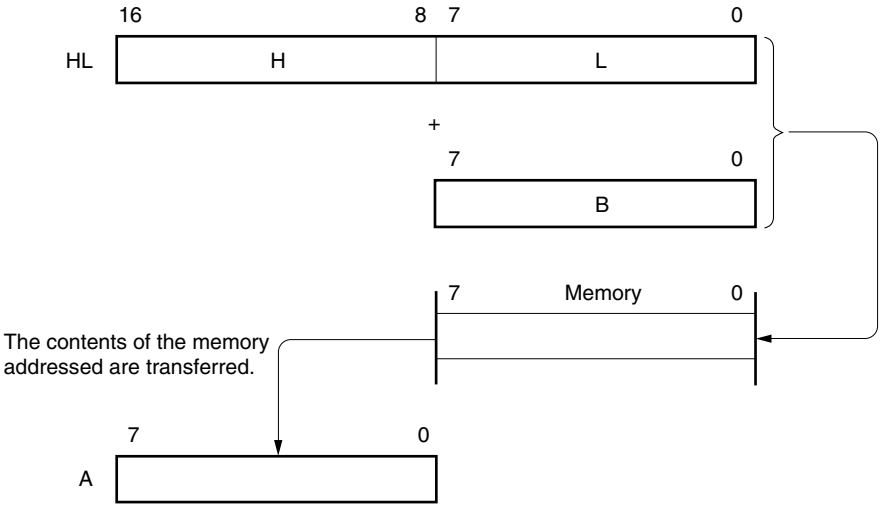
Identifier	Description
–	[HL + B], [HL + C]

[Description example]

MOV A, [HL +B]; when selecting B register

Operation code	1	0	1	0	1	0	1	1

[Illustration]



4.2.7 Port 7

<R>

78K0/KY2-L (μPD78F057x)	78K0/KA2-L (μPD78F056x)		78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)	
16 Pins	20, 25 Pins	32 Pins	30 Pins	40, 44 Pins	48 Pins
–	–	P70/ANI8	–	P70/KR0	P70/KR0
–	–	P71/ANI9	–	P71/KR1	P71/KR1
–	–	P72/ANI10	–	P72/KR2	P72/KR2
–	–	–	–	P73/KR3	P73/KR3
–	–	–	–	–	P74/KR4
–	–	–	–	–	P75/KR5

Port 7 is an I/O port with an output latch. Port 7 can be set to the input mode or output mode in 1-bit units using port mode register 7 (PM7). When the P70 to P75 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 7 (PU7) in 78K0/KC2-L.

<R> This port can also be used for A/D converter analog input and key interrupt input pins.

When using P70/ANI8 to P72/ANI10, set the registers according to the pin function to be used (refer to **Tables 4-13**).

<R> **Table 4-13. Setting Functions of P70/ANI8 to P72/ANI10 Pins**

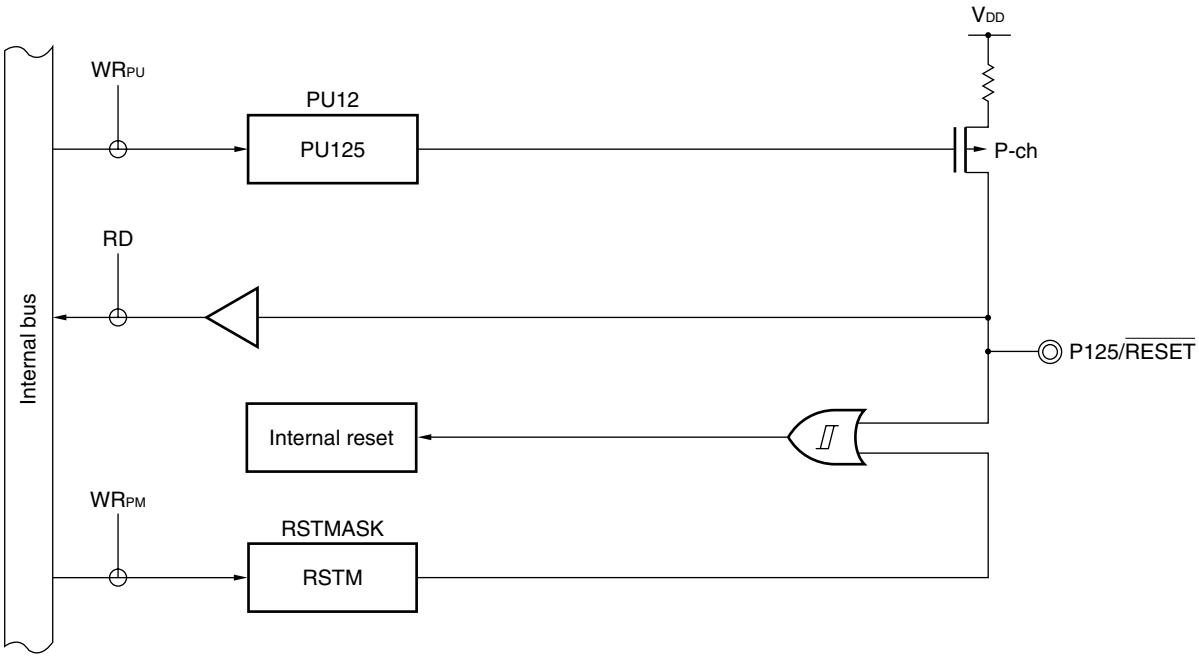
ADPC1 register	PM7 register	ADS register (n = 8 to 10)	P70/ANI8 to P72/ANI10 Pins
Digital I/O selection	Input mode	Selects ANIn.	Setting prohibited
		Does not select ANIn.	Digital input
	Output mode	Selects ANIn.	Setting prohibited
		Does not select ANIn.	Digital output
Analog input selection	Input mode	Selects ANIn.	Analog input (to be converted into digital signals)
		Does not select ANIn.	Analog input (not to be converted into digital signals)
	Output mode	–	Setting prohibited

Remark ADPC1: A/D port configuration register 1
PM7: Port mode register 7
ADS: Analog input channel specification register

Reset signal generation sets port 7 to input mode.

Figure 4-26 shows a block diagram of port 7.

Figure 4-29. Block Diagram of P125



PU12: Pull-up resistor option register 12
RD: Read signal
WR××: Write signal
RSTMASK: Reset pin mode register

<R> **Caution Because $\overline{\text{RESET}}$/P125 is set in the external reset input immediately after release of reset, if a reset signal is generated during low level input, the reset status continues until the input rises to the high level.**

Remark After reset, the external reset function and the pull-up resistor are enabled (RSTM = 0, PU125 = 1). Set RSTM bit to 1 when using as a port function.

(7) Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter. When X1 clock oscillation starts with the internal high-speed oscillation clock or subsystem clock used as the CPU clock, the X1 clock oscillation stabilization time can be checked.

OSTC can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POC, LVI, and WDT), the STOP instruction and MSTOP (bit 7 of MOC register) = 1 clear OSTC to 00H.

Figure 5-10. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFA3H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	0	0	0	MOST11	MOST13	MOST14	MOST15	MOST16

MOST11	MOST13	MOST14	MOST15	MOST16	Oscillation stabilization time status	
						fx = 10 MHz
1	0	0	0	0	2^{11}/fx min.	204.8 μs min.
1	1	0	0	0	2^{13}/fx min.	819.2 μs min.
1	1	1	0	0	2^{14}/fx min.	1.64 ms min.
1	1	1	1	0	2^{15}/fx min.	3.27 ms min.
1	1	1	1	1	2^{16}/fx min.	6.55 ms min.

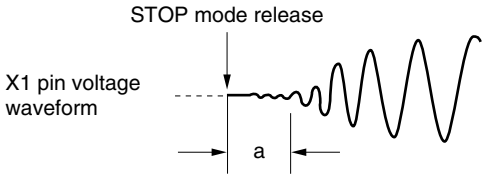
Cautions 1. After the above time has elapsed, the bits are set to 1 in order from MOST11 and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

Remark 2. When switching the CPU clock from the main system clock to the subsystem clock, calculate the number of clocks by rounding up to the next clock and discarding the decimal portion, as shown below.

Example When switching CPU clock from f_{XP} to f_{SUB} (@ oscillation with f_{XP} = 10 MHz, f_{SUB} = 32.768 kHz)

f_{XP}/f_{SUB} = 10000/32.768 ≅ 305.1 → 306 clocks

By setting bit 0 (MCM0) of the main clock mode register (MCM), the main system clock can be switched (between the internal high-speed oscillation clock and the high-speed system clock).

The actual switchover operation is not performed immediately after rewriting to MCM0; operation continues on the pre-switchover clock for several clocks (refer to **Table 5-10**).

Whether the CPU is operating on the internal high-speed oscillation clock or the high-speed system clock can be ascertained using bit 1 (MCS) of MCM.

Table 5-10. Maximum Time Required for Main System Clock Switchover

Set Value Before Switchover	Set Value After Switchover	
MCM0	MCM0	
	0	1
0		1 + $2f_{IH}/f_{XH}$ clock
1	1 + $2f_{XH}/f_{IH}$ clock	

Cautions 1. When switching the internal high-speed oscillation clock to the high-speed system clock, bit 2 (XSEL) of MCM must be set to 1 in advance. The value of XSEL can be changed only once after a reset release.

2. Do not rewrite MCM0 when the CPU clock operates with the subsystem clock.

Remarks 1. The number of clocks listed in Table 5-10 is the number of main system clocks before switchover.

2. Calculate the number of clocks in Table 5-10 by removing the decimal portion.

Example When switching the main system clock from the internal high-speed oscillation clock to the high-speed system clock (@ oscillation with f_{IH} = 8 MHz, f_{XH} = 10 MHz)

1 + $2f_{IH}/f_{XH}$ = 1 + 2 × 8/10 = 1 + 2 × 0.8 = 1 + 1.6 = 2.6 → 2 clocks

5.6.10 Peripheral hardware and source clocks

The following lists peripheral hardware and source clocks incorporated in the 78K0/Kx2-L microcontrollers.

Remark The peripheral hardware depends on the product. Refer to **1.4 Block Diagram** and **1.5 Outline of Functions**.

Table 5-13. Peripheral Hardware and Source Clocks

Peripheral Hardware \ Source Clock		Peripheral Hardware Clock (f_{PRS})	Subsystem Clock (f_{SUB})[Note 1]	Internal Low-Speed Oscillation Clock (f_{IL})	TM50 Output	External Clock from Peripheral Hardware Pins
16-bit timer/event counter 00		Y	N	N	N	Y (TI000 pin)[Note 2]
8-bit timer/ event counter	50	Y	N	N	N	Y (TI50 pin)[Note 2]
	51	Y	N	N	N	Y (TI51 pin)[Note 2]
8-bit timer	H0	Y	N	N	Y	N
	H1	Y	N	Y	N	N
Real-time counter		N	Y	N	N	N
Watchdog timer		N	N	Y	N	N
Clock output		Y	Y	N	N	N
A/D converter		Y	N	N	N	N
Serial interface	UART6	Y	N	N	Y	N
	CSI10	Y	N	N	N	Y ($\overline{SCK10}$ pin)[Note 2]
	CSI11	Y	N	N	N	Y ($\overline{SCK11}$ pin)[Note 2]
	IICA	Y	N	N	N	Y (SCLA0 pin)[Note 2]

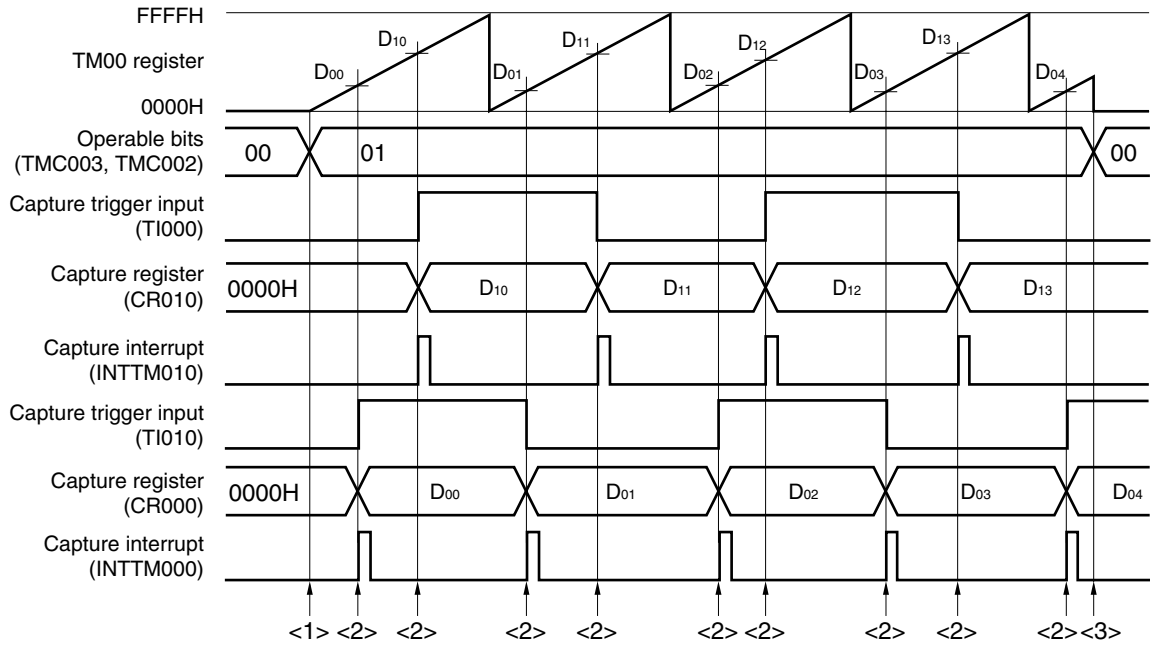
Notes 1. 78K0/KC2-L only

2. Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

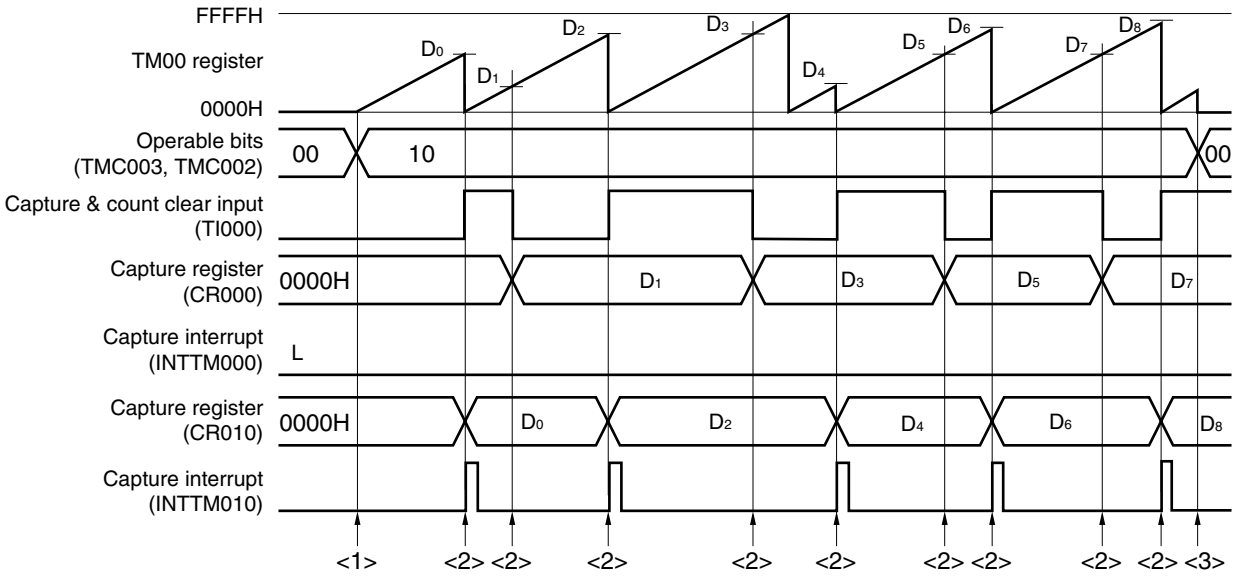
Remark Y: Can be selected, N: Cannot be selected

Figure 6-53. Example of Software Processing for Pulse Width Measurement (1/2)

(a) Example of free-running timer mode



(b) Example of clear & start mode entered by TI000 pin valid edge



(9) Capture operation

(a) When valid edge of TI000 is specified as count clock

When the valid edge of TI000 is specified as the count clock, the capture register for which TI000 is specified as a trigger does not operate correctly.

(b) Pulse width to accurately capture value by signals input to TI010 and TI000 pins

To accurately capture the count value, the pulse input to the TI000 and TI010 pins as a capture trigger must be wider than two count clocks selected by PRM00 (refer to **Figure 6-7**).

(c) Generation of interrupt signal

The capture operation is performed at the falling edge of the count clock but the interrupt signals (INTTM000 and INTTM010) are generated at the rising edge of the next count clock (refer to **Figure 6-7**).

(d) Note when CRC001 (bit 1 of capture/compare control register 00 (CRC00)) is set to 1

When the count value of the TM00 register is captured to the CR000 register in the phase reverse to the signal input to the TI000 pin, the interrupt signal (INTTM000) is not generated after the count value is captured. If the valid edge is detected on the TI010 pin during this operation, the capture operation is not performed but the INTTM000 signal is generated as an external interrupt signal. Mask the INTTM000 signal when the external interrupt is not used.

(10) Edge detection

(a) Specifying valid edge after reset

If the operation of the 16-bit timer/event counter 00 is enabled after reset and while the TI000 or TI010 pin is at high level and when the rising edge or both the edges are specified as the valid edge of the TI000 or TI010 pin, then the high level of the TI000 or TI010 pin is detected as the rising edge. Note this when the TI000 or TI010 pin is pulled up. However, the rising edge is not detected when the operation is once stopped and then enabled again.

(b) Sampling clock for eliminating noise

The sampling clock for eliminating noise differs depending on whether the valid edge of TI000 is used as the count clock or capture trigger. In the former case, the sampling clock is fixed to f_{PRS}. In the latter, the count clock selected by PRM00 is used for sampling.

When the signal input to the TI000 pin is sampled and the valid level is detected two times in a row, the valid edge is detected. Therefore, noise having a short pulse width can be eliminated (refer to **Figure 6-7**).

(11) Timer operation

The signal input to the TI000/TI010 pin is not acknowledged while the timer is stopped, regardless of the operation mode of the CPU.

Remark f_{PRS}: Peripheral hardware clock frequency

10.3 Registers Controlling Real-Time Counter

The real-time counter is controlled by the following 18 registers.

- Peripheral enable register 0 (PER0)
- Real-time counter control register 0 (RTCC0)
- Real-time counter control register 1 (RTCC1)
- Real-time counter control register 2 (RTCC2)
- Sub-count register (RSUBC)
- Second count register (SEC)
- Minute count register (MIN)
- Hour count register (HOUR)
- Day count register (DAY)
- Week count register (WEEK)
- Month count register (MONTH)
- Year count register (YEAR)
- Watch error correction register (SUBCUD)
- Alarm minute register (ALARMWM)
- Alarm hour register (ALARMWH)
- Alarm week register (ALARMWW)
- Port mode register 4 (PM4)
- Port register 4 (P4)

Cautions 1. Be sure to clear bits 4, 5, and 7 to "0".

2. Set a channel to be used for A/D conversion in the input mode by using port mode registers 1, 2, 7 (PM1, PM2, PM7).

3. Set ADS after PGA operation setting when selecting the PGA output signal as analog input. Set ADS after single AMP operation setting when selecting the operational amplifier output signal as analog input (refer to CHAPTER 13 OPERATIONAL AMPLIFIERS).

4. If data is written to ADS, a wait cycle is generated. Do not write data to ADS when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 31 CAUTIONS FOR WAIT.

(6) A/D port configuration registers 0, 1[Note] (ADPC0, ADPC1[Note])

ADPC0 switches the P20/AMP0-/ANI0 to P27/ANI7 pins to digital I/O or analog I/O of port. Each bit of ADPC0 corresponds to a pin of port 2 and can be specified in 1-bit units.

ADPC1 switches the P10/AMP1-/ANI8 to P12/AMP1+/ANI10 or P70/ANI8 to P72/ANI10 pins to digital I/O or analog I/O of port. Each bit of ADPC1 corresponds to a pin of P10 to P12 in port 1 or P70 to P72 in port7 and can be specified in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

<R> Reset signal generation clears ADPC0 to 00H, sets ADPC1 of 78K0/KA2-L (32-pin products) to 00H, and sets ADPC1 of 78K0/KB2-L and 78K0/KC2-L to 07H.

Note 78K0/KA2-L (32-pin products), 78K0/KB2-L, and 78K0/KC2-L only

<R> **Figure 12-9. Format of A/D Port Configuration Registers 0, 1 (ADPC0, ADPC1) (1/3)**

(a) 78K0/KY2-L

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	ADPCS3	ADPCS2	ADPCS1	ADPCS0

(b) 78K0/KA2-L (20-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

(c) 78K0/KA2-L (25-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	ADPCS6	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

Figure 15-6. Format of IICA Status Register 0 (IICAS0) (3/3)

ACKD0	Detection of acknowledge ($\overline{ACK}$)
0	Acknowledge was not detected.
1	Acknowledge was detected.

Condition for clearing (ACKD0 = 0)	Condition for setting (ACKD0 = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by LREL0 = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• After the SDAA0 line is set to low level at the rising edge of SCLA0's ninth clock

STD0	Detection of start condition
0	Start condition was not detected.
1	Start condition was detected. This indicates that the address transfer period is in effect.

Condition for clearing (STD0 = 0)	Condition for setting (STD0 = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by LREL0 = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is detected

SPD0	Detection of stop condition
0	Stop condition was not detected.
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

Condition for clearing (SPD0 = 0)	Condition for setting (SPD0 = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a stop condition is detected

Remark LREL0: Bit 6 of IICA control register 0 (IICACTL0)
IICE0: Bit 7 of IICA control register 0 (IICACTL0)

(3) IICA flag register 0 (IICAF0)

This register sets the operation mode of I^2C and indicates the status of the I^2C bus.

This register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the STT0 clear flag (STCF) and I^2C bus status flag (IICBSY) are read-only.

The IICRSV bit can be used to enable/disable the communication reservation function.

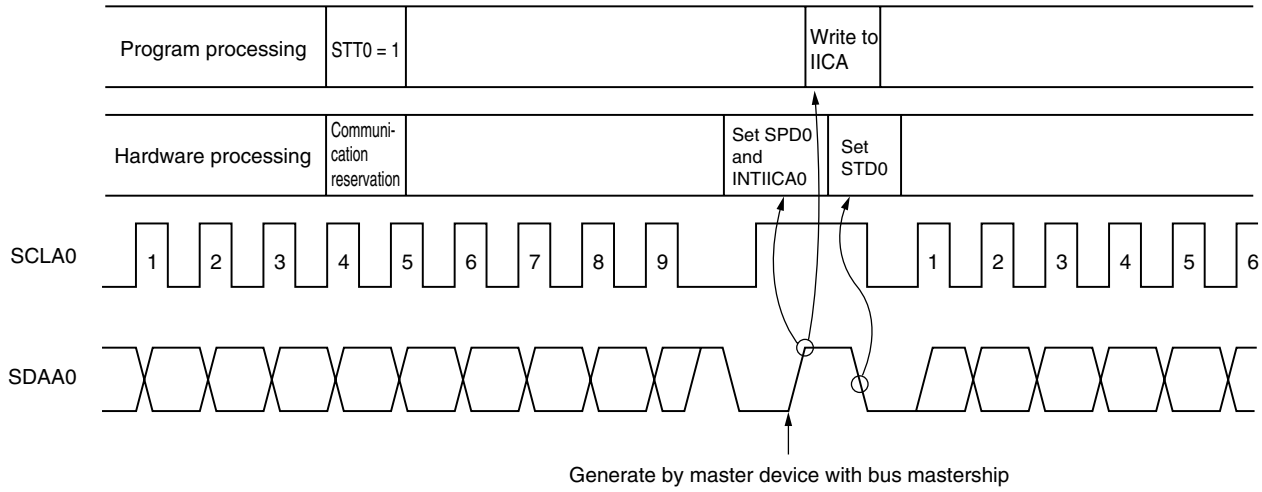
The STCEN bit can be used to set the initial value of the IICBSY bit.

The IICRSV and STCEN bits can be written only when the operation of I^2C is disabled (bit 7 (IICE0) of the IICA control register 0 (IICACTL0) = 0). When operation is enabled, the IICAF0 register can be read.

Reset signal generation clears this register to 00H.

Figure 15-26 shows the communication reservation timing.

Figure 15-26. Communication Reservation Timing



Remark IICA: IICA shift register
STT0: Bit 1 of IICA control register 0 (IICACTL0)
STD0: Bit 1 of IICA status register 0 (IICAS0)
SPD0: Bit 0 of IICA status register 0 (IICAS0)

Communication reservations are accepted via the timing shown in Figure 15-27. After bit 1 (STD0) of the IICA status register 0 (IICAS0) is set to 1, a communication reservation can be made by setting bit 1 (STT0) of the IICA control register 0 (IICACTL0) to 1 before a stop condition is detected.

Figure 15-27. Timing for Accepting Communication Reservations

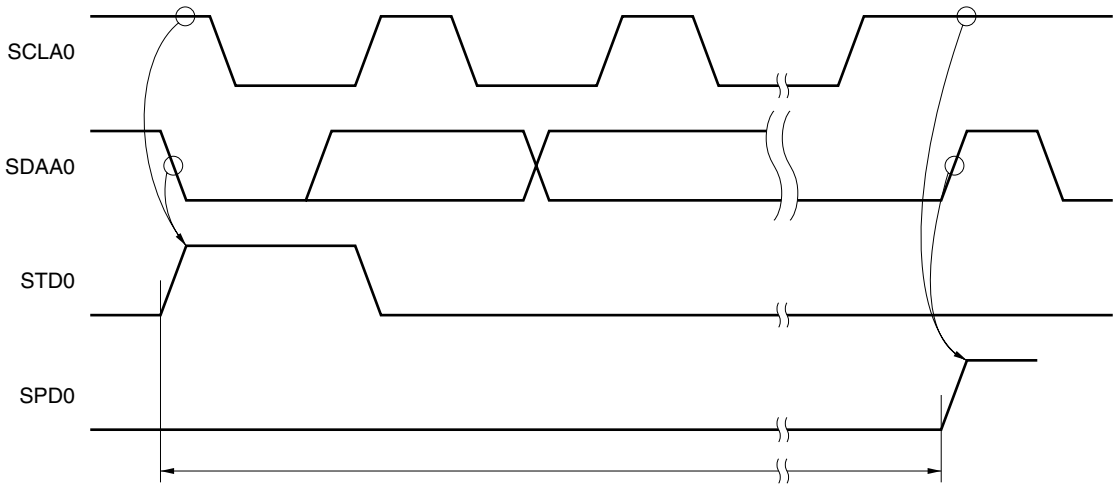
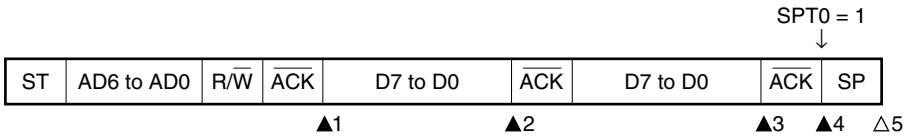


Figure 15-28 shows the communication reservation protocol.

(1) Master device operation

(a) Start ~ Address ~ Data ~ Data ~ Stop (transmission/reception)

(i) When WTIM0 = 0

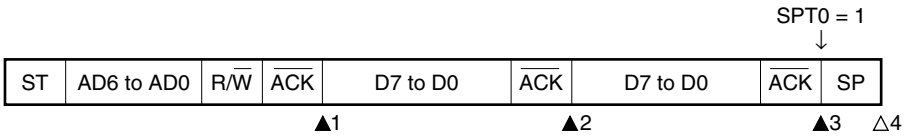


▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 1000×000B
▲3: IICAS0 = 1000×000B (Sets WTIM0 to 1)[Note]
▲4: IICAS0 = 1000××00B (Sets SPT0 to 1)[Note]
△5: IICAS0 = 00000001B

Note To generate a stop condition, set WTIM0 to 1 and change the timing for generating the INTIICA0 interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1

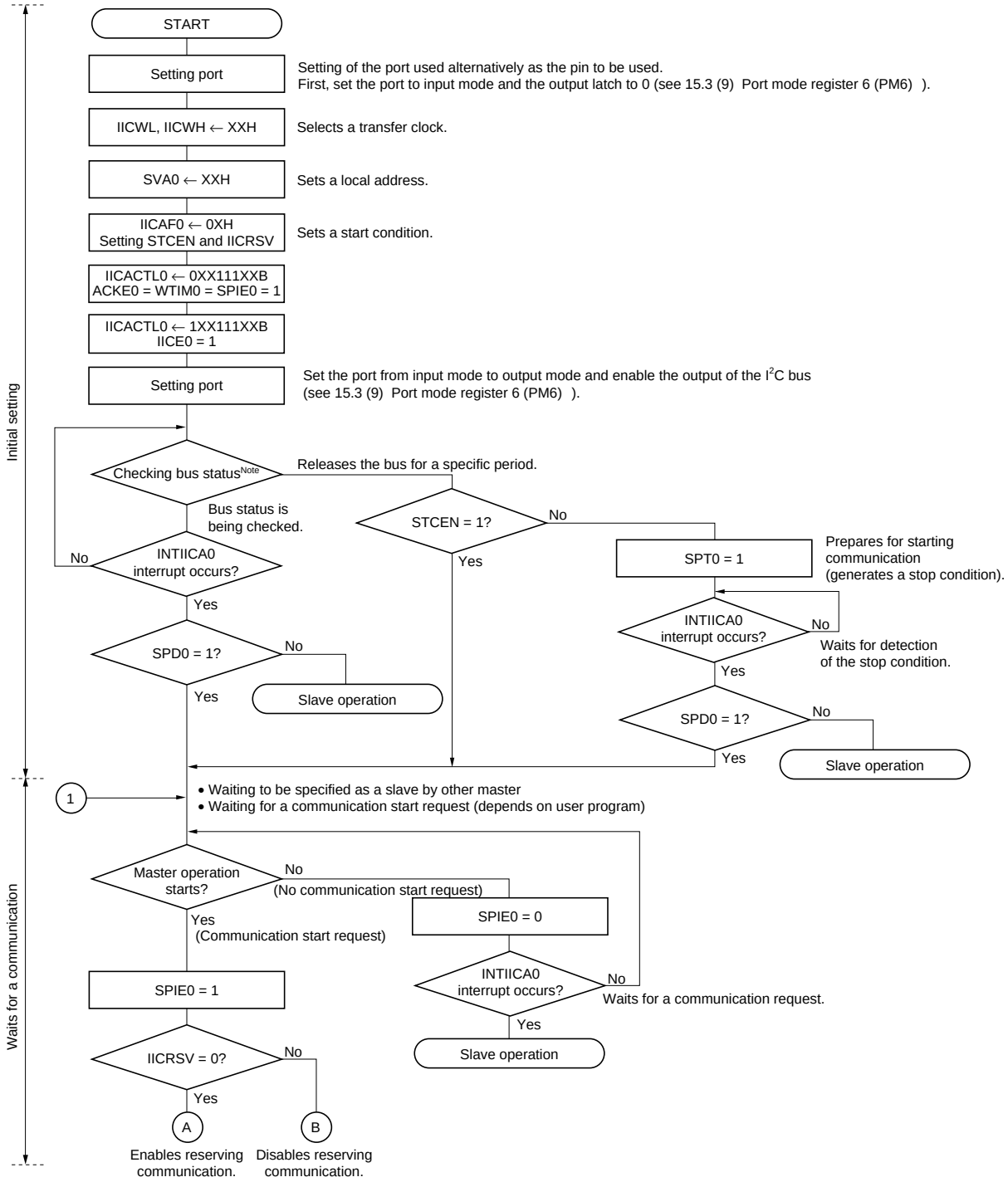


▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 1000×100B
▲3: IICAS0 = 1000××00B (Sets SPT0 to 1)
△4: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(2) Master operation in multi-master system

Figure 15-30. Master Operation in Multi-Master System (1/3)



Note Confirm that the bus is released (CLD0 bit = 1, DAD0 bit = 1) for a specific period (for example, for a period of one frame). If the SDAA0 pin is constantly at low level, decide whether to release the I^2C bus (SCLA0 and SDAA0 pins = high level) in conformance with the specifications of the product that is communicating.