# Renesas Electronics America Inc - UPD78F0561MC-CAA-AX Datasheet

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## What is "Embedded - Microcontrollers"?

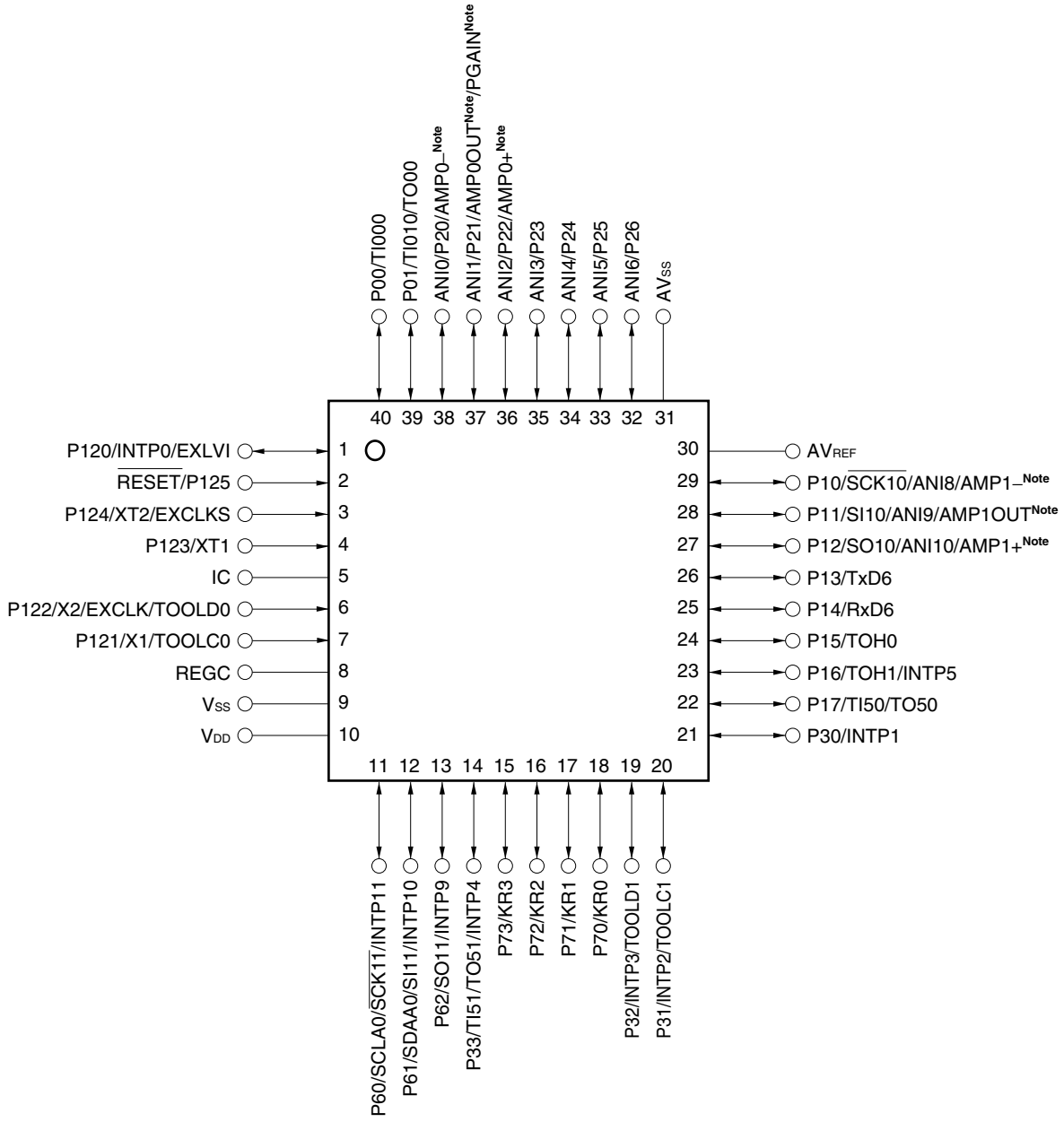
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 78K/0 |
| Core Size | 8-Bit |
| Speed | 10MHz |
| Connectivity | I²C, LINbus, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 13 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 6x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-LSSOP (0.240", 6.10mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0561mc-caa-ax |

### 1.3.4 78K0/KC2-L

<R> **(1) 40-pin plastic WQFN (6x6) (1/2)**




**Note** μPD78F0586, 78F0587, 78F0588 (products with operational amplifier) only

**Cautions 1. Leave the IC (Internally Connected) pin open.**

**2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).**

**3. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, and ANI3/P23 to ANI6/P26 are set in the analog input mode, P10/ANI8/AMP1-/SCK10, P11/ANI9/AMP1OUT/SI10, and P12/ANI10/AMP1+/SO10 are set in the digital input mode after release of reset.**

**4. RESET/P125 immediately after release of reset is set in the external reset input.**

**5. Set P40, P41, and P63 to output mode (PM40 = PM41 = PM63 = 0) by using software after release of reset.**

### (3) 48-pin plastic LQFP (fine pitch) (7x7) (2/2)

| | | | |
|---|---|---|---|
| AMP0-[Note], AMP0+[Note], AMP1-[Note], AMP1+[Note] : | Amplifier Input | REGC : | Regulator Capacitance |
| AMP0OUT[Note], AMP1OUT[Note] : | Amplifier Output | $\overline{\text{RESET}}$ : | Reset |
| PGAIN[Note] : | Programmable Gain Amplifier Input | RTC1HZ : | Real-time Counter Correction Clock (1 Hz) Output |
| ANI0-ANI10 : | Analog Input | RTCCL : | Real-time Counter Clock (32 kHz Original Oscillation) Output |
| $AV_{REF}$ : | Analog Reference Voltage | RTCDIV : | Real-time Counter Clock (32 kHz Divided Frequency) Output |
| $AV_{SS}$ : | Analog Ground | | |
| EXCLK : | External Clock Input (Main System Clock) | RxD6 : | Receive Data |
| EXCLKS : | External Clock Input (Subsystem Clock) | SCLA0, $\overline{\text{SCK10}}$, $\overline{\text{SCK11}}$ : | Serial Clock Input/Output |
| | | SDAA0 : | Serial Data Input/Output |
| EXLVI : | External potential Input for Low-voltage detector | SI10, SI11 : | Serial Data Input |
| | | SO10, SO11 : | Serial Data Output |
| IC : | Internally Connected | $\overline{\text{SSI11}}$ : | Serial Interface Chip Select Input |
| INTP0 to INTP11 : | External Interrupt Input | TI000, TI010, TI50, TI51 : | Timer Input |
| KR0 to KR5 : | Key Return | TO00, TO50, TO51, TOH0, TOH1 : | Timer Output |
| P00 to P02 : | Port 0 | TOOLC0, TOOLC1 : | Clock Input for Tool |
| P10 to P17 : | Port 1 | TOOLD0, TOOLD1 : | Data Input/Output for Tool |
| P20 to P27 : | Port 2 | TxD6 : | Transmit Data |
| P30 to P33 : | Port 3 | $V_{DD}$ : | Power Supply |
| P40 to P42 : | Port 4 | $V_{SS}$ : | Ground |
| P60 to P63 : | Port 6 | X1, X2 : | Crystal Oscillator (Main System Clock) |
| P70 to P75 : | Port 7 | | |
| P120 to P125 : | Port 12 | XT1, XT2 : | Crystal Oscillator (Subsystem Clock) |
| PCL : | Programmble Clock Output | | |

**Note** $\mu$PD78F0586, 78F0587, 78F0588 (products with operational amplifier) only

### 2.2.8 P120 to P125 (port 12)

P120 functions as an I/O port. P121 to P125 function as an Input port. These pins also function as pins for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, external clock input for main system clock, external clock input for subsystem clock, external reset input, and clock input and data I/O for flash memory programmer/on-chip debugger.

Set bit 5 (RSTM) of the reset pin mode register (RSTMASK) to 1 when using P125/$\overline{\text{RESET}}$ as an input port, and clear RSTM to 0 when using P125/$\overline{\text{RESET}}$ as an external reset input.

<R> Furthermore, the timer input and external interrupt request input can be assigned to P121 of the 78K0/KA2-L (25-pin products) and P121 and P125 of the 78K0/KA2-L (32-pin products) by setting the port alternate switch control register (MUXSEL). The data output of the serial interface can be assigned to P120 of the 78K0/KC2-L (44-pin and 48-pin products) by setting the port alternate switch control register (MUXSEL).

<R>

| 78K0/KY2-L (μPD78F055x) | 78K0/KA2-L (μPD78F056x) | | | 78K0/KB2-L (μPD78F057x) | 78K0/KC2-L (μPD78F058x) | |
|---|---|---|---|---|---|---|
| 16 Pins | 20 Pins | 25 Pins | 32 Pins | 30 Pins | 40 Pins | 44, 48 Pins |
| – | – | – | – | P120/EXLVI/ INTP0 | P120/EXLVI/ INTP0 | P120/EXLVI/ INTP0(/SO11) |
| P121/X1/ TOOLC0 | P121/X1/ TOOLC0 | P121/X1/ TOOLC0 (/TI000) (/INTP0) | P121/X1/ TOOLC0 (/TI000) (/INTP0) | P121/X1/ TOOLC0 | P121/X1/ TOOLC0 | P121/X1/ TOOLC0 |
| P122/X2/ EXCLK/ TOOLD0 | P122/X2/ EXCLK/ TOOLD0 | P122/X2/ EXCLK/ TOOLD0 | P122/X2/ EXCLK/ TOOLD0 | P122/X2/ EXCLK/ TOOLD0 | P122/X2/ EXCLK/ TOOLD0 | P122/X2/ EXCLK/ TOOLD0 |
| – | – | – | – | – | P123/XT1 | P123/XT1 |
| – | – | – | – | – | P124/XT2/ EXCLKS | P124/XT2/ EXCLKS |
| P125/$\overline{\text{RESET}}$ | P125/$\overline{\text{RESET}}$ | P125/$\overline{\text{RESET}}$ | P125/$\overline{\text{RESET}}$ (/TI000) (/INTP0) | P125/$\overline{\text{RESET}}$ | P125/$\overline{\text{RESET}}$ | P125/$\overline{\text{RESET}}$ |

**Remark** Functions in parentheses ( ) can be assigned by setting the port alternate switch control register (MUXSEL).

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P120 to P125 function as an I/O port. P120 to P125 can be set to input or output port using port mode register 12 (PM12). Only for P120 and P125, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

**(2) Control mode**

P120 to P125 function as pins for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, external clock input for main system clock, external clock input for subsystem clock, external reset input, and clock input and data I/O for flash memory programmer/on-chip debugger.

**Figure 4-48. Format of A/D Port Configuration Register 0, 1 (ADPC0, ADPC1) (2/2)**

**(e) 78K0/KB2-L**

Address: FF2EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC0 | 0 | 0 | 0 | 0 | ADPCS3 | ADPCS2 | ADPCS1 | ADPCS0 |

Address: FF2FH After reset: 07H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC1 | 0 | 0 | 0 | 0 | 0 | ADPCS10 | ADPCS9 | ADPCS8 |

**(f) 78K0/KC2-L (40-pin products)**

Address: FF2EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC0 | 0 | ADPCS6 | ADPCS5 | ADPCS4 | ADPCS3 | ADPCS2 | ADPCS1 | ADPCS0 |

Address: FF2FH After reset: 07H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC1 | 0 | 0 | 0 | 0 | 0 | ADPCS10 | ADPCS9 | ADPCS8 |

**(g) 78K0/KC2-L (44-pin and 48-pin products)**

Address: FF2EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC0 | ADPCS7 | ADPCS6 | ADPCS5 | ADPCS4 | ADPCS3 | ADPCS2 | ADPCS1 | ADPCS0 |

Address: FF2FH After reset: 07H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC1 | 0 | 0 | 0 | 0 | 0 | ADPCS10 | ADPCS9 | ADPCS8 |

| ADPCSn | Digital I/O or analog I/O selection (n = 0 to 10) |
|---|---|
| 0 | Analog I/O |
| 1 | Digital I/O |

**Cautions 1. Set the pin set to analog input to the input mode by using port mode register 1, 2, and 7 (PM1, PM2, and PM7).**

**2. If data is written to ADPC0 and ADPC1, a wait cycle is generated. Do not write data to ADPC0 and ADPC1 when the peripheral hardware clock is stopped. For details, refer to CHAPTER 31 CAUTIONS FOR WAIT.**

**Table 4-15. Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KA2-L (20-pin products)) (2/2)**

| Pin Name | Alternate Function | | PM×× | P×× |
|---|---|---|---|---|
| | Function Name | I/O | | |
| P121 | X1[Note 1] | – | × | × |
| | TOOLC0 | Input | × | × |
| P122 | X2[Note 1] | – | × | × |
| | EXCLK[Note 1] | Input | × | × |
| | TOOLD0 | I/O | × | × |
| P125 | $\overline{\text{RESET}}$[Note 2] | Input | × | × |

**Notes 1.** When using the P121 and P122 pins to connect a resonator for the main system clock (X1, X2) or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode or external clock input mode must be set by using OSCCTL register (for details, refer to **5.3 (1) Clock operation mode select register (OSCCTL)**). The reset value of OSCCTL is 00H (both P121 and P122 are input port pins).

**2.** Clear RSTM bit (bit 5 of RSTMASK register) to 0 when using P125 as an external reset input ($\overline{\text{RESET}}$).

**Remark** ×: Don't care
PM××: Port mode register
P××: Port output latch

<R> **Table 4-16. Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KA2-L (25-pin and 32-pin products)) (2/2)**

| Pin Name | Alternate Function | | MUXSEL | PM×× | P×× |
|---|---|---|---|---|---|
| | Function Name | I/O | | | |
| P60 | SCLA0 Notes 1, 2 | I/O | – | 0 | 1 |
| | TxD6 Note 3 | Output | – | 0 | 1 |
| P61 | SDAA0 Notes 1, 2 | I/O | – | 0 | 1 |
| | RxD6 | Input | – | 1 | × |
| P70 to P72 Note 4 | ANI8 to ANI10 Notes 4, 5 | Input | – | 1 | × |
| P121 | X1 Note 6 | – | – | × | × |
| | TOOLC0 | Input | – | × | × |
| | (TI000) | Input | TM00SEL1 Note 4, TM00SEL0 = 0, 1 | × | × |
| | (INTP0) | Input | INTP0SEL1 Note 4, INTP0SEL0 = 0, 1 | × | × |
| P122 | X2 Note 6 | – | – | × | × |
| | EXCLK Note 6 | Input | – | × | × |
| | TOOLD0 | I/O | – | × | × |
| P125 | $\overline{\text{RESET}}$ Note 7 | Input | – | × | × |
| | (TI000) Note 4 | Input | TM00SEL1, TM00SEL0 = 1, 0 | × | × |
| | (INTP0) Note 4 | Input | INTP0SEL1, INTP0SEL0 = 1, 0 | × | × |

**Notes 1.** During $I^2C$ communication, set SCLA0 and SDAA0 to N-ch open drain output ($V_{DD}$ tolerance) mode by using POM6 register (refer to **4.3 (5) Port output mode register 6 (POM6)**).

**2.** When using an input compliant with the SMBus specifications in $I^2C$ communication, select the SMBus input buffer by using PIM6 register (refer to **4.3 (4) Port input mode register 6 (PIM6)**).

**3.** During UART communication, set TxD6 to normal output (CMOS output) mode by using POM6 register (refer to **4.3 (5) Port output mode register 6 (POM6)**).

**4.** 32-pin products only

**5.** The pin function can be selected by using ADPC1 register, PM7 register, and ADS register. Refer to **Table 4-13** of **4.2.7 Port 7**.

**6.** When using the P121 and P122 pins to connect a resonator for the main system clock (X1, X2) or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode or external clock input mode must be set by using OSCCTL register (for details, refer to **5.3 (1) Clock operation mode select register (OSCCTL)**). The reset value of OSCCTL is 00H (both P121 and P122 are input port pins).

**7.** Clear RSTM bit (bit 5 of RSTMASK register) to 0 when using P125 as an external reset input ($\overline{\text{RESET}}$).

**Remarks 1.** ×: Don't care
PM××: Port mode register
P××: Port output latch

**2.** Functions in parentheses ( ) can be assigned by setting MUXSEL register.

**(2) Measuring the pulse width by using one input signal of the TI000 pin (free-running timer mode)**

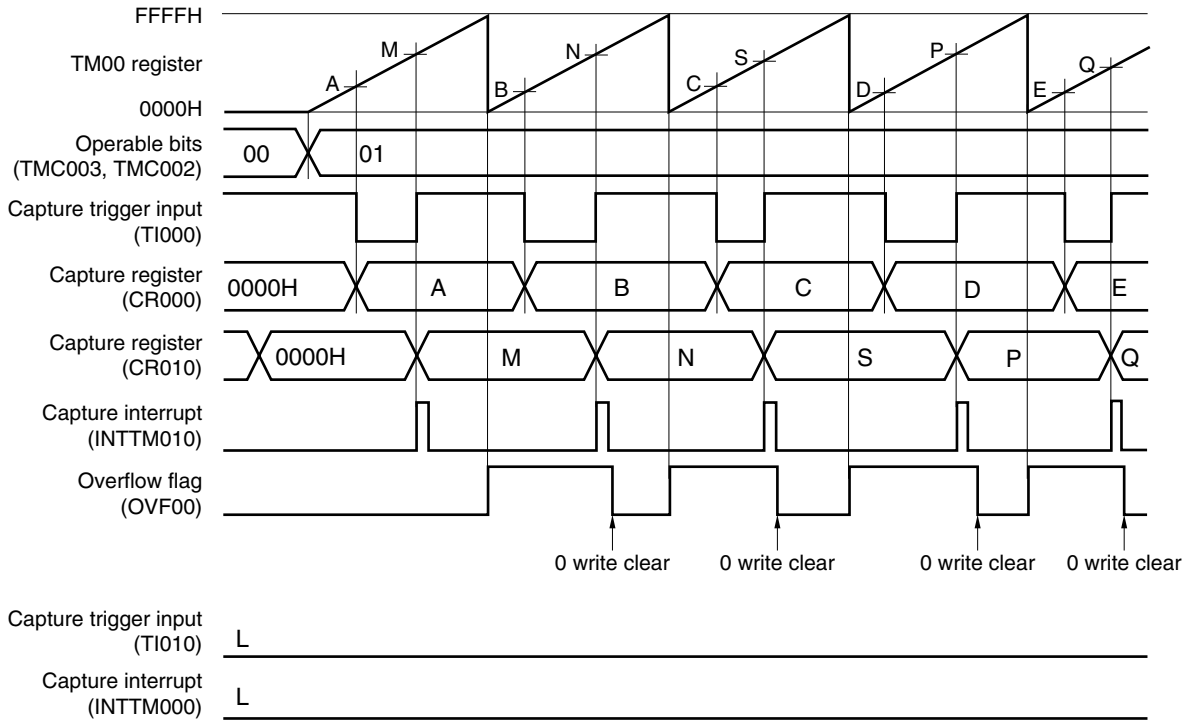
Set the free-running timer mode (TMC003 and TMC002 = 01). The count value of TM00 is captured to CR000 in the phase reverse to the valid edge detected on the TI000 pin. When the valid edge of the TI000 pin is detected, the count value of TM00 is captured to CR010.

By this measurement method, values are stored in separate capture registers when a width from one edge to another is measured. Therefore, the capture values do not have to be saved. By subtracting the value of one capture register from that of another, a high-level width, low-level width, and cycle are calculated.

If an overflow occurs, the value becomes negative if one captured value is simply subtracted from another and, therefore, a borrow occurs (bit 0 (CY) of the program status word (PSW) is set to 1). If this happens, ignore CY and take the calculated value as the pulse width. In addition, clear bit 0 (OVF00) of 16-bit timer mode control register 00 (TMC00) to 0.

**Figure 6-50. Timing Example of Pulse Width Measurement (2)**

**• TMC00 = 04H, PRM00 = 10H, CRC00 = 07H**



### 7.4.3 Square-wave output operation

A square wave with any selected frequency is output at intervals determined by the value preset to 8-bit timer compare register 5n (CR5n).

The TO5n pin output status is inverted at intervals determined by the count value preset to CR5n by setting bit 0 (TOE5n) of 8-bit timer mode control register 5n (TMC5n) to 1. This enables a square wave with any selected frequency to be output (duty = 50%).

**Remark** Square-wave output is operable only in the 78K0/KB2-L and 78K0/KC2-L.

Setting

<1> Set each register.

- Clear the port output latch (P17 or P33)[Note] and port mode register (PM17 or PM33)[Note] to 0.
- TCL5n: Select the count clock.
- CR5n: Compare value
- TMC5n: Stop the count operation, select the mode in which clear & start occurs on a match of TM5n and CR5n.

| LVS5n | LVR5n | Timer Output F/F Status Setting |
|---|---|---|
| 0 | 1 | Timer output F/F clear (0) (default value of TO5n output: low level) |
| 1 | 0 | Timer output F/F set (1) (default value of TO5n output: high level) |

Timer output enabled
(TMC5n = 00001011B or 00000111B)

<2> After TCE5n = 1 is set, the count operation starts.

<3> The timer output F/F is inverted by a match of TM5n and CR5n. After INTTM5n is generated, TM5n is cleared to 00H.

<4> After these settings, the timer output F/F is inverted at the same interval and a square wave is output from TO5n. The frequency is as follows.

- Frequency = 1/2t (N + 1)
  (N: 00H to FFH)

**Note** 8-bit timer/event counter 50: P17, PM17
8-bit timer/event counter 51: P33, PM33

**Caution Do not write other values to CR5n during operation.**

**Remarks 1.** For how to enable the INTTM5n signal interrupt, refer to **CHAPTER 17 INTERRUPT FUNCTIONS**.

**2.** 78K0/KB2-L, 78K0/KC2-L: n = 0, 1

# CHAPTER 11 CLOCK OUTPUT CONTROLLER

| Item | 78K0/KY2-L ($\mu$PD78F055x) | 78K0/KA2-L ($\mu$PD78F056x) | 78K0/KB2-L ($\mu$PD78F057x) | 78K0/KC2-L ($\mu$PD78F058x) | |
|---|---|---|---|---|---|
| | 16 Pins | 20, 25, 32 Pins | 30 Pins | 40, 44 Pins | 48 Pins |
| Clock output controller | – | | | | √ |

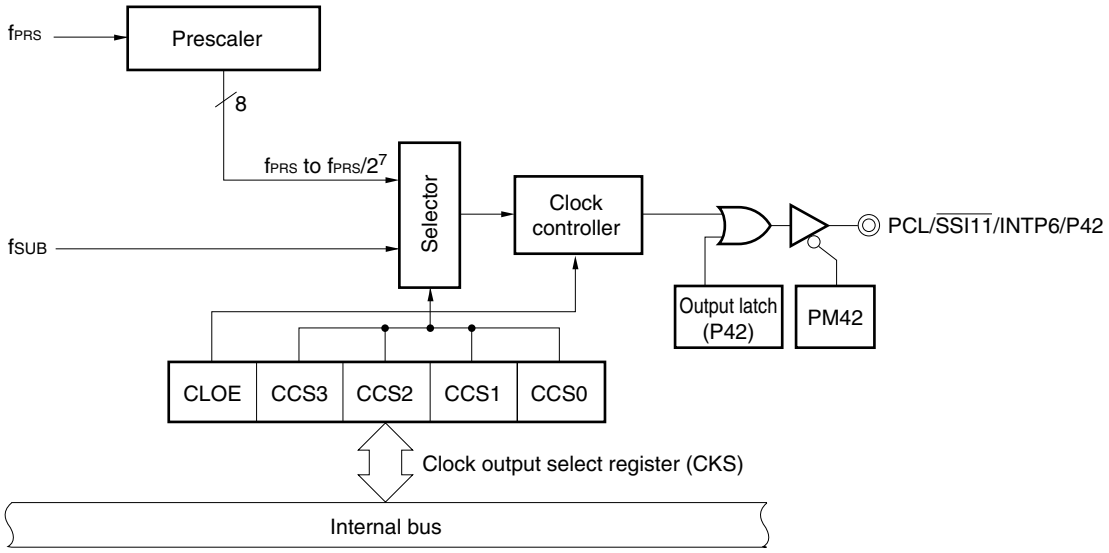
**Remark** √: Mounted, –: Not mounted

## 11.1 Functions of Clock Output Controller

The clock output controller is intended for carrier output during remote controlled transmission and clock output for supply to peripheral ICs. The clock selected with the clock output selection register (CKS) is output.

Figure 11-1 shows the block diagram of clock output controller.

**Figure 11-1. Block Diagram of Clock Output Controller (48-pin products of 78K0/KC2-L)**




## 11.2 Configuration of Clock Output Controller

The clock output controller includes the following hardware.

**Table 11-1. Configuration of Clock Output Controller**

| Item | Configuration |
|---|---|
| Control registers | Clock output selection register (CKS)<br>Port mode register 4 (PM4)<br>Port register 4 (P4) |

**Table 12-2. A/D Conversion Time Selection (1/3)**

**(1) 4.0 V ≤ $AV_{REF}$ ≤ 5.5 V**

| A/D Converter Mode Register 0 (ADM0) | | | | | Mode | Conversion Time Selection | | | | Conversion Clock ($f_{AD}$) |
|---|---|---|---|---|---|---|---|---|---|---|
| FR2 | FR1 | FR0 | LV1 | LV0 | | | $f_{PRS}$ = 4 MHz | $f_{PRS}$ = 8 MHz | $f_{PRS}$ = 10 MHz | |
| 0 | 0 | 0 | 0 | 0 | Standard | 264/$f_{PRS}$ | 66.0 μs | 33.0 μs | 26.4 μs | $f_{PRS}$/12 |
| 0 | 0 | 1 | | | | 176/$f_{PRS}$ | 44.0 μs | 22.0 μs | 17.6 μs | $f_{PRS}$/8 |
| 0 | 1 | 0 | | | | 132/$f_{PRS}$ | 33.0 μs | 16.5 μs | 13.2 μs | $f_{PRS}$/6 |
| 0 | 1 | 1 | | | | 88/$f_{PRS}$ | 22.0 μs | 11.0 μs | 8.8 μs | $f_{PRS}$/4 |
| 1 | 0 | 0 | | | | 66/$f_{PRS}$ | 16.5 μs | 8.25 μs | 6.6 μs | $f_{PRS}$/3 |
| 1 | 0 | 1 | | | | 44/$f_{PRS}$ | 11.0 μs | Setting prohibited | | $f_{PRS}$/2 |
| 1 | 1 | 0 | | | | 33/$f_{PRS}$ | 8.25 μs | Setting prohibited | | $f_{PRS}$/1.5 |
| 1 | 1 | 1 | | | | 22/$f_{PRS}$ | Setting prohibited | | | $f_{PRS}$ |
| 1 | 0 | 1 | 1 | 1 | High-speed 2 | 44/$f_{PRS}$ | 11.0 μs | 5.5 μs | 4.4 μs | $f_{PRS}$/2 |
| 1 | 1 | 1 | | | | 22/$f_{PRS}$ | 5.5 μs | Setting prohibited | | $f_{PRS}$ |
| 1 | 0 | 0 | 1 | 0 | High-speed 1 | 66/$f_{PRS}$ | 16.5 μs | 8.25 μs | 6.6 μs | $f_{PRS}$/3 |
| 1 | 1 | 0 | | | | 33/$f_{PRS}$ | 8.25 μs | 4.125 μs | 3.3 μs | $f_{PRS}$/1.5 |
| Other than above | | | | | Setting prohibited | | | | | |

**Cautions 1. When rewriting FR2 to FR0, LV1, and LV0 to other than the same data, stop A/D conversion once (ADCS = 0) beforehand.**

**2. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.**

**Remark** $f_{PRS}$: Peripheral hardware clock frequency

<R> **Figure 12-12. Format of Port Mode Register 7 (PM7) (78K0/KA2-L (32-pin products))**

Address: FF27H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM7 | 1 | 1 | 1 | 1 | 1 | PM72 | PM71 | PM70 |

| PM7n | P7n pin I/O mode selection (n = 0 to 2) |
|---|---|
| 0 | Output mode (output buffer on) |
| 1 | Input mode (output buffer off) |

**Figure 13-4. Format of A/D Port Configuration Register 0 (ADPC0)**

**(a) 78K0/KY2-L**

Address: FF2EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC0 | 0 | 0 | 0 | 0 | ADPCS3 | ADPCS2 | ADPCS1 | ADPCS0 |

**(b) 78K0/KA2-L (20-pin products)**

Address: FF2EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC0 | 0 | 0 | ADPCS5 | ADPCS4 | ADPCS3 | ADPCS2 | ADPCS1 | ADPCS0 |

**(c) 78K0/KA2-L (25-pin products)**

Address: FF2EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC0 | 0 | ADPCS6 | ADPCS5 | ADPCS4 | ADPCS3 | ADPCS2 | ADPCS1 | ADPCS0 |

**(d) 78K0/KA2-L (32-pin products)**

Address: FF2EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC0 | ADPCS7 | ADPCS6 | ADPCS5 | ADPCS4 | ADPCS3 | ADPCS2 | ADPCS1 | ADPCS0 |

**(e) 78K0/KB2-L**

Address: FF2EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC0 | 0 | 0 | 0 | 0 | ADPCS3 | ADPCS2 | ADPCS1 | ADPCS0 |

**(f) 78K0/KC2-L (40-pin products)**

Address: FF2EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC0 | 0 | ADPCS6 | ADPCS5 | ADPCS4 | ADPCS3 | ADPCS2 | ADPCS1 | ADPCS0 |

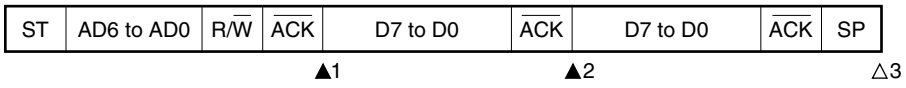
**(g) 78K0/KC2-L (44-pin and 48-pin products)**

Address: FF2EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC0 | ADPCS7 | ADPCS6 | ADPCS5 | ADPCS4 | ADPCS3 | ADPCS2 | ADPCS1 | ADPCS0 |

| ADPCSn | Digital I/O or analog I/O selection (n = 0 to 7) |
|---|---|
| 0 | Analog I/O |
| 1 | Digital I/O |

**(ii) When WTIM0 = 1**

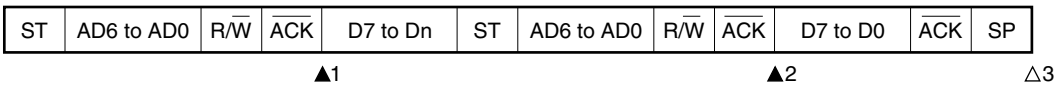



▲1: IICAS0 = 10001110B
▲2: IICAS0 = 01000100B
△3: IICAS0 = 00000001B

**Remark** ▲: Always generated
△: Generated only when SPIE0 = 1

**(d) When loss occurs due to restart condition during data transfer**

**(i) Not extension code (Example: unmatches with SVA0)**

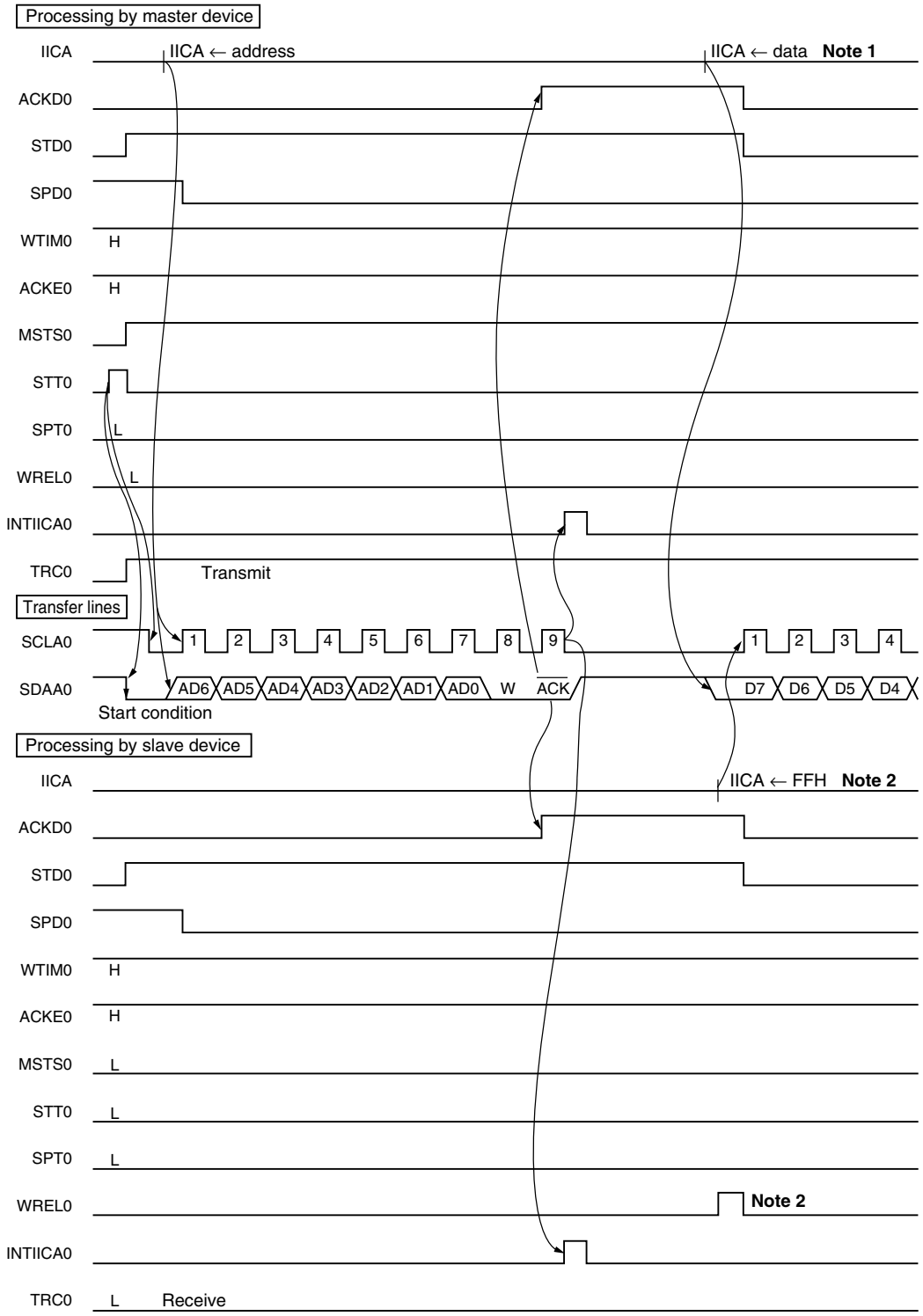



▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 01000110B
△3: IICAS0 = 00000001B

**Remark** ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care
n = 6 to 0

**Figure 15-33. Example of Master to Slave Communication**
**(When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)**

**(1) Start condition ~ address**




**Notes 1.** Write data to IICA, not setting WREL0, in order to cancel a wait state during master transmission.

**2.** To cancel slave wait, write “FFH” to IICA or set WREL0.

## 17.3 Registers Controlling Interrupt Functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H)
- Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H)
- Priority specification flag registers (PR0L, PR0H, PR1L, PR1H)
- External interrupt rising edge enable registers (EGPCTL0, EGPCTL1)
- External interrupt falling edge enable registers (EGNCTL0, EGNCTL1)
- Program status word (PSW)

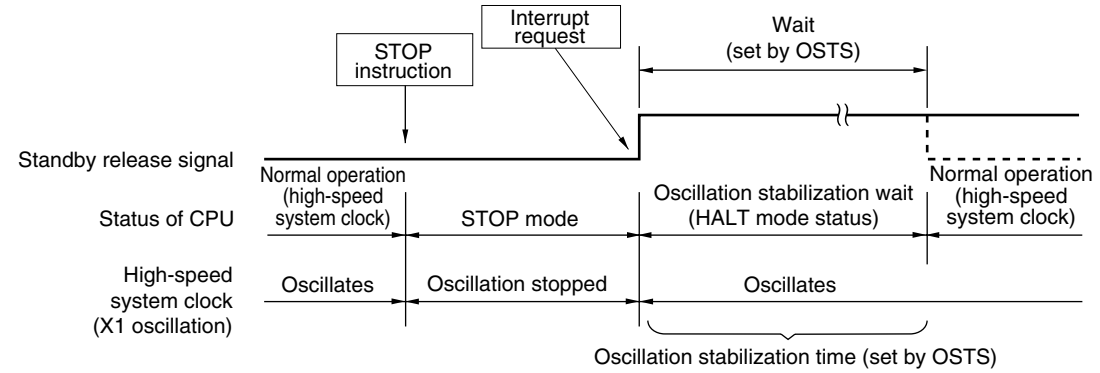
Table 17-2 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

<R> **Table 17-2. Flags Corresponding to Interrupt Request Sources (1/2)**

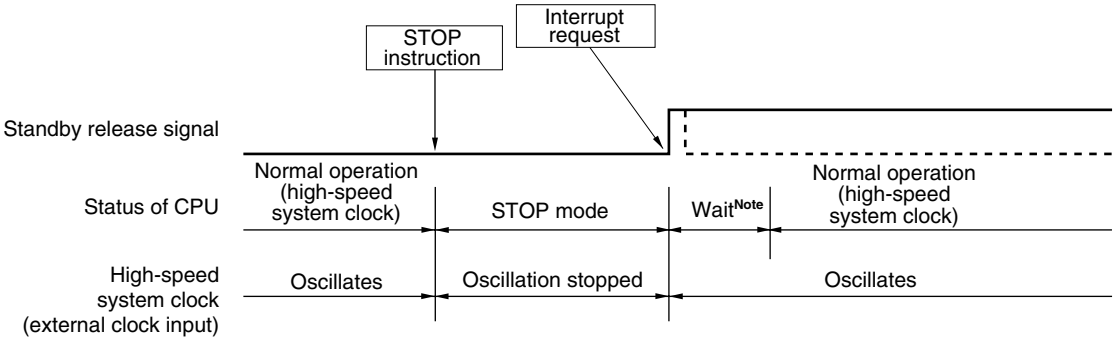
| KY 2-L | KA 2-L | | KB 2-L | KC2-L | | | Interrupt Source | Interrupt Request Flag | | Interrupt Mask Flag | | Priority Specification Flag | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Register | | Register | | Register |
| 16 pins | 20 pins | 25, 32 pins | 30 pins | 40 pins | 44 pins | 48 pins | | | | | | | |
| √ | √ | √ | √ | √ | √ | √ | INTLVI | LVIIF | IF0L | LVIMK | MK0L | LVIPR | PR0L |
| √ | √ | √ | √ | √ | √ | √ | INTP0 | PIF0 | | PMK0 | | PPR0 | |
| √ | √ | – | √ | √ | √ | √ | INTP1 | PIF1 | | PMK1 | | PPR1 | |
| – | √ | √ | √ | √ | √ | √ | INTP2 | PIF2 | | PMK2 | | PPR2 | |
| – | √ | √ | √ | √ | √ | √ | INTP3 | PIF3 | | PMK3 | | PPR3 | |
| – | – | √ | √ | √ | √ | √ | INTP4 | PIF4 | | PMK4 | | PPR4 | |
| – | – | √ | √ | √ | √ | √ | INTP5 | PIF5 | | PMK5 | | PPR5 | |
| √ | √ | √ | √ | √ | √ | √ | INTSRE6 | SREIF6 | | SREMK6 | | SREPR6 | |
| √ | √ | √ | √ | √ | √ | √ | INTSR6 | SRIF6 | IF0H | SRMK6 | MK0H | SRPR6 | PR0H |
| √ | √ | √ | √ | √ | √ | √ | INTST6 | STIF6 | | STMK6 | | STPR6 | |
| – | – | – | √ | √ | √ | √ | INTCSI10 | CSIIF10 | | CSIMK10 | | CSIPR10 | |
| – | – | √ | – | – | – | – | INTCSI11 | CSIIF11 | | CSIMK11 | | CSIPR11 | |
| √ | √ | √ | √ | √ | √ | √ | INTTMH1 | TMIFH1 | | TMMKH1 | | TMPRH1 | |
| – | – | – | √ | √ | √ | √ | INTTMH0 | TMIFH0 | | TMMKH0 | | TMPRH0 | |
| – | – | – | √ | √ | √ | √ | INTTM50 | TMIF50 | | TMMK50 | | TMPR50 | |
| √ | √ | √ | √ | √ | √ | √ | INTTM000 | TMIF000 | | TMMK000 | | TMPR000 | |
| √ | √ | √ | √ | √ | √ | √ | INTTM010 | TMIF010 | | TMMK010 | | TMPR010 | |

**Figure 19-6. STOP Mode Release by Interrupt Request Generation (1/2)**

**(1) When high-speed system clock (X1 oscillation) is used as CPU clock**




**(2) When high-speed system clock (external clock input) is used as CPU clock**




**Note** The wait time is as follows:

- When vectored interrupt servicing is carried out: 17 or 18 clocks
- When vectored interrupt servicing is not carried out: 11 or 12 clocks

**Remark** The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

## 25.8 Flash Memory Programming by Self Programming

The 78K0/Kx2-L microcontrollers support a self programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the 78K0/Kx2-L microcontroller self programming library, it can be used to upgrade the program in the field.

If an interrupt occurs during self programming, self programming can be temporarily stopped and interrupt servicing can be executed. If an unmasked interrupt request is generated in the EI state, the request branches directly from the self programming library to the interrupt routine. After the self programming mode is later restored, self programming can be resumed. However, the interrupt response time is different from that of the normal operation mode.

**Cautions 1. The self programming function cannot be used when the CPU operates with the subsystem clock.**

**2. To prohibit an interrupt during self programming, in the same way as in the normal operation mode, execute the self programming library in the state where the IE flag is cleared (0) by the DI instruction. To enable an interrupt, clear (0) the interrupt mask flag to accept in the state where the IE flag is set (1) by the EI instruction, and then execute the self programming library.**

**3. Make sure that the regulator output voltage mode is fixed when executing self programming or EEPROM emulation.**

**4. The power supply voltage range in which the flash memory can be rewritten in normal power mode is $V_{DD} \geq 2.5$ V. Note that program area can be rewritten by using the self programming library in normal power mode.**

**5. Observe the following points when rewriting the flash memory in low power consumption mode:**

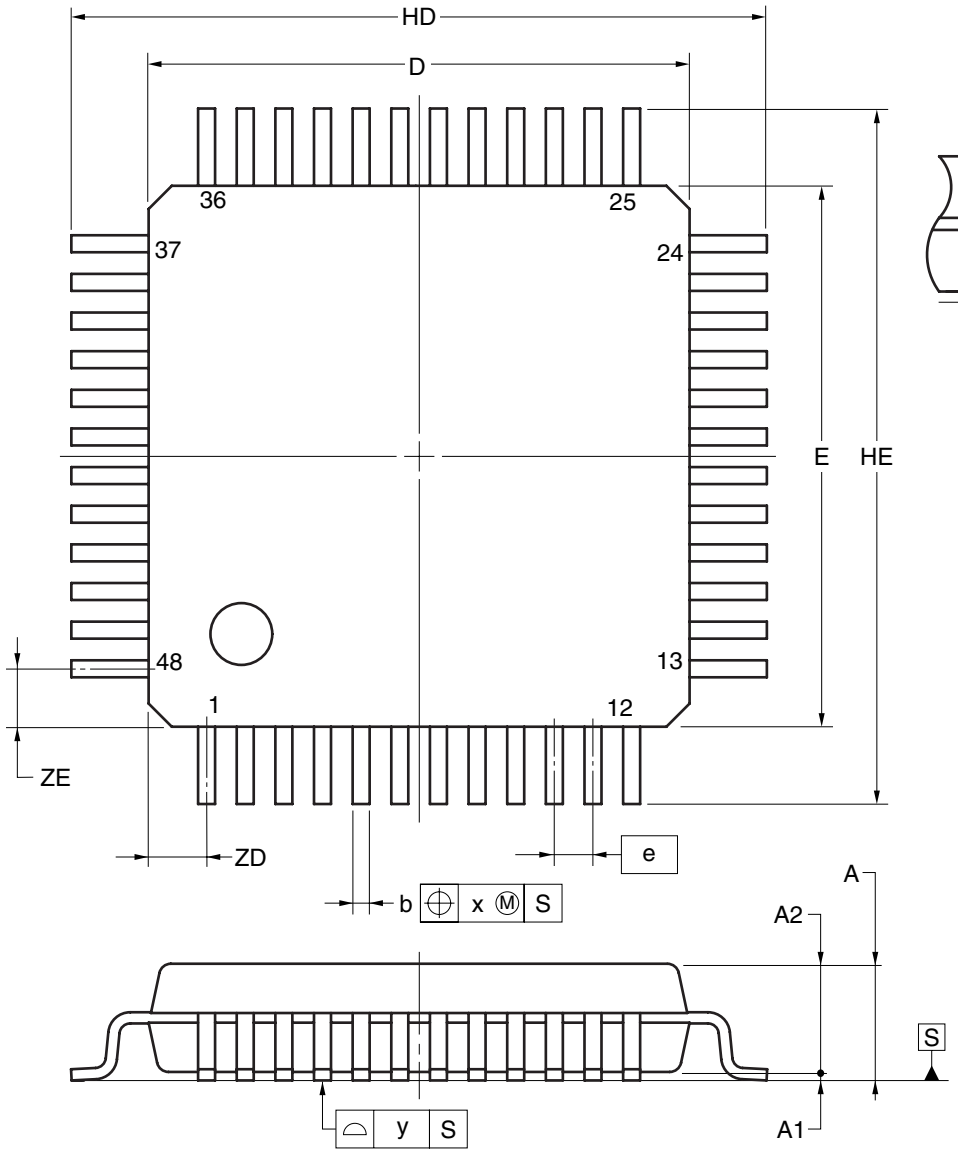
- **Data area can be rewritten in low power consumption mode, but program area cannot.**
  **Data area: Flash memory area handled as data**
  **Program area: Flash memory area handled as the program**
- **The flash memory cannot be rewritten in low power consumption mode if the power supply voltage is 2.0 V or lower.**
- **Flash memory that is erased and written in low power consumption mode cannot be accessed in normal power mode. To use this data in normal power mode, switch to low power consumption mode and transfer the flash memory contents to RAM.**
- **Blocks cannot be overwritten by using the self programming library. Be sure to erase a block first before rewriting data to it.**
- **A wait time of 2 ms is required before executing self programming after switching from normal power mode to low power consumption mode.**

<R> **Remark** For details of the self programming function and the self programming library, refer to **"78K0 Microcontrollers User's Manual Self Programming Library Type 01 (U18274E)"** and **"78K0 Microcontrollers Self Programming Library Type 01 Ver. 3.10 Operating Precautions (notification document) (ZUD-CD-09-0122)"**.

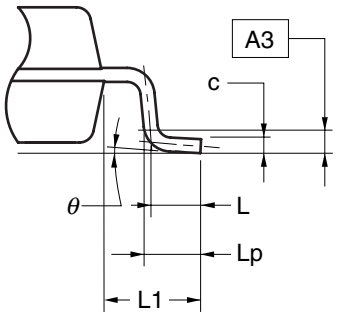
For details of the EEPROM emulation library, refer to **"78K0 Microcontrollers User's Manual EEPROM Emulation Library Type 01 (U18275E)"** and **"78K0 Microcontrollers EEPROM Emulation Library Type 01 Ver.2.10 Operating Precautions (notification document) (ZUD-CD-09-0165)"**.

- μPD78F0581GA-GAM-AX, 78F0582GA-GAM-AX, 78F0583GA-GAM-AX, 78F0586GA-GAM-AX, 78F0587GA-GAM-AX, 78F0588GA-GAM-AX

## 48-PIN PLASTIC LQFP (FINE PITCH) (7x7)




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 7.00±0.20 |
| E | 7.00±0.20 |
| HD | 9.00±0.20 |
| HE | 9.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.20^{+0.07}_{-0.03}$ |
| c | $0.125^{+0.075}_{-0.025}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 0.75 |
| ZE | 0.75 |

P48GA-50-GAM

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

(3/8)

| Edition | Description | Chapter |
|---|---|---|
| 2nd Edition | Modification of **Table 12-3 Setting Functions of P10/ANI8/AMP1-, P12/ANI10/AMP1+ Pins** | **CHAPTER 12 A/D CONVERTER** |
| | Modification of **Table 12-5 Setting Functions of P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins** | |
| | Deletion of **Caution 2** in **12.4.1 Basic operations of A/D converter** | |
| | Modification of description of setting methods and deletion of **Caution 2** in **12.4.3 (1) A/D conversion operation** | |
| | Modification of **Figure 13-1 Block Diagram of Operational Amplifier** | **CHAPTER 13 OPERATIONAL AMPLIFIERS** |
| | Addition of **Remark** to **Figure 13-2 Format of Operational Amplifier 0 Control Register (AMP0M) (Products with Operational Amplifier Only)** | |
| | Modification of **Figure 13-4 Format of A/D Port Configuration Register 0 (ADPC0)** | |
| | Modification of **Figure 13-5 Format of A/D Port Configuration Register 1 (ADPC1) (78K0/KB2-L and 78K0/KC2-L Only)** | |
| | Modification of **Table 13-2 Setting Functions of P10/ANI8/AMP1-, P12/ANI10/AMP1+ Pins** | |
| | Modification of **Table 13-4 Setting Functions of P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins** | |
| | Modification of **Remark** in **Figure 14-4 Block Diagram of Serial Interface UART6** | **CHAPTER 14 SERIAL INTERFACE UART6** |
| | Addition of **Note 3** to **Figure 14-8 Format of Clock Selection Register 6 (CKSR6)** | |
| | Modification of description in **14.3 (8) Port mode register 1 (PM1), port mode register 6 (PM6)** | |
| | Modification of **(1) 78K0/KY2-L and 78K0/KA2-L** in **Table 14-2 Relationship Between Register Settings and Pins** | |
| | Addition of **15.4.2 Setting transfer clock by using IICWL and IICWH registers** | **CHAPTER 15 SERIAL INTERFACE IICA** |
| | Modification of the mounted situation in the 78K0/KB2-L and 78K0/KC2-L | **CHAPTER 16 SERIAL INTERFACES CSI10 AND CSI11** |
| | Modification of description in **16.3 (4) Port mode registers 1, 4, 6, 12 (PM1, PM4, PM6, PM12)** | |
| | Modification of and addition of **Notes 3** and **4** to **Table 16-3 SO1n Output Status** | |
| | Modification of maskable interrupts (internal) in the 78K0/KB2-L and 78K0/KC2-L | **CHAPTER 17 INTERRUPT FUNCTIONS** |
| | Modification of **Table 17-1 Interrupt Source List (1/2)** | |
| | Modification of **Table 17-2 Flags Corresponding to Interrupt Request Sources (1/2)** | |
| | Modification of **Caution** in **Figure 17-4 Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (78K0/KB2-L)** to **Figure 17-6 Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (48-pin products of 78K0/KC2-L)** | |
| | Modification of **Caution** in **Figure 17-9 Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (78K0/KB2-L)** to **Figure 17-11 Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (48-pin products of 78K0/KC2-L)** | |

**Remark** "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

(6/8)

| Edition | Description | Chapter |
|---|---|---|
| 3rd Edition | Modification of **Related Documents** | **INTRODUCTION** |
| | Modification of description in **1.1 Features** | **CHAPTER 1 OUTLINE** |
| | Modification of **Caution 1** in **1.3.3 78K0/KB2-L** and **1.3.4 78K0/KC2-L** | |
| | Modification of **Caution 1** in **1.4.3 78K0/KB2-L** and **1.4.4 78K0/KC2-L** | |
| | Modification of description in **1.5 Outline of Functions** | |
| | Modification of **Table 3-6 Special Function Register List: 78K0/KY2-L** to **Table 3-9 Special Function Register List: 78K0/KC2-L** | **CHAPTER 3 CPU ARCHITECTURE** |
| | Modification of **Table 4-10 Setting Functions of P21/ANI1/AMP0OUT/PGAIN Pin** | **CHAPTER 4 PORT FUNCTIONS** |
| | Addition of description to **4.3 (5) Port output mode register 6 (POM6)** | |
| | Addition of **Caution 5** to **Table 4-12 Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KY2-L) (1/2)** | |
| | Addition of **Caution 5** to **Table 4-13 Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KA2-L) (1/2)** | |
| | Addition of **Caution 1** to **Figure 5-8 Format of Main OSC Control Register (MOC)** | **CHAPTER 5 CLOCK GENERATOR** |
| | Addition of **Caution 1** to **Figure 5-12 Format of Peripheral Enable Register 0 (PER0)** | |
| | Modification of **Figure 5-16 Clock Generator Operation When Power Supply Voltage Is Turned On, (When LVI Default Start Function Stopped Is Set (Option Byte: LVISTART = 0))** and **Figure 5-17 Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Enabled Is Set (Option Byte: LVISTART = 1))** | |
| | Modification of **Figure 7-2 Block Diagram of 8-Bit Timer 51 (78K0/KY2-L, 78K0/KA2-L)** | **CHAPTER 7 8-BIT TIMER/EVENT COUNTERS 50 AND 51** |
| | Addition of the port mode register 4 (PM4) and the port register 4 (P4) to **Table 10-1 Configuration of Real-Time Counter** | **CHAPTER 10 REAL-TIME COUNTER** |
| | Addition of **Caution 1** to **Figure 10-2 Format of Peripheral Enable Register 0 (PER0)** | |
| | Addition of the port mode register 4 (PM4) and the port register 4 (P4) to **10.3 Registers Controlling Real-Time Counter** | |
| | Modification of **Figure 10-3 Format of Real-Time Counter Control Register 0 (RTCC0)** | |
| | Modification of **Figure 10-4 Format of Real-Time Counter Control Register 0 (RTCC1)** | |
| | Modification of description in **(7) Minute count register (MIN), (8) Hour count register (HOUR), (9) Day count register (DAY), (11) Month count register (MONTH), (12) Year count register (YEAR)** | |
| | Modification of **Figure 10-14 Format of Watch Error Correction Register (SUBCUD)** | |
| | Modification of **Figure 10-19 Procedure for Starting Operation of Real-Time Counter** | |
| | Addition of **10.4.2 Shifting to STOP mode after starting operation** | |
| | Modification of **Figure 10-26 512 Hz, 16.384 kHz output Setting Procedure** | |
| | Modification of **(2) 2.7 V ≤ $AV_{REF}$ < 4.0 V** in **Table 12-2 A/D Conversion Time Selection** | **CHAPTER 12 A/D CONVERTER** |
| | Modification of **Caution 3** in **Figure 12-8 Format of Analog Input Channel Specification Register (ADS)** | |

**Remark** "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents