Renesas Electronics America Inc - UPD78F0562MC-CAA-AX Datasheet

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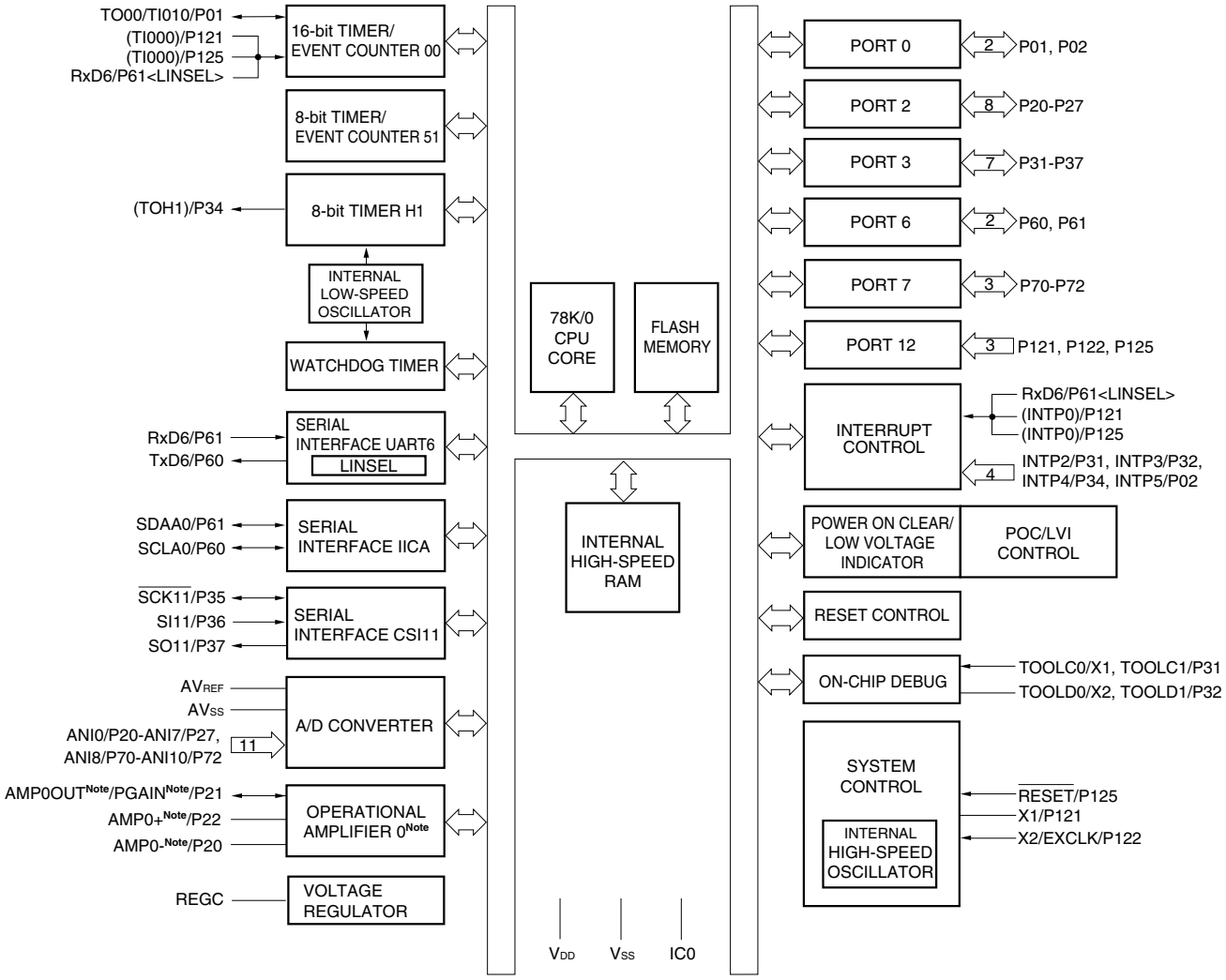
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0562mc-caa-ax

<R> **(3) 32-pin products**



Note μPD78F0565, 78F0566, 78F0567 (products with operational amplifier) only

Cautions 1. Connect directly IC0 (Internally Connected) to V_{SS}.

2. V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

4. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, ANI3/P23 to ANI7/P27, and ANI8/P70 to ANI10/P72 are set in the analog input mode after release of reset.

5. $\overline{\text{RESET}}$/P125 immediately after release of reset is set in the external reset input.

6. Set P30 to output mode (PM30 = 0) by using software after release of reset.

Remark Functions in parentheses ( ) in the figure above can be assigned by setting the port alternate switch control register (MUXSEL).

(2) Non-port functions: 78K0/KC2-L (4/4)

Function Name	I/O	Function	After Reset	Alternate Function
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input port	P17/TO50
TI51		External count clock input to 8-bit timer/event counter 51		P33/TO51/INTP4
TO00	Output	16-bit timer/event counter 00 output	Input port	P01/TI010
TO50	Output	8-bit timer/event counter 50 output	Input port	P17/TI50
TO51		8-bit timer/event counter 51 output		P33/TI51/INTP4
TOH0	Output	8-bit timer H0 output	Input port	P15
TOH1		8-bit timer H1 output		P16/INTP5
X1	–	Connecting resonator for main system clock	Input port	P121/TOOLC0
X2				P122/EXCLK/TOOLD0
EXCLK	Input	External clock input for main system clock	Input port	P122/X2/TOOLD0
XT1	–	Connecting resonator for subsystem clock	Input port	P123
XT2				P124/EXCLKS
EXCLKS	Input	External clock input for subsystem clock	Input port	P124/XT2
V_{DD}	–	Positive power supply for pins other than port 2	–	–
AV_{REF}	–	A/D converter reference voltage input and positive power supply for port 2 and A/D converter	–	–
V_{SS}	–	Ground potential for pins other than port 2	–	–
AV_{SS}		Ground potential for port 2 and A/D converter		
TOOLC0	Input	Clock input for flash memory programmer/on-chip debugger	Input port	P121/X1
TOOLC1				P31/INTP2
TOOLD0	I/O	Data I/O for flash memory programmer/on-chip debugger		P122/X2/EXCLK
TOOLD1				P32/INTP3
IC	–	Internally connected. Leave open.	–	–

(e) SO10

This is a serial data output pin of serial interface CSI10.

(f) $\overline{\text{SCK10}}$

This is a serial clock I/O pin of serial interface CSI10.

(g) RxD6

This is a serial data input pin of serial interface UART6.

(h) TxD6

This is a serial data output pin of serial interface UART6.

(i) TI50

This is a pin for inputting an external count clock to 8-bit timer/event counter 50.

(j) TO50

This is a timer output pin of 8-it timer/event counter 50.

(k) TOH0, TOH1

These are a timer output pins of 8-bit timers H0 and H1.

(l) INTP5

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

2.2.3 P20 to P27 (port 2)

P20 to P27 function as an I/O port. These pins also function as pins for A/D converter analog input, operational amplifier I/O, and PGA input.

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78K0/KY2-L (μPD78F055x)	78K0/KA2-L (μPD78F056x)			78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)		
16 Pins	20 Pins	25 Pins	32 Pins	30 Pins	40 Pins	44 Pins	48 Pins
P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note	P20/ANI0/ AMP0-Note
P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote	P21/ANI1/ AMP0OUTNote/ PGAINNote
P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note	P22/ANI2/ AMP0+Note
P23/ANI3	P23/ANI3	P23/ANI3	P23/ANI3	P23/ANI3	P23/ANI3	P23/ANI3	P23/ANI3
–	P24/ANI4	P24/ANI4	P24/ANI4	–	P24/ANI4	P24/ANI4	P24/ANI4
–	P25/ANI5	P25/ANI5	P25/ANI5	–	P25/ANI5	P25/ANI5	P25/ANI5
–	–	P26/ANI6	P26/ANI6	–	P26/ANI6	P26/ANI6	P26/ANI6
–	–	–	P27/ANI7	–	–	P27/ANI7	P27/ANI7

Note Products with operational amplifier only

The following operation modes can be specified in 1-bit units.

3.3.2 Immediate addressing

[Function]

Immediate data in the instruction word is transferred to the program counter (PC) and branched.

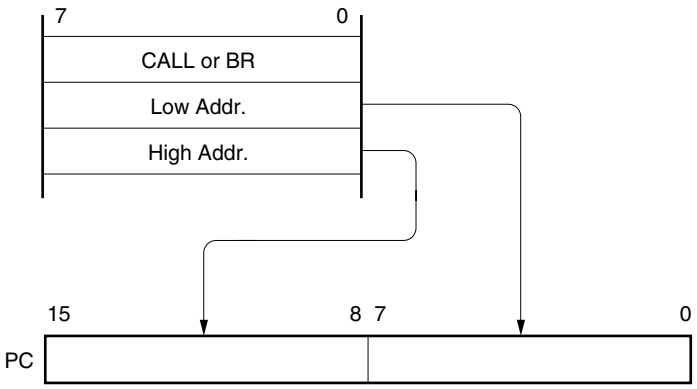
This function is carried out when the CALL !addr16 or BR !addr16 or CALLF !addr11 instruction is executed.

CALL !addr16 and BR !addr16 instructions can be branched to the entire memory space.

The CALLF !addr11 instruction is branched to the 0800H to 0FFFH area.

[Illustration]

In the case of CALL !addr16 and BR !addr16 instructions



In the case of CALLF !addr11 instruction

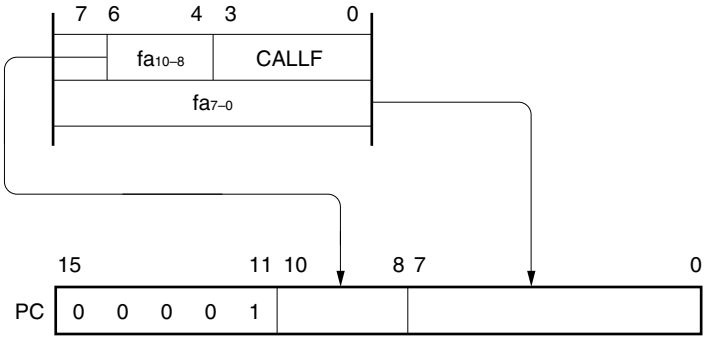
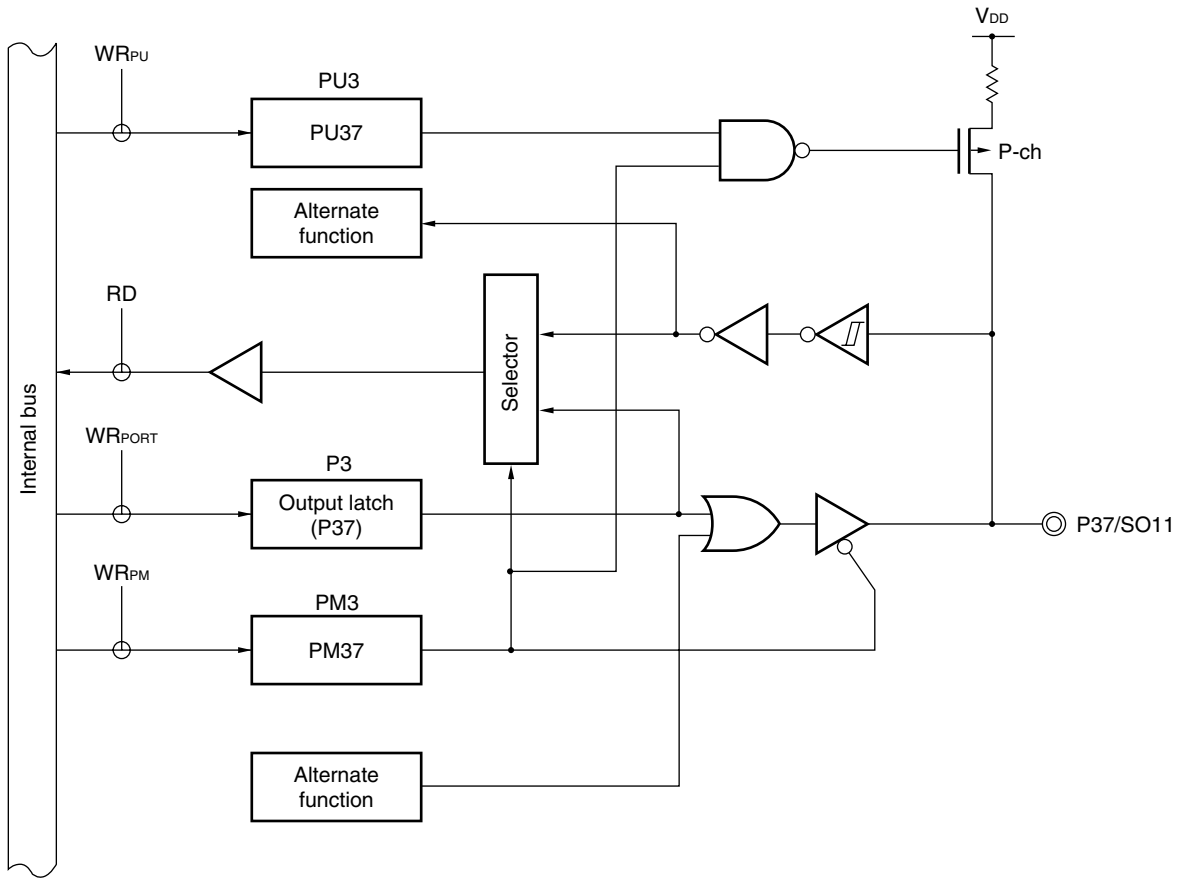
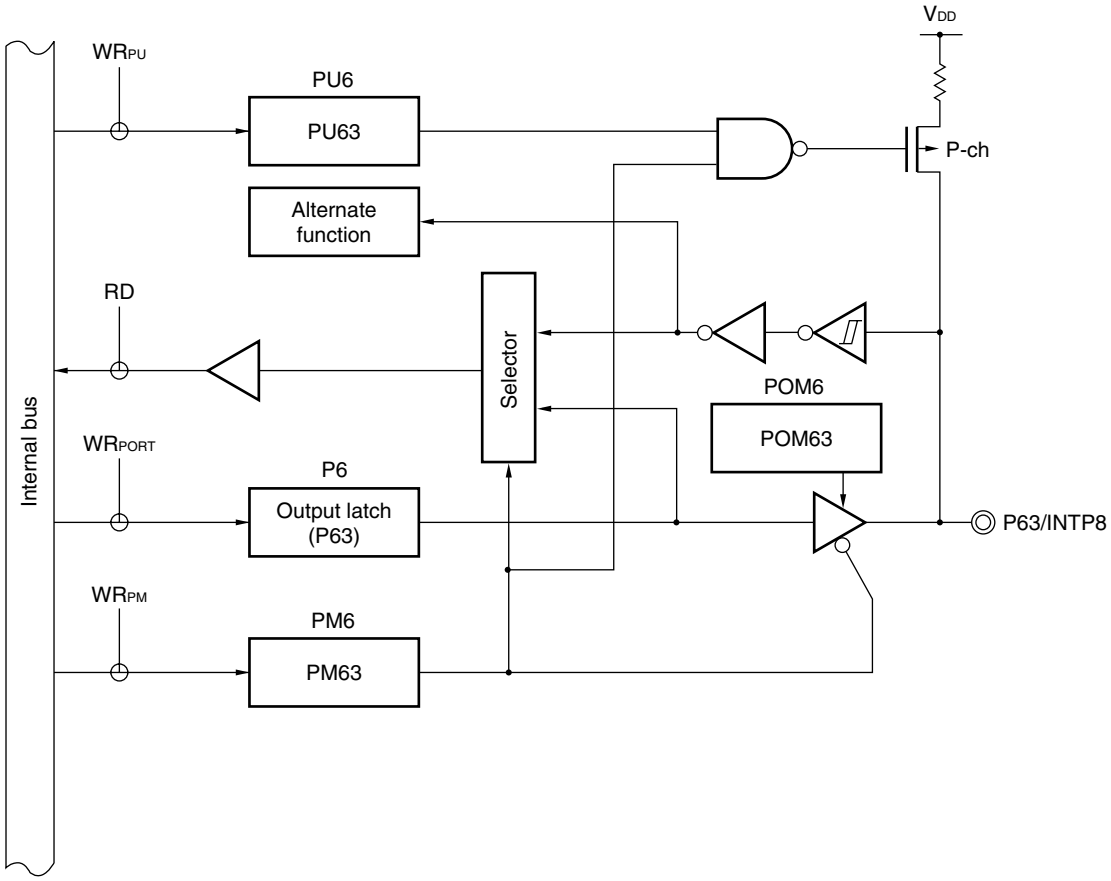


Figure 4-17. Block Diagram of P37



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Figure 4-25. Block Diagram of P63



P6: Port register 6
PU6: Pull-up resistor option register 6
PM6: Port mode register 6
POM6: Port output mode register 6
RD: Read signal
WR××: Write signal

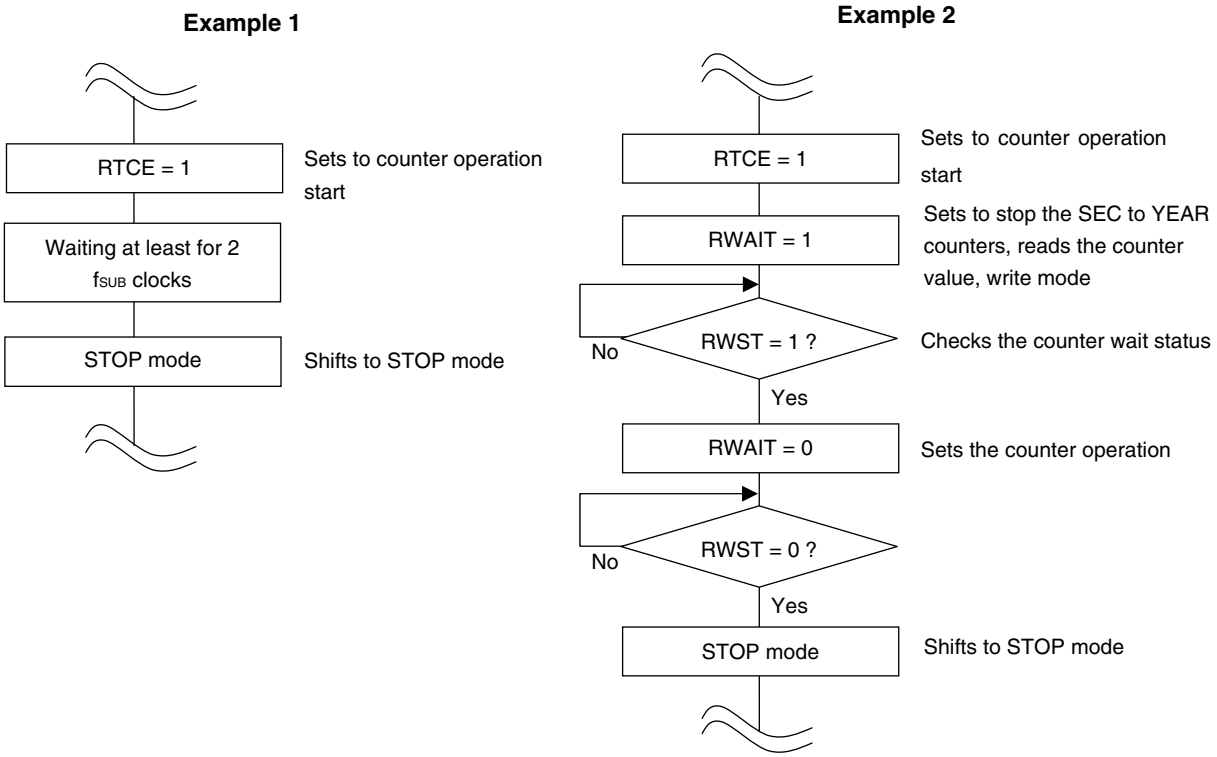
10.4.2 Shifting to STOP mode after starting operation

Perform one of the following processing when shifting to STOP mode immediately after setting RTCE to 1.

However, after setting RTCE to 1, this processing is not required when shifting to STOP mode after the first INTRTC interrupt has occurred.

- Shifting to STOP mode when at least two subsystem clocks (f_{SUB}) (about 62 μs) have elapsed after setting RTCE to 1 (see **Figure 10-20**, **Example 1**).
- Checking by polling RWST to become 1, after setting RTCE to 1 and then setting RWAIT to 1. Afterward, setting RWAIT to 0 and shifting to STOP mode after checking again by polling that RWST has become 0 (see **Figure 10-20**, **Example 2**).

Figure 10-20. Procedure for Shifting to STOP Mode After Setting RTCE to 1



CHAPTER 14 SERIAL INTERFACE UART6

14.1 Functions of Serial Interface UART6

Serial interface UART6 are mounted onto all 78K0/Kx2-L microcontroller products.
Serial interface UART6 has the following two modes.

(1) Operation stop mode

This mode is used when serial communication is not executed and can enable a reduction in the power consumption.
For details, refer to **14.4.1 Operation stop mode**.

(2) Asynchronous serial interface (UART) mode

This mode supports the LIN (Local Interconnect Network)-bus. The functions of this mode are outlined below.
For details, refer to **14.4.2 Asynchronous serial interface (UART) mode** and **14.4.3 Dedicated baud rate generator**.

- Maximum transfer rate: 625 kbps
- Two-pin configuration TxD6: Transmit data output pin
  RxD6: Receive data input pin
- Data length of communication data can be selected from 7 or 8 bits.
- Dedicated internal 8-bit baud rate generator allowing any baud rate to be set
- Transmission and reception can be performed independently (full duplex operation).
- MSB- or LSB-first communication selectable
- Inverted transmission operation
- Sync break field transmission from 13 to 20 bits
- More than 11 bits can be identified for sync break field reception (SBF reception flag provided).

Cautions 1. The TxD6 output inversion function inverts only the transmission side and not the reception side. To use this function, the reception side must be ready for reception of inverted data.

2. If clock supply to serial interface UART6 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART6 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD6 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER6 = 0, RXE6 = 0, and TXE6 = 0.

3. Set POWER6 = 1 and then set TXE6 = 1 (transmission) or RXE6 = 1 (reception) to start communication.

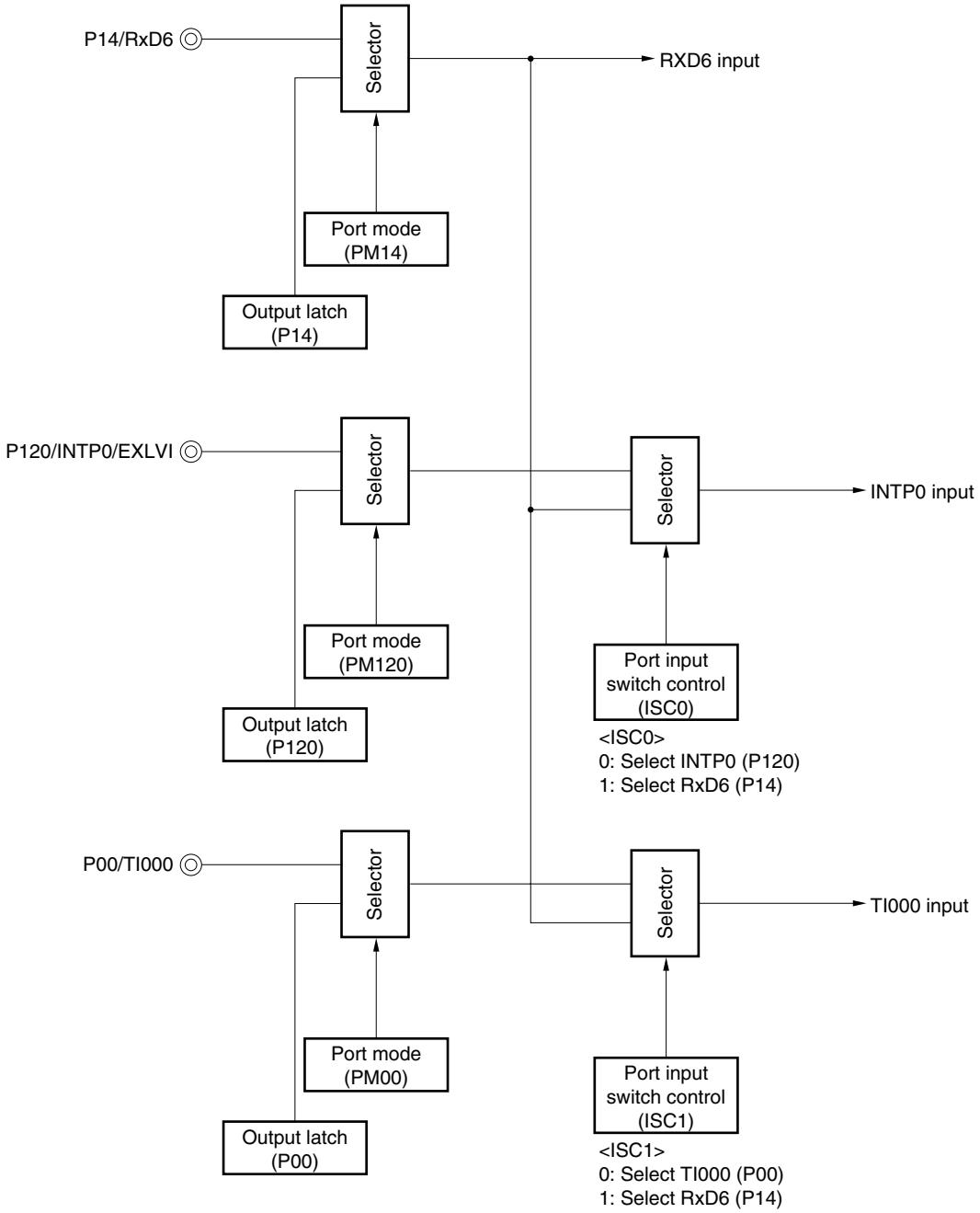
4. TXE6 and RXE6 are synchronized by the base clock (f_{XCLK6}) set by CKSR6. To enable transmission or reception again, set TXE6 or RXE6 to 1 at least two clocks of the base clock after TXE6 or RXE6 has been cleared to 0. If TXE6 or RXE6 is set within two clocks of the base clock, the transmission circuit or reception circuit may not be initialized.

5. Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.

6. If data is continuously transmitted, the communication timing from the stop bit to the next start bit is extended two operating clocks of the macro. However, this does not affect the result of communication because the reception side initializes the timing when it has detected a start bit. Do not use the continuous transmission function if the interface is used in LIN communication operation.

Figure 14-3. Port Configuration for LIN Reception Operation (2/2)

(2) 78K0/KB2-L and 78K0/KC2-L



Remark ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (refer to **Figure 14-11**)

Table 16-2. Relationship Between Register Settings and Pins (3/4)

(c) Serial interface CSI11 (CSISEL = 1) (78K0/KC2-L)

CSIE11	TRMD11	SSE11	PM41	P41	PM120	P120	PM40	P40	PM42	P42	CSI11 Operation	Pin Function			
												SI11/P41/RTC1HZ	SO11/P120/EXLVI/INTP0	$\overline{\text{SCK11}}$/P40/RTCCL/RTCDIV	$\overline{\text{SSI11}}$/P42/PCL/INTP6
0	0	×	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	Stop	P41/RTC1HZ	P120/EXLVI/INTP0	P40/RTCCL/RTCDIV Note 2	P42/PCL/INTP6
1	0	0	1	×	×Note 1	×Note 1	1	×	×Note 1	×Note 1	Slave reception Note 3	SI11	P120/EXLVI/INTP0	$\overline{\text{SCK11}}$ (input) Note 3	P42/PCL/INTP6
		1							1	×					$\overline{\text{SSI11}}$
1	1	0	×Note 1	×Note 1	0	0	1	×	×Note 1	×Note 1	Slave transmission Note 3	P41/RTC1HZ	SO11	$\overline{\text{SCK11}}$ (input) Note 3	P42/PCL/INTP6
		1							1	×					$\overline{\text{SSI11}}$
1	1	0	1	×	0	0	1	×	×Note 1	×Note 1	Slave transmission/reception Note 3	SI11	SO11	$\overline{\text{SCK11}}$ (input) Note 3	P42/PCL/INTP6
		1							1	×					$\overline{\text{SSI11}}$
1	0	0	1	×	×Note 1	×Note 1	0	1	×Note 1	×Note 1	Master reception	SI11	P120/EXLVI/INTP0	$\overline{\text{SCK11}}$ (output)	P42/PCL/INTP6
1	1	0	×Note 1	×Note 1	0	0	0	1	×Note 1	×Note 1	Master transmission	P41/RTC1HZ	SO11	$\overline{\text{SCK11}}$ (output)	P42/PCL/INTP6
1	1	0	1	×	0	0	0	1	×Note 1	×Note 1	Master transmission/reception	SI11	SO11	$\overline{\text{SCK11}}$ (output)	P42/PCL/INTP6

Notes 1. Can be set as port function.

2. To use P40/$\overline{\text{SCK11}}$/RTCCL/RTCDIV as port pins, clear CKP11 to 0.

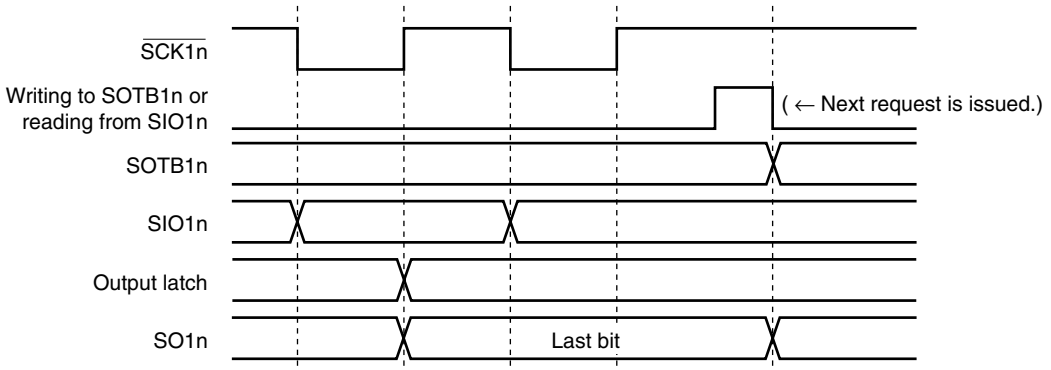
3. To use the slave mode, set CKS112, CKS111, and CKS110 to 1, 1, 1.

Remarks 1. ×: don't care
CSIE11: Bit 7 of serial operation mode register 11 (CSIM11)
TRMD11: Bit 6 of CSIM11
CKP11: Bit 4 of serial clock selection register 11 (CSIC11)
CKS112, CKS111, CKS110: Bits 2 to 0 of CSIC11
PM×: Port mode register
P×: Port output latch

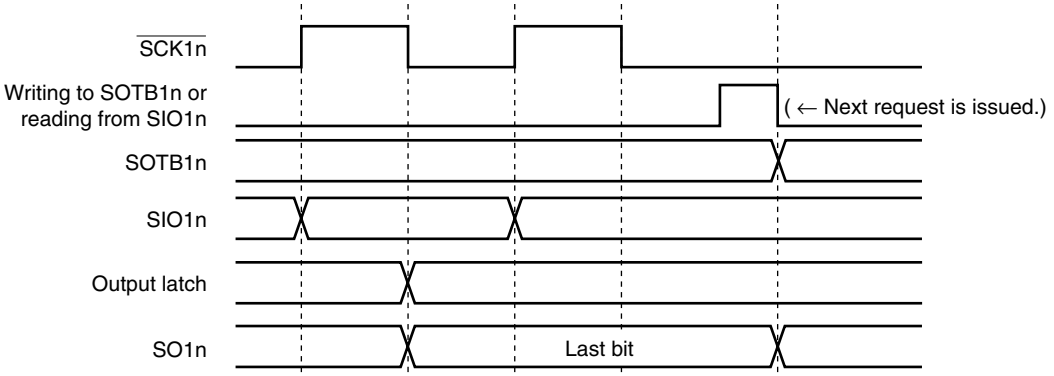
2. The $\overline{\text{SSI11}}$ pin is available only in 48-pin products of 78K0/KC2-L.

Figure 16-18. Output Value of SO1n Pin (Last Bit) (2/2)

(c) Type 2: CKP1n = 0, DAP1n = 1



(d) Type 4: CKP1n = 1, DAP1n = 1



Remark 78K0/KA2-L (25, 32-pin products): n = 1
78K0/KB2-L: n = 0
78K0/KC2-L: n = 0, 1

17.4 Interrupt Servicing Operations

17.4.1 Maskable interrupt acknowledgment

A maskable interrupt becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request (when the ISP flag is reset to 0).

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 17-4 below.

For the interrupt request acknowledgment timing, refer to **Figures 17-26** and **17-27**.

Table 17-4. Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time[Note]
When ××PR = 0	7 clocks	32 clocks
When ××PR = 1	8 clocks	33 clocks

Note If an interrupt request is generated just before a divide instruction, the wait time becomes longer.

Remark 1 clock: $1/f_{CPU}$ (f_{CPU}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

Figure 17-25 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP flag. The vector table data determined for each interrupt request is the loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

Cautions 1. To stop LVI, follow either of the procedures below.

- **When using 8-bit memory manipulation instruction: Write 00H to LVIM.**
- **When using 1-bit memory manipulation instruction: Clear LVION to 0.**

2. Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.

3. If LVI operation is disabled (clears LVION) when LVI is used in interrupt mode (LVIMD = 0), LVISEL is set to 0, and the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), or when LVI is used in interrupt mode (LVIMD = 0), LVISEL is set to 1, and input voltage of external input pin (EXLVI) is less than or equal to the detection voltage (V_{EXLVI})), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

4. For 78K0/KY2-L and 78K0/KA2-L, be sure to clear bit 2 to 0.

Figure 24-1. Format of Option Byte (2/3)

Address: 0081H/1081H[Notes 1, 2]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	LVISTART

<R>

LVISTART	LVI default start operation control
0	LVI is OFF by default upon power application (LVI default start function stopped)
1	LVI is ON by default upon power application (LVI default start function enabled)

Notes 1. LVISTART can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming. However, because 0080H and 1080H are switched during the boot swap operation, set a value that is the same as that of 0080H to 1080H.

2. To change the setting for the LVI default start, set the value to 0081H again after batch erasure (chip erasure) of the flash memory. The setting cannot be changed after the memory of the specified block is erased.

Caution Be sure to clear bits 7 to 1 to "0".

Address: 0082H/1082H[Note]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	R4M8MSEL

R4M8MSEL	Internal high-speed oscillation clock frequency selection
0	8 MHz (TYP.)
1	4 MHz (TYP.)

Note Set a value that is the same as that of 0082H to 1082H because 0082H and 1082H are switched during the boot swap operation.

Caution Be sure to clear bits 7 to 1 to "0".

Table 25-5. Flash Memory Control Commands

Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Chip Erase	Erases the entire flash memory.
	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased.
Write	Programming	Writes data to a specified area in the flash memory.
Getting information	Silicon Signature	Gets 78K0/Kx2-L information (such as the part number and flash memory configuration).
	Version Get	Gets the 78K0/Kx2-L version and firmware version.
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
Others	Reset	Used to detect synchronization status of communication.
	Baud Rate Set	Sets baud rate when UART communication mode is selected.

The 78K0/Kx2-L microcontrollers return a response for the command issued by the dedicated flash memory programmer. The response names sent from the 78K0/Kx2-L microcontrollers are listed below.

Table 25-6. Response Names

Response Name	Function
ACK	Acknowledges command/data.
NAK	Acknowledges illegal command/data.

Table 26-1. On-Chip Debug Security ID

Address	On-Chip Debug Security ID
0085H to 008EH	Any ID code of 10 bytes
1085H to 108EH	

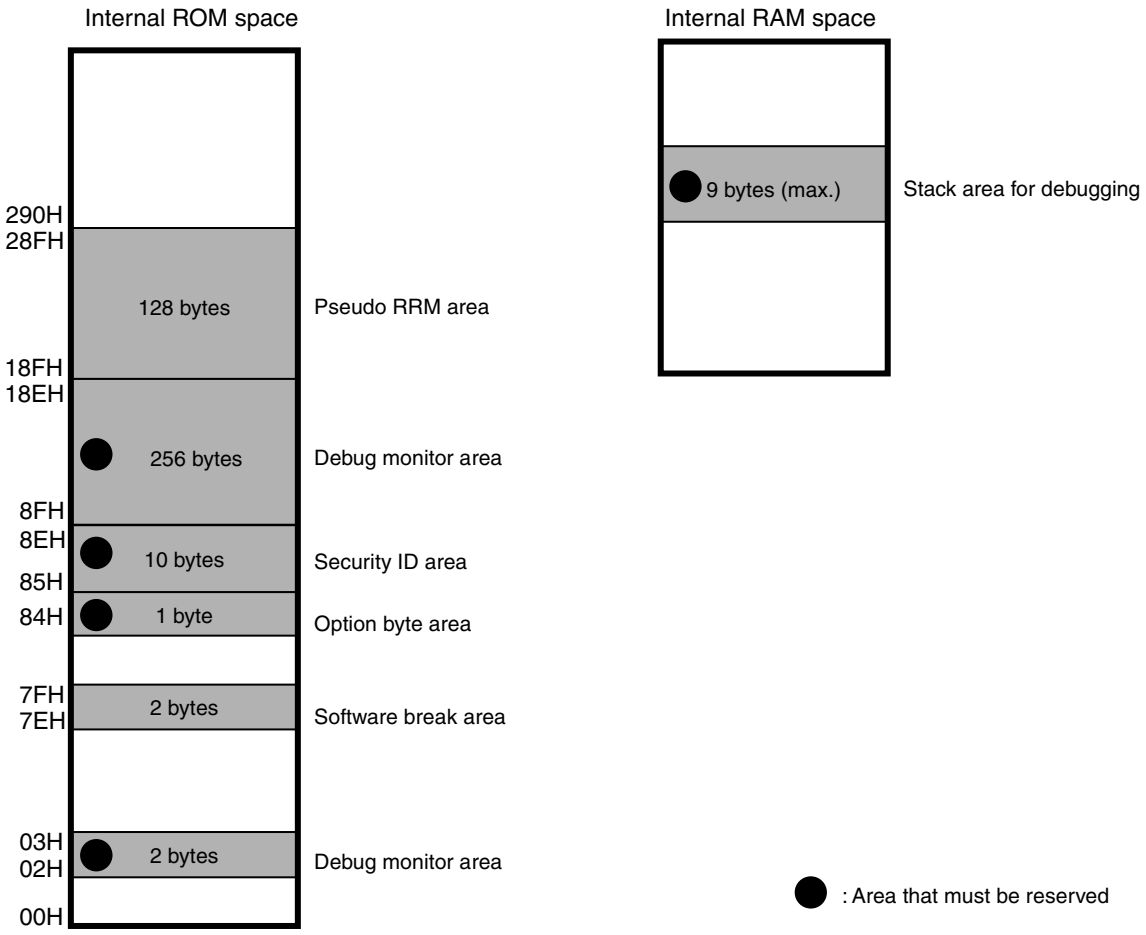
26.3 Securing of User Resources

QB-MINI2 uses the user memory spaces (shaded portions in Figure 26-2) to implement communication with the target device, or each debug functions. The areas marked with a dot (•) are always used for debugging, and other areas are used for each debug function used.

These areas can be secured by using user programs or the linker option.

For details on the securing of these areas, refer to the **QB-MINI2 On-Chip Debug Emulator with Programming Function User's Manual (U18371E)**.

Figure 26-2. Reserved Area Used by QB-MINI2



CHAPTER 28 ELECTRICAL SPECIFICATIONS

Target products: 78K0/KY2-L: μPD78F0550, 78F0551, 78F0552, 78F0555, 78F0556, 78F0557
78K0/KA2-L: μPD78F0560, 78F0561, 78F0562, 78F0565, 78F0566, 78F0567
78K0/KB2-L: μPD78F0571, 78F0572, 78F0573, 78F0576, 78F0577, 78F0578
78K0/KC2-L: μPD78F0581, 78F0582, 78F0583, 78F0586, 78F0587, 78F0588

Cautions 1. The 78K0/Kx2-L microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product as follows.

<R> **(1) Port functions**

Port	78K0/KY2-L	78K0/KA2-L			78K0/KB2-L	78K0/KC2-L		
	16 Pins	20 Pins	25 Pins	32 Pins	30 Pins	40 Pins	44 Pins	48 Pins
Port 0	P00, P01		P00, P02	P01, P02	P00, P01			P00 to P02
Port 1	–				P10 to P17			
Port 2	P20 to P23	P20 to P25	P20 to P26	P20 to P27	P20 to P23	P20 to P26	P20 to P27	
Port 3	P30	P30 to P32	P31 to P37		P30 to P33			
Port 4	–						P40, P41	P40 to P42
Port 6	P60, P61					P60 to P62	P60 to P63	
Port 7	–			P70 to P73	–	P70 to P73		P70 to P75
Port 12	P121, P122, P125				P120 to P122, P125	P120 to P125		

(The remaining table is on the next page.)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(2) PGA

(T_A = –40 to +85°C, 2.7 V ≤ AV_{REF} ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}					±5	±10	mV
Input voltage range	V_{IPGA}				0.1AV_{REF}/gain		0.9AV_{REF}/gain	V
Maximum output voltage	V_{OPGA}				0.1AV_{REF}		0.9AV_{REF}	V
Gain error		4, 8 times					±1	%
		16 times					±1.5	%
		32 times					±2	%
Slew rate	SR_{RPGA}	Rising edge	4.0 V ≤ AV_{REF} ≤ 5.5 V	4, 8 times	4			V/μs
				16, 32 times	1.5			V/μs
			2.7 V ≤ AV_{REF} < 4.0 V	4, 8 times	1.8			V/μs
				16, 32 times	0.5			V/μs
	SR_{FPGA}	Falling edge	4.0 V ≤ AV_{REF} ≤ 5.5 V	4, 8 times	3.2			V/μs
				16, 32 times	1.5			V/μs
			2.7 V ≤ AV_{REF} < 4.0 V	4, 8 times	1.2			V/μs
				16, 32 times	0.5			V/μs
Operation stabilization wait time[Note]	t_{PGA}	4, 8 times					5	μs
		16, 32 times					10	μs

Note Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

(3) Operational amplifier 0

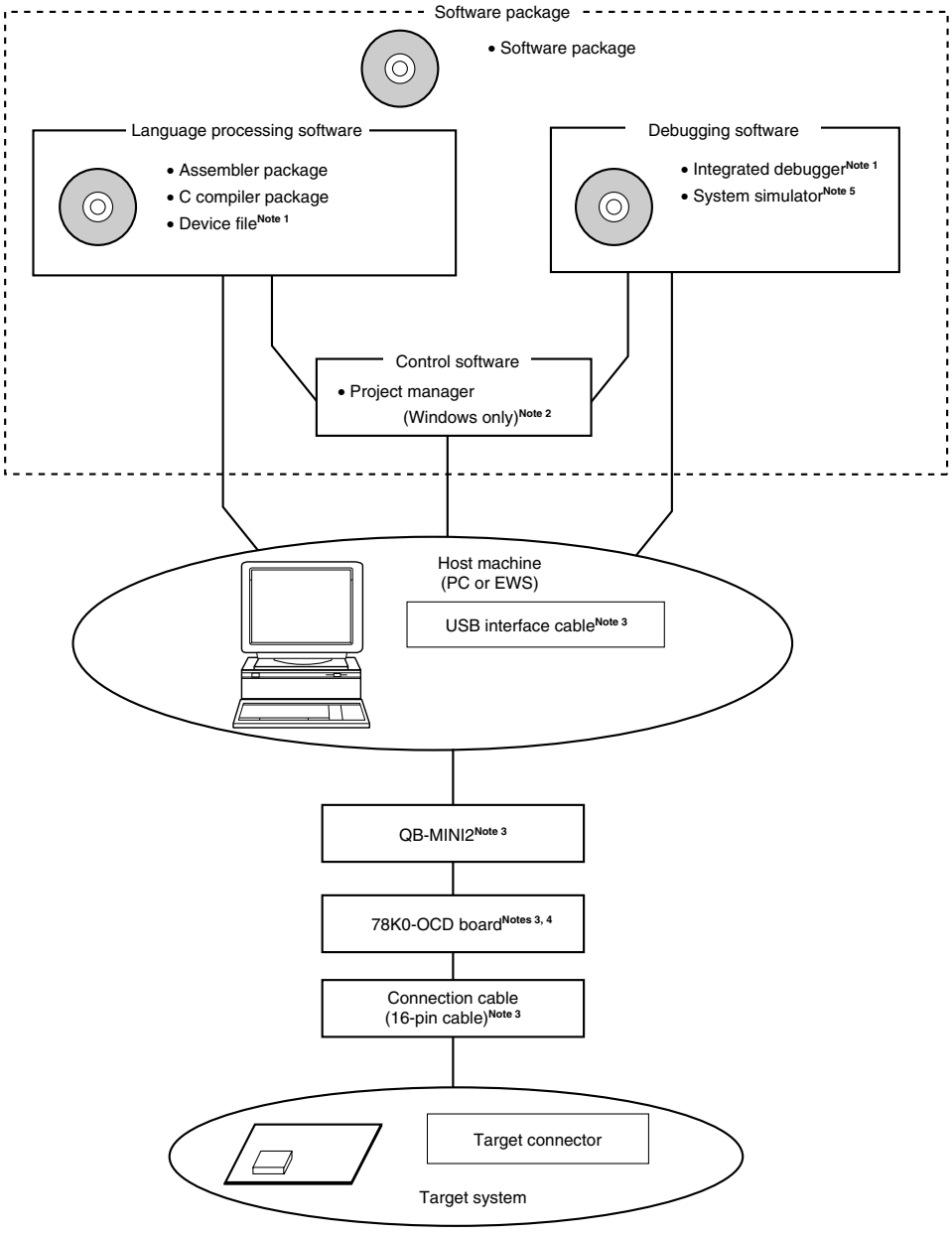
(T_A = –40 to +85°C, 2.2 V ≤ V_{DD} ≤ 5.5 V, 2.2 V ≤ AV_{REF} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V,
Output load: R_L = 47 kΩ, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOP0}	V_{BIAS} = 1/2 V_{DD}, AV_{REF} = 3.0 V			±10	mV
Power supply voltage rejection ratio	$PSRR_{OP0}$	AV_{REF} = 3.0 V		70		dB
Output voltage, high	V_{OHOP0}	AV_{REF} = 3.0 V/2.2 V, I_{OH} = –500 μA	AV_{REF}–0.2			V
Output voltage, low	V_{OLOP0}	AV_{REF} = 3.0 V/2.2 V, I_{OL} = 500 μA			0.1	V
Common-mode input voltage	V_{ICMOP0}	AV_{REF} = 3.0 V/2.2 V	0		AV_{REF}–0.6	V
Slew rate	SR_{OP0}	AV_{REF} = 3.0 V		1.8		V/μs
		AV_{REF} = 5.0 V		2.0		V/μs
Input noise spectral density (Inoise)		AV_{REF} = 3.0 V, V_{IN} = 0.1 V, f = 1 kHz		73		nV/√Hz
		AV_{REF} = 3.0 V, V_{IN} = AV_{REF}/2 V, f = 1 kHz		60		
		AV_{REF} = 3.0 V, V_{IN} = AV_{REF} –0.6 V, f = 1 kHz		55		
Phase margin		AV_{REF} = 3.0 V		40		deg
Large-amplitude voltage gain	AV_{OP0}	AV_{REF} = 3.0 V		100		dB
Gain-bandwidth product	GBW_{OP0}	AV_{REF} = 5.0 V/3.0 V/2.2 V		3.0		MHz
Operation stabilization wait time[Note]	t_{OP0}	AV_{REF} = 3.0 V		10		μs

Note Time required until a state is entered where the DC and AC specifications of the operational amplifier 0 are satisfied after the operational amplifier 0 operation has been enabled (OPAMP0E = 1).

Figure A-1. Development Tool Configuration (2/2)

(2) When using the on-chip debug emulator with programming function QB-MINI2



Notes 1. Download the device file for 78K0/Kx2-L microcontrollers (DF780588) and the integrated debugger ID78K0-QB from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html). <R>

2. The project manager PM+ is included in the assembler package.
The PM+ is only used for Windows.

3. On-chip debug emulator QB-MINI2 is supplied with USB interface cable, connection cables (10-pin cable and 16-pin cable), and 78K0-OCD board. In addition, download the software for operating the QB-MINI2 from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html). <R>

4. This is used only when using QB-MINI2 as an on-chip debug emulator.

5. This is an instruction simulation version included in the software package.

A.1 Software Package

SP78K0 78K0 microcontroller software package	Development tools (software) common to the 78K0 microcontrollers are combined in this package.

A.2 Language Processing Software

RA78K0[Note 1] Assembler package	This assembler converts programs written in mnemonics into object codes executable with a microcontroller. This assembler is also provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with a device file (DF780588). **<Precaution when using RA78K0 in PC environment>** This assembler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.
CC78K0[Note 1] C compiler package	This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an assembler package and device file. **<Precaution when using CC78K0 in PC environment>** This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.
DF780588[Note 2] Device file	This file contains information peculiar to the device. This device file should be used in combination with a tool (RA78K0, CC78K0, ID78K0-QB, and SM+ for 78K0). The corresponding OS and host machine differ depending on the tool to be used.

Notes 1. If the versions of RA78K0 and CC78K0 are Ver.4.00 or later, different versions of RA78K0 and CC78K0 can be installed on the same machine.

2. The DF780588 can be used in common with the RA78K0, CC78K0, ID78K0-QB, and SM+ for 78K0. Download the DF780588 from the download site for development tools <R> (http://www2.renesas.com/micro/en/ods/index.html).