Renesas Electronics America Inc - UPD78F0565MC-CAA-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0565mc-caa-ax

Table 3-7. Special Function Register List: 78K0/KA2-L (20-pin products) (1/4)

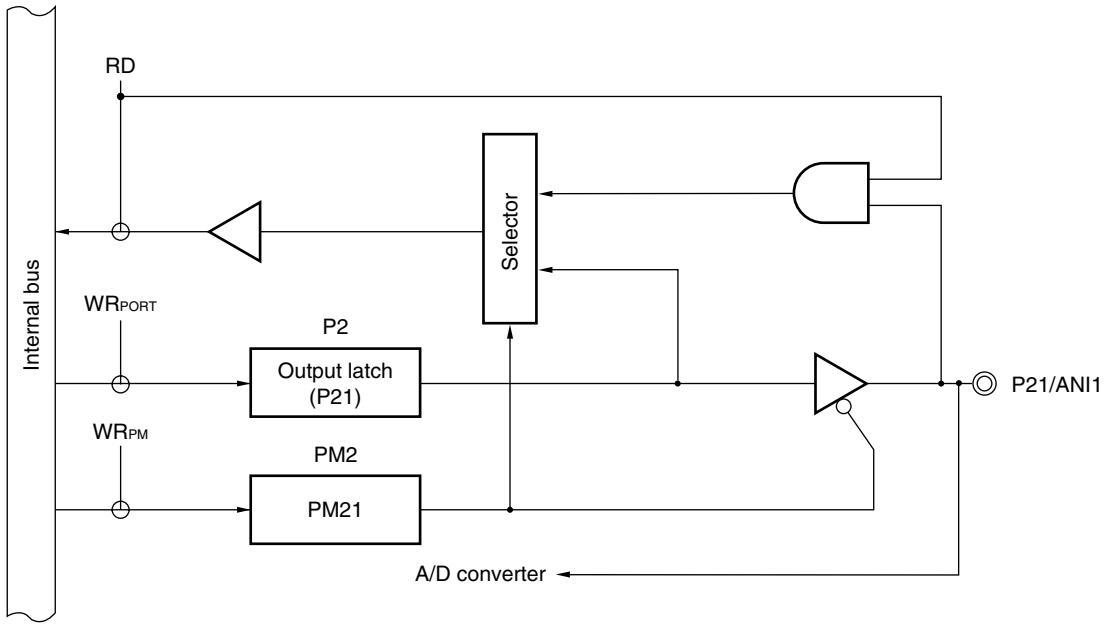
Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF00H	P0	0	0	0	0	0	0	P01	P00	R/W	√	√	–	00H	172
FF01H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF02H	P2	0	0	P25	P24	P23	P22	P21	P20	R/W	√	√	–	00H	172
FF03H	P3	0	0	0	0	0	P32	P31	P30	R/W	√	√	–	00H	172
FF04H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF05H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF06H	P6	0	0	0	0	0	0	P61	P60	R/W	√	√	–	00H	172
FF07H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF08H	AD ADCRL	–	–	–	–	–	–	–	–	R	–	√	–	00H	411
FF09H	CR	0	0	0	0	0	0	–	–	R	–	–	√	0000H	410
FF0AH	RXB6	–	–	–	–	–	–	–	–	R	–	√	–	FFH	452
FF0BH	TXB6	–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	453
FF0CH	P12	0	0	P125	0	0	P122	P121	0	R	√	√	–	00H	172
FF0DH	ADCRH	–	–	–	–	–	–	–	–	R	–	√	–	00H	411
FF0EH	ADS	0	<ADOAS> Note	0	0	0	<ADS2>	<ADS1>	<ADS0>	R/W	√	√	–	00H	412, 439
FF0FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF10H	TM00	–	–	–	–	–	–	–	–	R	–	–	√	0000H	243
FF11H		–	–	–	–	–	–	–	–						
FF12H	CR000	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	244
FF13H		–	–	–	–	–	–	–	–						
FF14H	CR010	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	244
FF15H		–	–	–	–	–	–	–	–						
FF16H to FF19H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF1AH	CMP01	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	338
FF1BH	CMP11	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	338
FF1CH to FF1EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF1FH	TM51	–	–	–	–	–	–	–	–	R	–	√	–	00H	317
FF20H	PM0	1	1	1	1	1	1	PM01	PM00	R/W	√	√	–	FFH	167, 256
FF21H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF22H	PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20	R/W	√	√	–	FFH	167, 415, 440
FF23H	PM3	1	1	1	1	1	PM32	PM31	PM30	R/W	√	√	–	FFH	167, 324, 345
FF24H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF25H	–	–	–	–	–	–	–	–	–		–	–	–	–	–

Note This bit is incorporated only in products with operational amplifier.

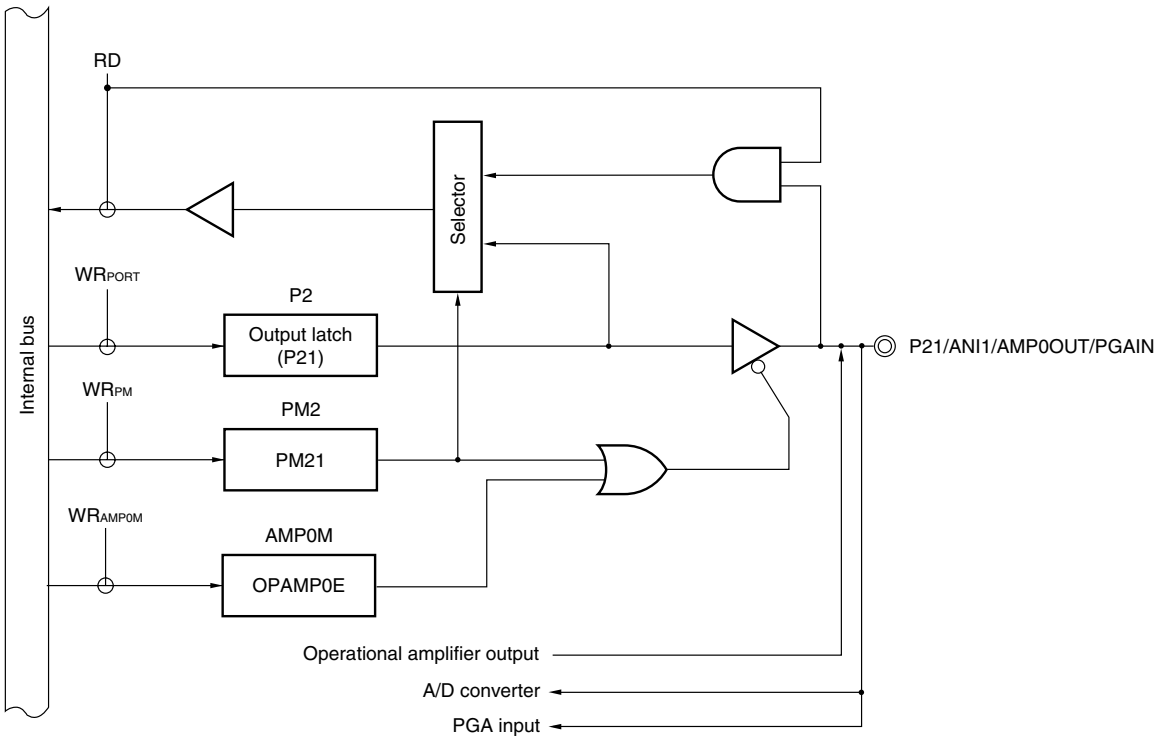
Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

Figure 4-12. Block Diagram of P21

(1) Products without operational amplifier



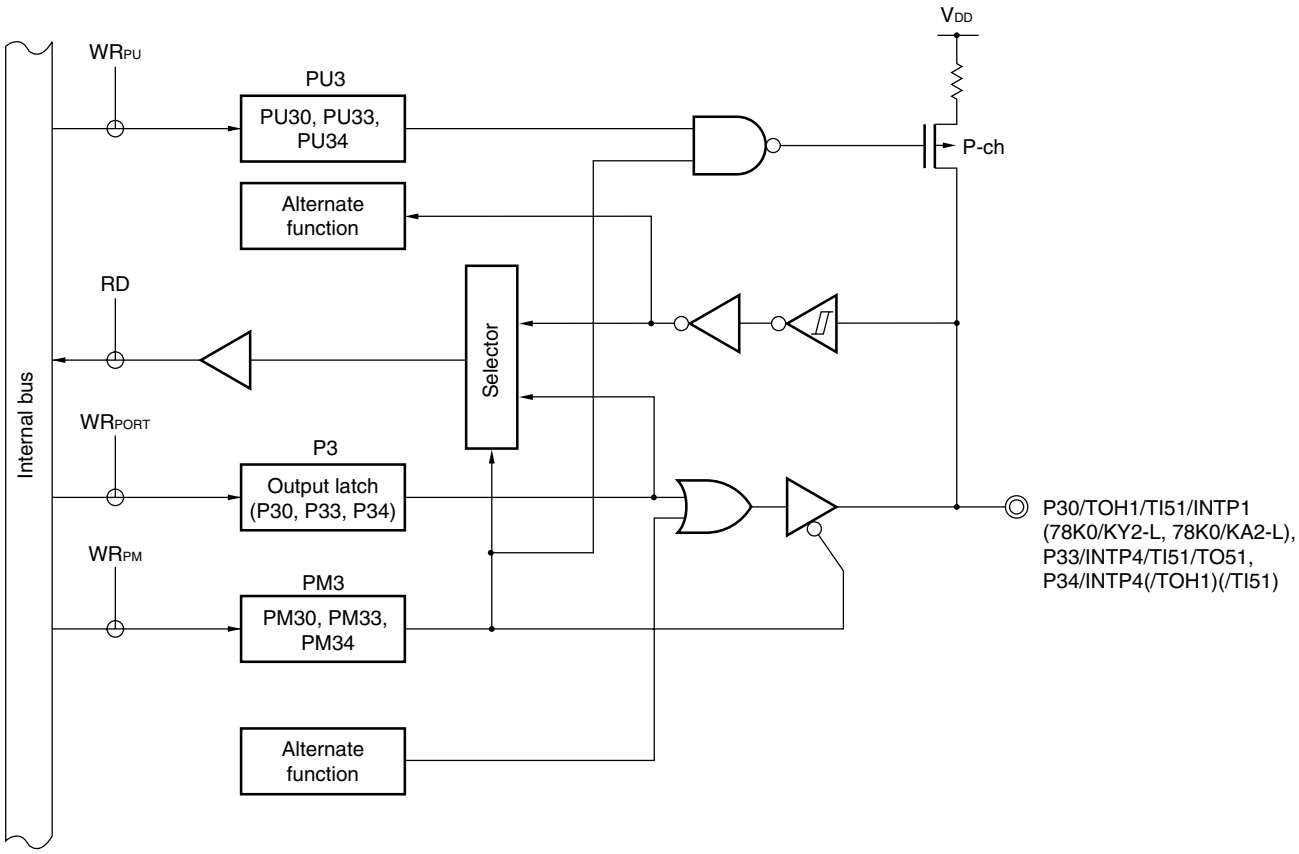
<R> **(2) Products with operational amplifier**



P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Remark PGA: Programmable Gain Amplifier

Figure 4-15. Block Diagram of P30 (78K0/KY2-L, 78K0/KA2-L), P33, P34



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

(5) Port output mode register 6 (POM6)

This register sets the output mode of P60 to P63 in 1-bit units.

During I^2C communication, set POM60 and POM61 to 1.

<R> In the 78K0/KY2-L and 78K0/KA2-L, clear POM60 to 0 when using the P60/TxD6/SCLA0 pin as the data output of serial interface UART6.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 4-46. Format of Port Output Mode Register 6 (POM6)

Address: FF2AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
POM6	0	0	0	0	POM63Note	POM62Note	POM61	POM60

POM6n	P6n pin output mode selection (n = 0 to 3)
0	Normal output (CMOS output) mode
1	N-ch open drain output (V_{DD} tolerance) mode

Note 78K0/KC2-L only

(6) Reset pin mode register (RSTMASK)

This register sets the pin function of $\overline{\text{RESET}}$/P125 (external reset input/input-dedicated port).

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 4-47. Format of Reset Pin Mode Register (RSTMASK)

Address: FF2DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
RSTMASK	0	0	RSTM	0	0	0	0	0

RSTM	$\overline{\text{RESET}}$/P125 pin function selection
0	Using as external reset input ($\overline{\text{RESET}}$)
1	Using as input-dedicated port (P125)

(3) Example of setting procedure when stopping the internal high-speed oscillation clock

The internal high-speed oscillation clock can be stopped in the following two ways.

- Executing the STOP instruction to set the STOP mode
- Setting RSTOP to 1 and stopping the internal high-speed oscillation clock

(a) To execute a STOP instruction

<1> Setting of peripheral hardware

Stop peripheral hardware that cannot be used in the STOP mode (for peripheral hardware that cannot be used in STOP mode, refer to **CHAPTER 19 STANDBY FUNCTION**).

<2> Setting the X1 clock oscillation stabilization time after standby release

When the CPU is operating on the X1 clock, set the value of the OSTS register before the STOP instruction is executed. To operate the CPU immediately after the STOP mode has been released, set MCM0 to 0, switch the CPU clock to the internal high-speed oscillation clock, and check that RSTS is 1.

<3> Executing the STOP instruction

When the STOP instruction is executed, the system is placed in the STOP mode and internal high-speed oscillation clock is stopped.

(b) To stop internal high-speed oscillation clock by setting RSTOP to 1

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the internal high-speed oscillation clock.

When CLS = 0 and MCS = 0, the internal high-speed oscillation clock is supplied to the CPU, so change the CPU clock to a clock other than the internal high-speed oscillation clock.

- 78K0/KY2-L, 78K0/KA2-L, and 78K0/KB2-L

MCS	CPU Clock Status
0	Internal high-speed oscillation clock
1	High-speed system clock

- 78K0/KC2-L

CLS	MCS	CPU Clock Status
0	0	Internal high-speed oscillation clock
0	1	High-speed system clock
1	×	Subsystem clock

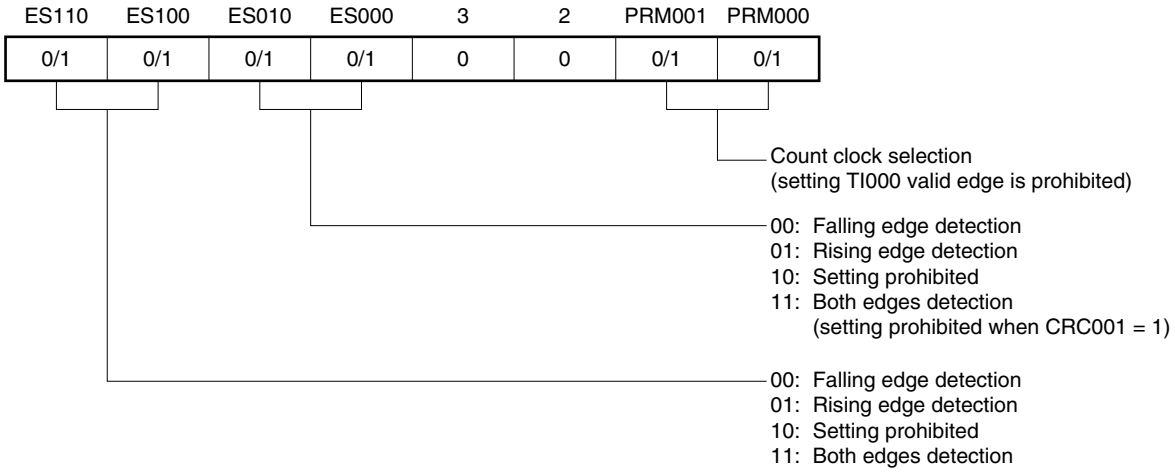
<2> Stopping the internal high-speed oscillation clock (RCM register)

When RSTOP is set to 1, internal high-speed oscillation clock is stopped.

Caution Be sure to confirm that MCS = 1 or CLS = 1 when setting RSTOP to 1. In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock.

Figure 6-39. Example of Register Settings in Free-Running Timer Mode (2/2)

(d) Prescaler mode register 00 (PRM00)



(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM000) is generated. The count value of TM00 is not cleared.

To use this register as a capture register, select either the TI000 or TI010 pin input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR000.

(g) 16-bit capture/compare register 010 (CR010)

When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM010) is generated. The count value of TM00 is not cleared.

When this register is used as a capture register, the TI000 pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR010.

Figure 6-52. Example of Register Settings for Pulse Width Measurement (1/2)

(a) 16-bit timer mode control register 00 (TMC00)

				TMC003	TMC002	TMC001	OVF00
0	0	0	0	0/1	0/1	0	0

01: Free running timer mode
10: Clear and start mode entered by valid edge of TI000 pin.

(b) Capture/compare control register 00 (CRC00)

					CRC002	CRC001	CRC000
0	0	0	0	0	1	0/1	1

1: CR000 used as capture register

0: TI010 pin is used as capture trigger of CR000.
1: Reverse phase of TI000 pin is used as capture trigger of CR000.

1: CR010 used as capture register

(c) 16-bit timer output control register 00 (TOC00)

	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00
0	0	0	0	0	0	0	0

(d) Prescaler mode register 00 (PRM00)

ES110	ES100	ES010	ES000	3	2	PRM001	PRM000
0/1	0/1	0/1	0/1	0	0	0/1	0/1

Selects count clock
(setting valid edge of TI000 is prohibited)

00: Falling edge detection
01: Rising edge detection
10: Setting prohibited
11: Both edges detection
(setting when CRC001 = 1 is prohibited)

00: Falling edge detection
01: Rising edge detection
10: Setting prohibited
11: Both edges detection

Figure 7-9. Format of 8-Bit Timer Mode Control Register 50 (TMC50) (78K0/KB2-L, 78K0/KC2-L Only)

Address: FF6BH After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC50	TCE50	TMC506	0	0	LVS50	LVR50	TMC501	TOE50

TCE50	TM50 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC506	TM50 operating mode selection
0	Mode in which clear & start occurs on a match between TM50 and CR50
1	PWM (free-running) mode

LVS50	LVR50	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO50 output: low level)
1	0	Timer output F/F set (1) (default value of TO50 output: high level)
1	1	Setting prohibited

TMC501	In other modes (TMC506 = 0)	In PWM mode (TMC506 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

TOE50	Timer output control
0	Output disabled (TO50 output is low level)
1	Output enabled

Note Bits 2 and 3 are write-only.

Cautions 1. The settings of LVS50 and LVR50 are valid in other than PWM mode.

2. Perform <1> to <4> below in the following order, not at the same time.

<1> Set TMC501, TMC506: Operation mode setting

<2> Set TOE50 to enable output: Timer output enable

<3> Set LVS50, LVR50 (refer to Caution 1): Timer F/F setting

<4> Set TCE50

3. When TCE50 = 1, setting the other bits of TMC50 is prohibited.

4. The actual TO50/TI50/P17 pin output is determined depending on PM17 and P17 besides TO50 output.

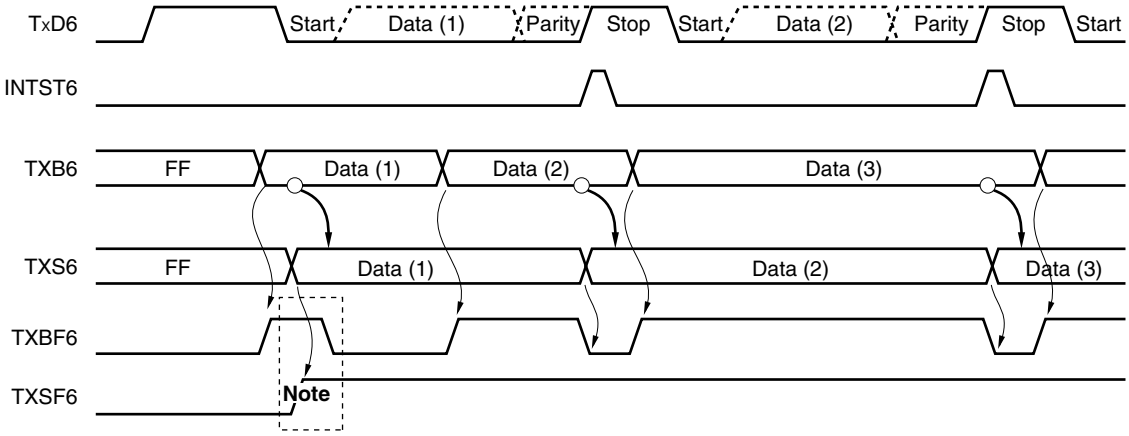
Remarks 1. In PWM mode, PWM output is made inactive by clearing TCE50 to 0.

2. If LVS50 and LVR50 are read, the value is 0.

3. The values of the TMC506, LVS50, LVR50, TMC501, and TOE50 bits are reflected at the TO50 output regardless of the value of TCE50.

Figure 14-19 shows the timing of starting continuous transmission, and Figure 14-20 shows the timing of ending continuous transmission.

Figure 14-19. Timing of Starting Continuous Transmission



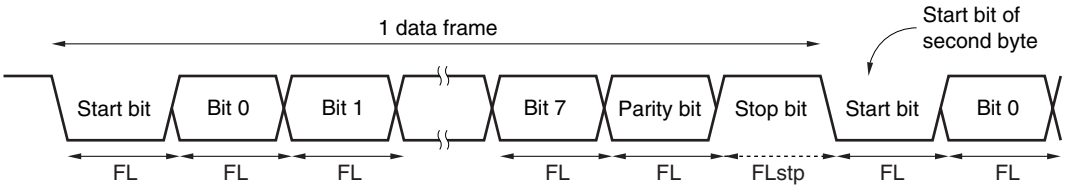
Note When ASIF6 is read, there is a period in which TXBF6 and TXSF6 = 1, 1. Therefore, judge whether writing is enabled using only the TXBF6 bit.

Remark TxD6: TxD6 pin (output)
INTST6: Interrupt request signal
TXB6: Transmit buffer register 6
TXS6: Transmit shift register 6
ASIF6: Asynchronous serial interface transmission status register 6
TXBF6: Bit 1 of ASIF6
TXSF6: Bit 0 of ASIF6

(5) Data frame length during continuous transmission

When data is continuously transmitted, the data frame length from a stop bit to the next start bit is extended by two clocks of base clock from the normal value. However, the result of communication is not affected because the timing is initialized on the reception side when the start bit is detected.

Figure 14-28. Data Frame Length During Continuous Transmission



Where the 1-bit data length is FL, the stop bit length is FLstp, and base clock frequency is f_{XCLK6}, the following expression is satisfied.

$$FLstp = FL + 2/f_{XCLK6}$$

Therefore, the data frame length during continuous transmission is:

$$\text{Data frame length} = 11 \times FL + 2/f_{XCLK6}$$

Figure 15-5. Format of IICA Control Register 0 (IICACTL0) (1/4)

Address: FFA7H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICACTL0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

IICE0	I^2C operation enable
0	Stop operation. Reset the IICA status register 0 (IICAS0)[Note 1]. Stop internal operation.
1	Enable operation.
Be sure to set this bit (1) while the SCLA0 and SDLA0 lines are at high level.	
Condition for clearing (IICE0 = 0)	Condition for setting (IICE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

LREL0[Notes 2,3]	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCLA0 and SDAA0 lines are set to high impedance. The following flags of IICA control register 0 (IICACTL0) and IICA status register 0 (IICAS0) are cleared to 0. • STT0 • SPT0 • MSTS0 • EXC0 • COI0 • TRC0 • ACKD0 • STD0
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL0 = 0)	Condition for setting (LREL0 = 1)
• Automatically cleared after execution • Reset	• Set by instruction

WREL0[Notes 2,3]	Wait cancellation
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared after wait is canceled.
When WREL0 is set (wait canceled) during the wait period at the ninth clock pulse in the transmission status (TRC0 = 1), the SDAA0 line goes into the high impedance state (TRC0 = 0).	
Condition for clearing (WREL0 = 0)	Condition for setting (WREL0 = 1)
• Automatically cleared after execution • Reset	• Set by instruction

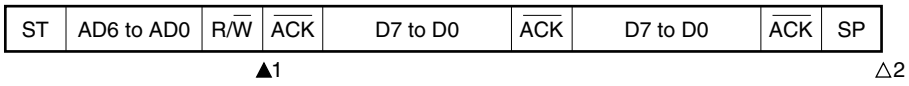
Notes 1. The IICAS0 register, the STCF and IICBSY bits of the IICAF0 register, and the CLD0 and DAD0 bits of the IICACTL1 register are reset.

2. The signals of these bits are invalid while the IICE0 bit is 0.

3. When the LREL0 and WREL0 bits are read, 0 is always read.

Caution If the operation of I^2C is enabled (IICE0 = 1) when the SCLA0 line is high level, the SDAA0 line is low level, and the digital filter is turned on (DFC0 of the IICACTL1 register = 1), a start condition will be inadvertently detected immediately. In this case, set (1) the LREL0 bit by using a 1-bit memory manipulation instruction immediately after enabling operation of I^2C (IICE0 = 1).

(b) When arbitration loss occurs during transmission of extension code

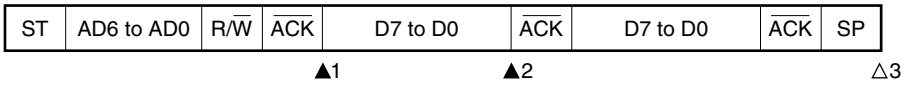


▲1: IICAS0 = 0110×010B
Sets LREL0 = 1 by software
△2: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(c) When arbitration loss occurs during transmission of data

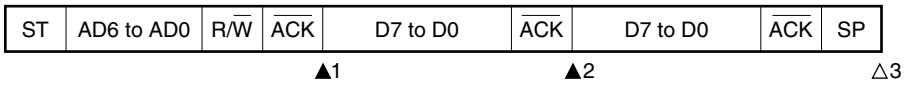
(i) When WTIM0 = 0



▲1: IICAS0 = 10001110B
▲2: IICAS0 = 01000000B
△3: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1

(ii) When WTIM0 = 1

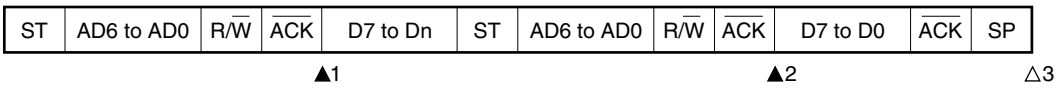


▲1: IICAS0 = 10001110B
▲2: IICAS0 = 01000100B
△3: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1

(d) When loss occurs due to restart condition during data transfer

(i) Not extension code (Example: unmatches with SVA0)

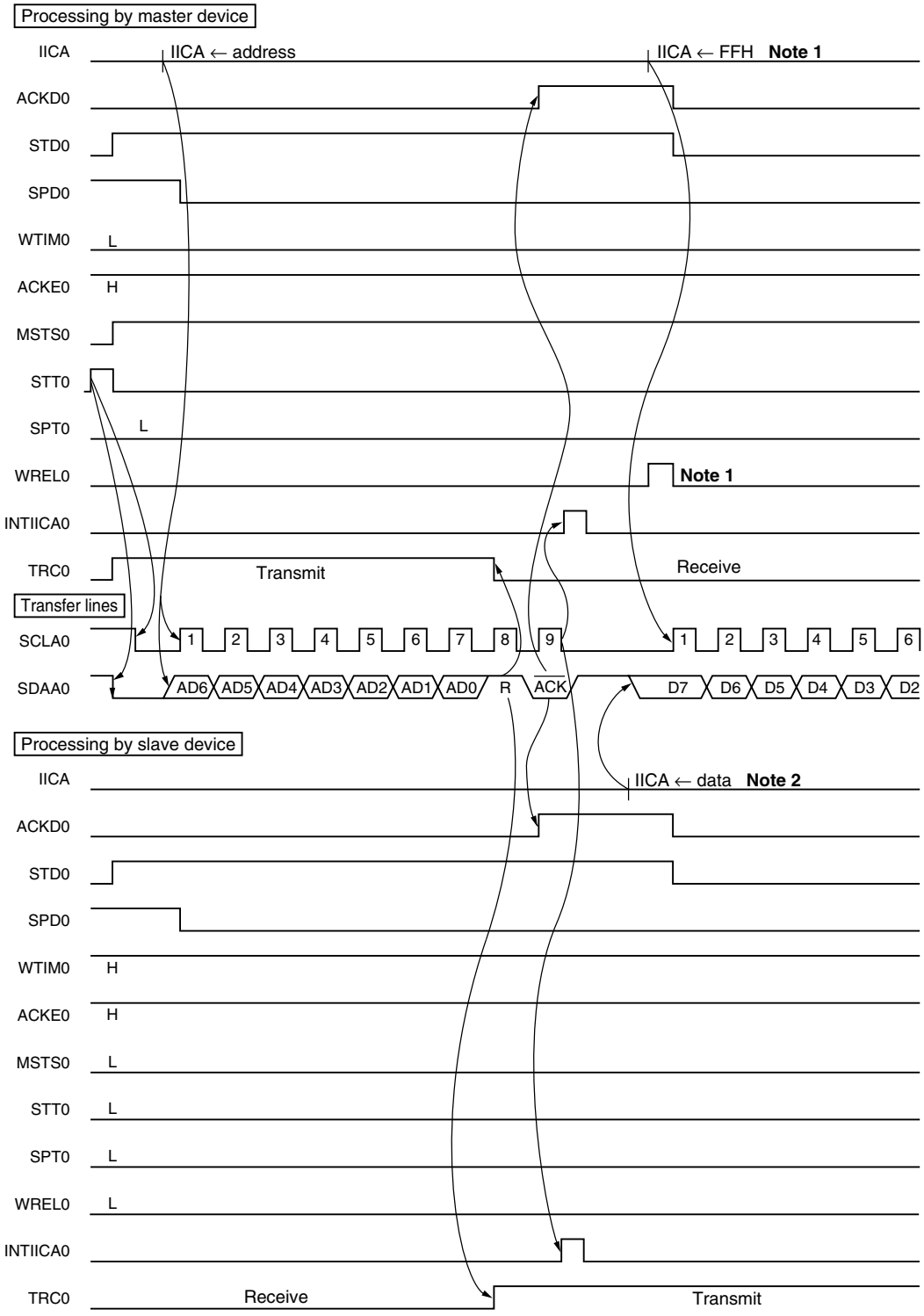


▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 01000110B
△3: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care
n = 6 to 0

Figure 15-34. Example of Slave to Master Communication
(When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)

(1) Start condition ~ address



Notes 1. To cancel master wait, write “FFH” to IICA or set WREL0.

2. Write data to IICA, not setting WREL0, in order to cancel a wait state during slave transmission.

PM0, PM1, PM3, PM4, PM6, and PM12 can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation sets these registers to FFH.

<R> **Figure 16-9. Format of Port Mode Register 0 (PM0)**

Address: FF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	1	1	1	1	PM02	PM01 Note 1	PM00 Note 2

PM0n	P1n pin I/O mode selection (n = 0 to 2)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Notes 1. 32-pin products only
2. 25-pin products only

Remark The figure shown above presents the format of port mode register 1 of the 78K0/KB2-L and 78K0/KA2-L (25, 32-pin products).

Figure 16-10. Format of Port Mode Register 1 (PM1)

Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

PM1n	P1n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 1 of the 78K0/KB2-L and 78K0/KC2-L.

<R> **Figure 16-11. Format of Port Mode Register 3 (PM3)**

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 1 of the 78K0/KB2-L and 78K0/KA2-L (25, 32-pin products).

<R> **Figure 17-6. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (40-pin products of 78K0/KC2-L)**

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	CSIIF10	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	7	6	<5>	<4>	<3>	<2>	1	<0>
IF1L	0	0	RTCIF	KRIF	TMIF51	RTCIIF	0	ADIF

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
IF1H	0	0	0	PIF11	PIF10	PIF9	CSIIF11	IICAIF0

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Caution Be sure to clear bits 1, 6, and 7 of IF1L, and bits 5 to 7 of IF1H to 0.

27.2 Operation List

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	**MOV**	r, #byte	2	4	–	r ← byte	
		saddr, #byte	3	6	7	(saddr) ← byte	
		sfr, #byte	3	–	7	sfr ← byte	
		A, r Note 3	1	2	–	A ← r	
		r, A Note 3	1	2	–	r ← A	
		A, saddr	2	4	5	A ← (saddr)	
		saddr, A	2	4	5	(saddr) ← A	
		A, sfr	2	–	5	A ← sfr	
		sfr, A	2	–	5	sfr ← A	
		A, !addr16	3	8	9	A ← (addr16)	
		!addr16, A	3	8	9	(addr16) ← A	
		PSW, #byte	3	–	7	PSW ← byte	× × ×
		A, PSW	2	–	5	A ← PSW	
		PSW, A	2	–	5	PSW ← A	× × ×
		A, [DE]	1	4	5	A ← (DE)	
		[DE], A	1	4	5	(DE) ← A	
		A, [HL]	1	4	5	A ← (HL)	
		[HL], A	1	4	5	(HL) ← A	
		A, [HL + byte]	2	8	9	A ← (HL + byte)	
		[HL + byte], A	2	8	9	(HL + byte) ← A	
		A, [HL + B]	1	6	7	A ← (HL + B)	
		[HL + B], A	1	6	7	(HL + B) ← A	
		A, [HL + C]	1	6	7	A ← (HL + C)	
		[HL + C], A	1	6	7	(HL + C) ← A	
	XCH	A, r Note 3	1	2	–	A ↔ r	
		A, saddr	2	4	6	A ↔ (saddr)	
		A, sfr	2	–	6	A ↔ (sfr)	
		A, !addr16	3	8	10	A ↔ (addr16)	
		A, [DE]	1	4	6	A ↔ (DE)	
		A, [HL]	1	4	6	A ↔ (HL)	
		A, [HL + byte]	2	8	10	A ↔ (HL + byte)	
		A, [HL + B]	2	8	10	A ↔ (HL + B)	
		A, [HL + C]	2	8	10	A ↔ (HL + C)	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

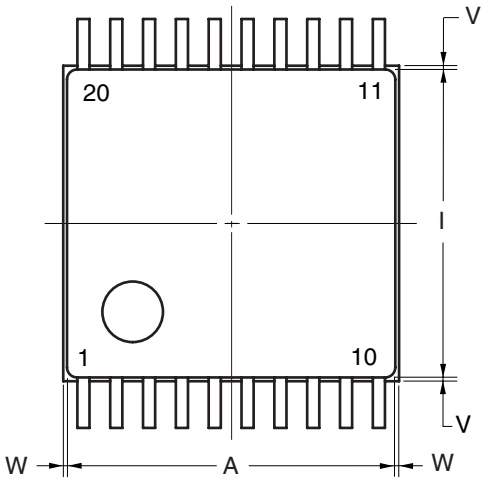
Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

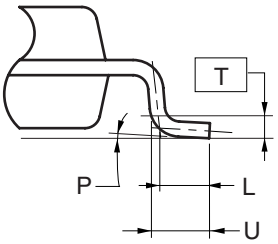
29.2 78K0/KA2-L

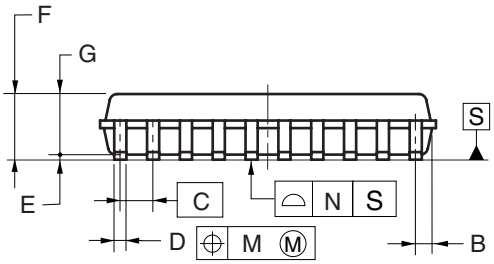
- μPD78F0560MC-CAA-AX, 78F0561MC-CAA-AX, 78F0562MC-CAA-AX, 78F0565MC-CAA-AX, 78F0566MC-CAA-AX, 78F0567MC-CAA-AX

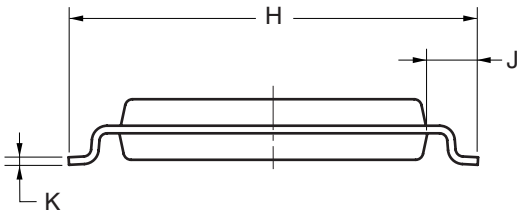
20-PIN PLASTIC SSOP (7.62 mm (300))



detail of lead end







(UNIT:mm)

ITEM	DIMENSIONS
A	6.50±0.10
B	0.325
C	0.65 (T.P.)
D	$0.22^{+0.10}_{-0.05}$
E	0.10±0.05
F	1.30±0.10
G	1.20
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.05}_{-0.01}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

P20MC-65-CAA

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

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Page	Description	Classification
CHAPTER 12 A/D CONVERTER		
p.421	Change of **Table 12-8. Setting Functions of P70/ANI8 to P72/ANI10 Pins**	(d)
p.433	Change of mode name in **Table 12-9. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)**	(c)
CHAPTER 13 OPERATIONAL AMPLIFIERS		
p.435	Change of **Figure 13-1. Block Diagram of Operational Amplifier**	(c)
p.439	Change of **Figure 13-6. Format of Analog Input Channel Specification Register (ADS)**	(c)
p.444	Change of **Table 13-5. Setting Functions of P21/ANI1/AMP0OUT/PGAIN Pin**	(c)
CHAPTER 16 SERIAL INTERFACES CSI10 AND CSI11		
p.573	Change of **(4) Port mode registers 0, 1, 3, 4, 6, 12 (PM0, PM1, PM3, PM4, PM6, PM12)** in **16.3 Registers Controlling Serial Interfaces CSI10 and CSI11**	(d)
p.574	Addition of **Figure 16-9. Format of Port Mode Register 0 (PM0)**	(d)
p.574	Addition of **Figure 16-11. Format of Port Mode Register 3 (PM3)**	(d)
CHAPTER 17 INTERRUPT FUNCTIONS		
pp.592, 593	Change of **Table 17-1. Interrupt Source List**	(d)
CHAPTER 19 STANDBY FUNCTION		
p.649	Addition of **Caution** in **Table 19-3. Operating Statuses in STOP Mode**	(c)
CHAPTER 20 RESET FUNCTION		
pp.662, 663	Change of **Note** in **Table 20-2. Hardware Statuses After Reset Acknowledgment**	(b)
p.664	Change of **Table 20-3. RESF Status When Reset Request Is Generated**	(b)
CHAPTER 21 POWER-ON-CLEAR CIRCUIT		
p.668	Change of **Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2/2)**	(b)
CHAPTER 22 LOW-VOLTAGE DETECTOR		
p.673	Change of **Note 1** in **Figure 22-2. Format of Low-Voltage Detection Register (LVIM)**	(b)
p.675	Change of **Note** in **Figure 22-3. Format of Low-Voltage Detection Level Select Register (LVIS)**	(b)
p.676	Change of **Remark 1** in **22.4 (1) Used as reset (LVIMD = 1)**	(b)
p.680	Change of description in **22.4.1 (1) (b) When LVI default start function enabled is set (LVISTART = 1)**	(b)
p.680	Change of **Figure 22-6. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVISTART = 1)**	(b)
p.685	Change of description in **22.4.2 (1) (b) When LVI default start function enabled is set (LVISTART = 1)**	(b)
p.685	Change of **Figure 22-9. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 0, Option Byte: LVISTART = 1)**	(b)
CHAPTER 23 REGULATOR		
p.691	Change of **(1) Regulator mode control register (RMC)** in **23.2 Register Controlling Regulator**	(b)
CHAPTER 24 OPTION BYTE		
p.694	Change of **(4) 0083H/1083H** in **24.1 Functions of Option Bytes**	(b)
p.696	Change of description of LVISTART bit in **Figure 24-1. Format of Option Byte (2/3)**	(b)
p.697	Change of **Figure 24-1. Format of Option Byte (3/3)**	(b)
p.698	Change of description example of software in **24.2 Format of Option Byte**	(b)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

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Edition	Description	Chapter
2nd Edition	Modification of **Table 12-3 Setting Functions of P10/ANI8/AMP1-, P12/ANI10/AMP1+ Pins**	**CHAPTER 12 A/D CONVERTER**
	Modification of **Table 12-5 Setting Functions of P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins**	
	Deletion of **Caution 2** in **12.4.1 Basic operations of A/D converter**	
	Modification of description of setting methods and deletion of **Caution 2** in **12.4.3 (1) A/D conversion operation**	
	Modification of **Figure 13-1 Block Diagram of Operational Amplifier**	**CHAPTER 13 OPERATIONAL AMPLIFIERS**
	Addition of **Remark** to **Figure 13-2 Format of Operational Amplifier 0 Control Register (AMP0M) (Products with Operational Amplifier Only)**	
	Modification of **Figure 13-4 Format of A/D Port Configuration Register 0 (ADPC0)**	
	Modification of **Figure 13-5 Format of A/D Port Configuration Register 1 (ADPC1) (78K0/KB2-L and 78K0/KC2-L Only)**	
	Modification of **Table 13-2 Setting Functions of P10/ANI8/AMP1-, P12/ANI10/AMP1+ Pins**	
	Modification of **Table 13-4 Setting Functions of P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins**	
	Modification of **Remark** in **Figure 14-4 Block Diagram of Serial Interface UART6**	**CHAPTER 14 SERIAL INTERFACE UART6**
	Addition of **Note 3** to **Figure 14-8 Format of Clock Selection Register 6 (CKSR6)**	
	Modification of description in **14.3 (8) Port mode register 1 (PM1), port mode register 6 (PM6)**	
	Modification of **(1) 78K0/KY2-L and 78K0/KA2-L** in **Table 14-2 Relationship Between Register Settings and Pins**	
	Addition of **15.4.2 Setting transfer clock by using IICWL and IICWH registers**	**CHAPTER 15 SERIAL INTERFACE IICA**
	Modification of the mounted situation in the 78K0/KB2-L and 78K0/KC2-L	**CHAPTER 16 SERIAL INTERFACES CSI10 AND CSI11**
	Modification of description in **16.3 (4) Port mode registers 1, 4, 6, 12 (PM1, PM4, PM6, PM12)**	
	Modification of and addition of **Notes 3** and **4** to **Table 16-3 SO1n Output Status**	
	Modification of maskable interrupts (internal) in the 78K0/KB2-L and 78K0/KC2-L	**CHAPTER 17 INTERRUPT FUNCTIONS**
	Modification of **Table 17-1 Interrupt Source List (1/2)**	
	Modification of **Table 17-2 Flags Corresponding to Interrupt Request Sources (1/2)**	
	Modification of **Caution** in **Figure 17-4 Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (78K0/KB2-L)** to **Figure 17-6 Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (48-pin products of 78K0/KC2-L)**	
	Modification of **Caution** in **Figure 17-9 Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (78K0/KB2-L)** to **Figure 17-11 Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (48-pin products of 78K0/KC2-L)**	

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