Renesas Electronics America Inc - UPD78F0566MC-CAA-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0566mc-caa-ax

<R> **Table 3-10. Special Function Register List: 78K0/KC2-L (1/6)**

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF00H	P0	0	0	0	0	0	P02 Note1	P01	P00	R/W	√	√	–	00H	172
FF01H	P1	P17	P16	P15	P14	P13	P12	P11	P10	R/W	√	√	–	00H	172
FF02H	P2	P27 Note2	P26	P25	P24	P23	P22	P21	P20	R/W	√	√	–	00H	172
FF03H	P3	0	0	0	0	P33	P32	P31	P30	R/W	√	√	–	00H	172
FF04H	P4 Note2	0	0	0	0	0	P42 Note1	P41 Note2	P40 Note2	R/W	√	√	–	00H	172
FF05H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF06H	P6	0	0	0	0	P63 Note2	P62	P61	P60	R/W	√	√	–	00H	172
FF07H	P7	0	0	P75 Note1	P74 Note1	P73	P72	P71	P70	R/W	√	√	–	00H	172
FF08H	AD ADCRL	–	–	–	–	–	–	–	–	R	–	√	–	00H	411
FF09H	CR	0	0	0	0	0	0	–	–	R	–	–	√	0000H	410
FF0AH	RXB6	–	–	–	–	–	–	–	–	R	–	√	–	FFH	452
FF0BH	TXB6	–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	453
FF0CH	P12	0	0	P125	P124	P123	P122	P121	P120	R Note3	√	√	–	00H	172
FF0DH	ADCRH	–	–	–	–	–	–	–	–	R	–	√	–	00H	411
FF0EH	ADS	0	<ADOAS> Note4	0	0	<ADS3>	<ADS2>	<ADS1>	<ADS0>	R/W	√	√	–	00H	412, 439
FF0FH	SIO10	–	–	–	–	–	–	–	–	R	–	√	–	00H	566
FF10H	TM00	–	–	–	–	–	–	–	–	R	–	–	√	0000H	243
FF11H		–	–	–	–	–	–	–	–						
FF12H	CR000	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	244
FF13H		–	–	–	–	–	–	–	–						
FF14H	CR010	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	244
FF15H		–	–	–	–	–	–	–	–						
FF16H	TM50	–	–	–	–	–	–	–	–	R	–	√	–	00H	317
FF17H	CR50	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	317
FF18H	CMP00	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	338
FF19H	CMP10	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	338
FF1AH	CMP01	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	338
FF1BH	CMP11	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	338
FF1CH to FF1EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF1FH	TM51	–	–	–	–	–	–	–	–	R	–	√	–	00H	317

Notes 1. 48-pin products only.

2. 44-pin and 48-pin products only.

3. Only P120 is R/W.

4. This bit is incorporated only in products with operational amplifier.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

Table 3-10. Special Function Register List: 78K0/KC2-L (4/6)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF6BH	TMC50	<TCE50>	TMC506	0	0	<LVS50>	<LVR50>	TMC501	<TOE50>	R/W	√	√	–	00H	320
FF6CH	TMHMD1	<TMHE1>	CKS12	CKS11	CKS10	TMMD11	TMMD10	<TOLEV1>	<TOEN1>	R/W	√	√	–	00H	339
FF6DH	TMCYC1	0	0	0	0	0	RMC1	NRZB1	<NRZ1>	R/W	√	√	–	00H	343
FF6EH	KRM	0	0	KRM5 Note1	KRM4 Note1	KRM3	KRM2	KRM1	KRM0	R/W	√	√	–	00H	638
FF6FH	RTCC2	<RINTE>	<RCLOE2>	<RCKDIV>	0	0	ICT2	ICT1	ICT0	R/W	√	√	–	00H	377
FF70H to FF79H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF7AH	SIO11	–	–	–	–	–	–	–	–	R	–	√	–	00H	566
FF7BH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF7CH	SOTB11	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	565
FF7DH to FF7FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF80H	CSIM10	<CSIE10>	TRMD10	0	DIR10	0	0	0	CSOT10	R/W	√	√	–	00H	566
FF81H	CSIC10	0	0	0	CKP10	DAP10	CKS102	CKS101	CKS100	R/W	√	√	–	00H	569
FF82H FF83H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF84H	SOTB10	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	565
FF85H to FF87H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF88H	CSIM11	<CSIE11>	TRMD11	SSE11 Note1	DIR11	0	0	0	CSOT11	R/W	√	√	–	00H	566
FF89H	CSIC11	0	0	0	CKP11	DAP11	CKS112	CKS111	CKS110	R/W	√	√	–	00H	569
FF8AH to FF8BH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF8CH	TCL51	0	0	0	0	0	TCL512	TCL511	TCL510	R/W	√	√	–	00H	318
FF8DH to FF98H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF99H	WDTE	–	–	–	–	–	–	–	–	R/W	–	√	–	1AH/9AH Note2	365
FF9AH	ALARMWM	0	WM40	WM20	WM10	WM8	WM4	WM2	WM1	R/W	–	√	–	00H	384
FF9BH	ALARMWH	0	0	WH20	WH10	WH8	WH4	WH2	WH1	R/W	–	√	–	12H	384
FF9CH	ALARMWW	0	WW6	WW5	WW4	WW3	WW2	WW1	WW0	R/W	–	√	–	00H	384

Notes 1. 48-pin products only.

2. The reset value of WDTE is determined by setting of option byte.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

(8) Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using OSTS after the STOP mode is released.

When the internal high-speed oscillation clock is selected as the CPU clock, confirm with OSTC that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using OSTC.

OSTS can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets OSTS to 05H.

Figure 5-11. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection	
				fx = 10 MHz
0	0	1	2^{11}/fx	204.8 μs
0	1	0	2^{13}/fx	819.2 μs
0	1	1	2^{14}/fx	1.64 ms
1	0	0	2^{15}/fx	3.27 ms
1	0	1	2^{16}/fx	6.55 ms
Other than above			Setting prohibited	

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

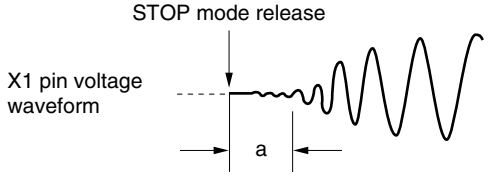
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).

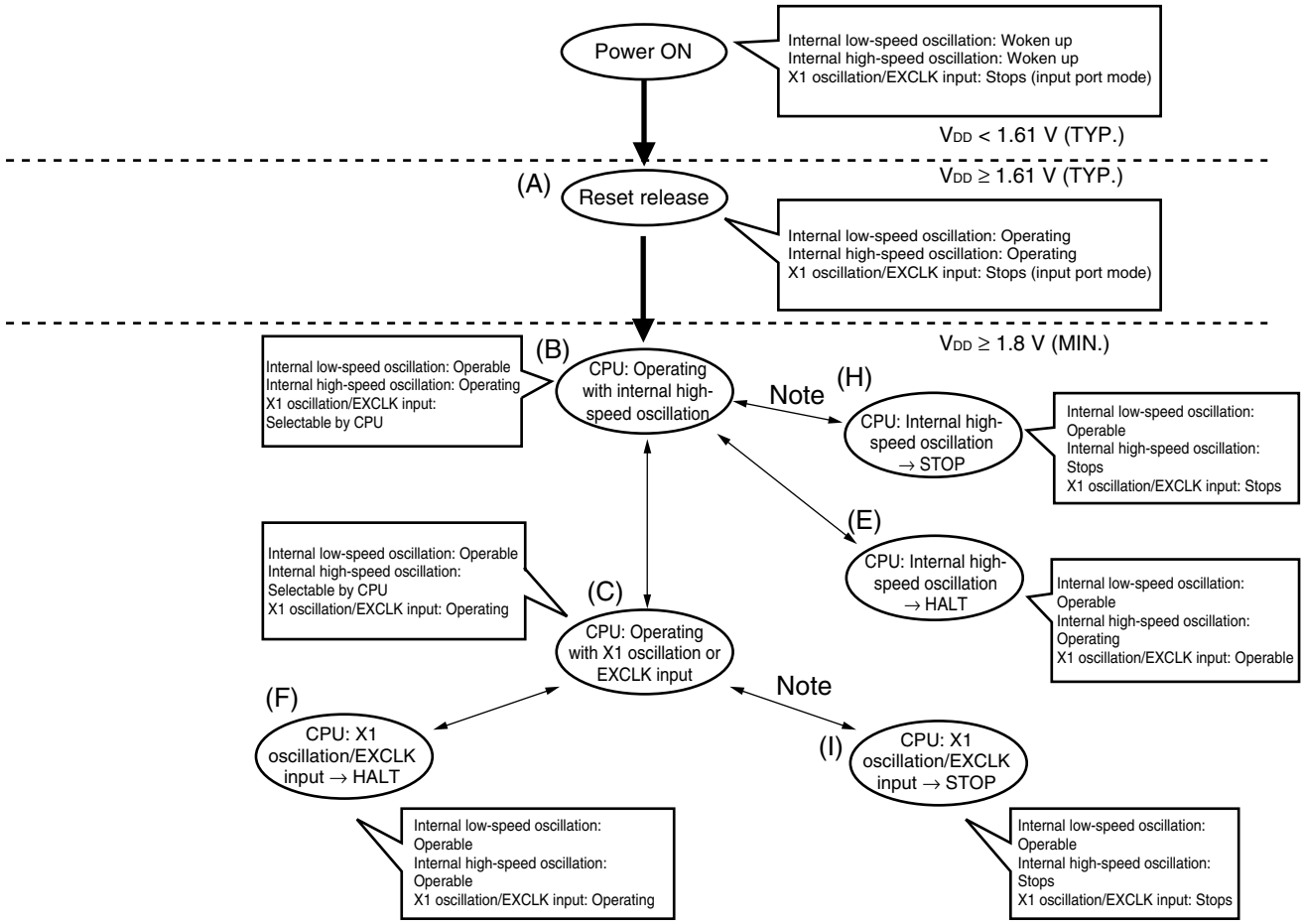


Remark fx: X1 clock oscillation frequency

5.6.6 CPU clock status transition diagram

Figures 5-18 and 5-19 show the CPU clock status transition diagram of this product.

Figure 5-18. CPU Clock Status Transition Diagram (When LVI Default Start Mode Function Stopped Is Set (Option Byte: LVISTART = 0), 78K0/KY2-L, 78K0/KA2-L, and 78K0/KB2-L)



<R> **Note** When transitioning to the STOP mode, it is possible to achieve low power consumption by setting RMC = 56H first.

Remark When LVI default start function enabled is set (option byte: LVISTART = 1), the CPU clock status changes to (A) in the above figure when the supply voltage exceeds 1.91 V (TYP.), and to (B) after reset processing (12 to 51 μs).

6.4.5 Free-running timer operation

When bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 01 (free-running timer mode), 16-bit timer/event counter 00 continues counting up in synchronization with the count clock. When it has counted up to FFFFH, the overflow flag (OVF00) is set to 1 at the next clock, and TM00 is cleared (to 0000H) and continues counting. Clear OVF00 to 0 by executing the CLR instruction via software.

The following three types of free-running timer operations are available.

- Both CR000 and CR010 are used as compare registers.
- One of CR000 or CR010 is used as a compare register and the other is used as a capture register.
- Both CR000 and CR010 are used as capture registers.

Remarks 1. For the setting of the I/O pins, refer to **6.3 (6) Port mode register 0 (PM0)**.

2. For how to enable the INTTM000 signal interrupt, refer to **CHAPTER 17 INTERRUPT FUNCTIONS**.

(1) Free-running timer mode operation

(CR000: compare register, CR010: compare register)

Figure 6-33. Block Diagram of Free-Running Timer Mode
(CR000: Compare Register, CR010: Compare Register)

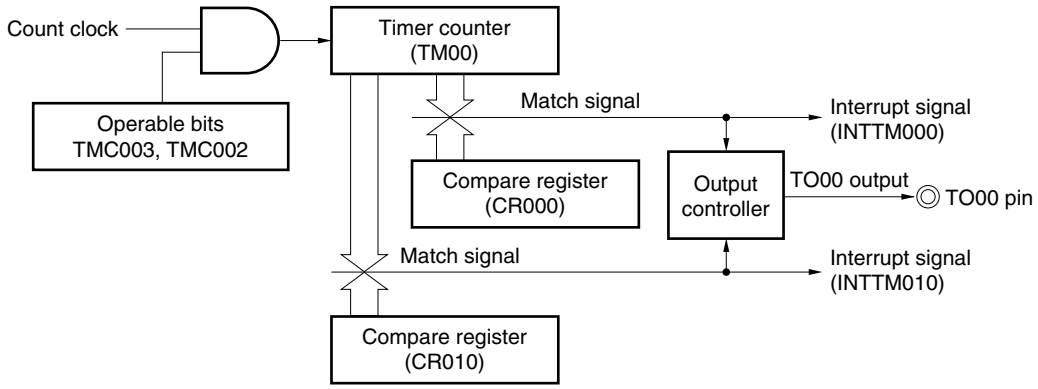
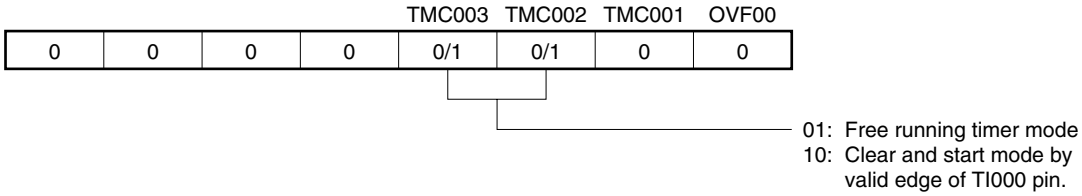
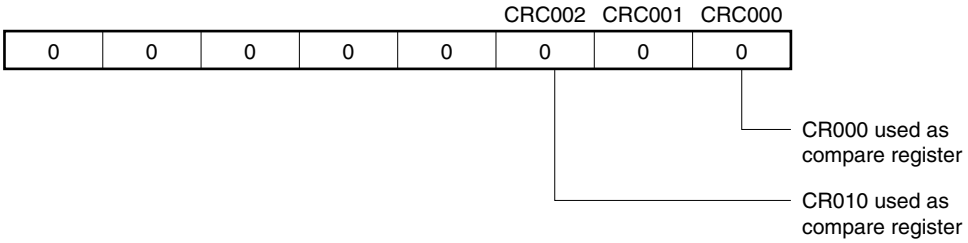


Figure 6-45. Example of Register Settings for One-Shot Pulse Output Operation (1/2)

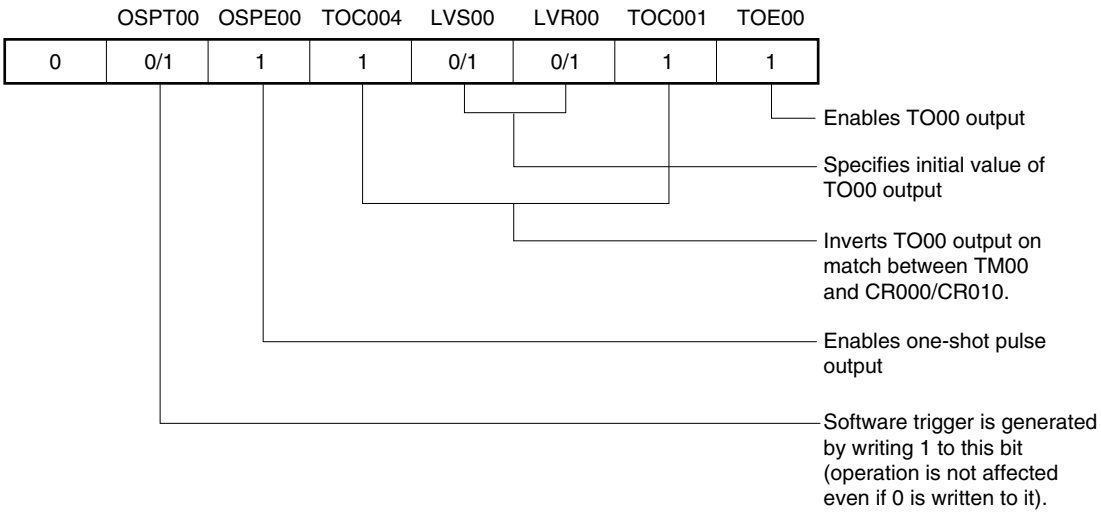
(a) 16-bit timer mode control register 00 (TMC00)



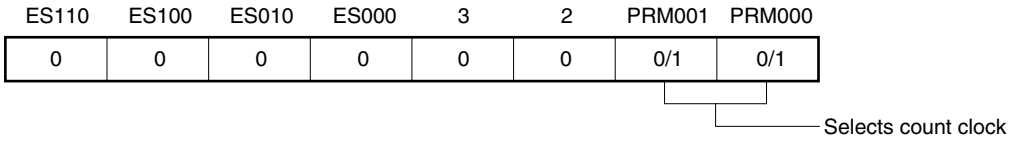
(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)



8.4 Operation of 8-Bit Timers H0 and H1

8.4.1 Operation as interval timer/square-wave output

When the 8-bit timer counter Hn and compare register 0n (CMP0n) match, an interrupt request signal (INTTMHn) is generated and the 8-bit timer counter Hn is cleared to 00H.

Compare register 1n (CMP1n) is not used in interval timer mode. Since a match of the 8-bit timer counter Hn and the CMP1n register is not detected even if the CMP1n register is set, timer output is not affected.

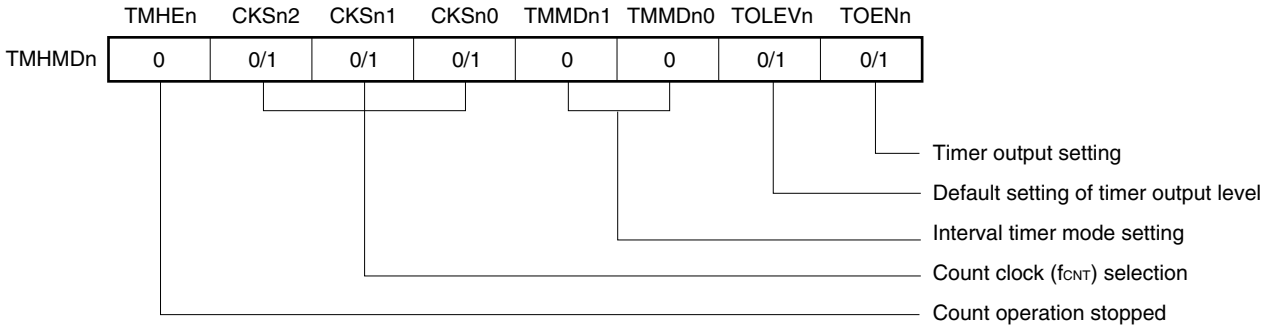
By setting bit 0 (TOENn) of timer H mode register n (TMHMDn) to 1, a square wave of any frequency (duty = 50%) is output from TOHn.

Setting

<1> Set each register.

Figure 8-12. Register Setting During Interval Timer/Square-Wave Output Operation

(i) Setting timer H mode register n (TMHMDn)



(ii) CMP0n register setting

The interval time is as follows if N is set as a comparison value.

- Interval time = (N +1)/f_{CNT}

<2> Count operation starts when TMHEn = 1.

<3> When the values of the 8-bit timer counter Hn and the CMP0n register match, the INTTMHn signal is generated and the 8-bit timer counter Hn is cleared to 00H.

<4> Subsequently, the INTTMHn signal is generated at the same interval. To stop the count operation, clear TMHEn to 0.

Remarks 1. For the setting of the output pin, refer to **8.3 (4) Port mode register 0 (PM0), port mode register 1 (PM1), port mode register 3 (PM3)**.

2. For how to enable the INTTMHn signal interrupt, refer to **CHAPTER 17 INTERRUPT FUNCTIONS**.

3. 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

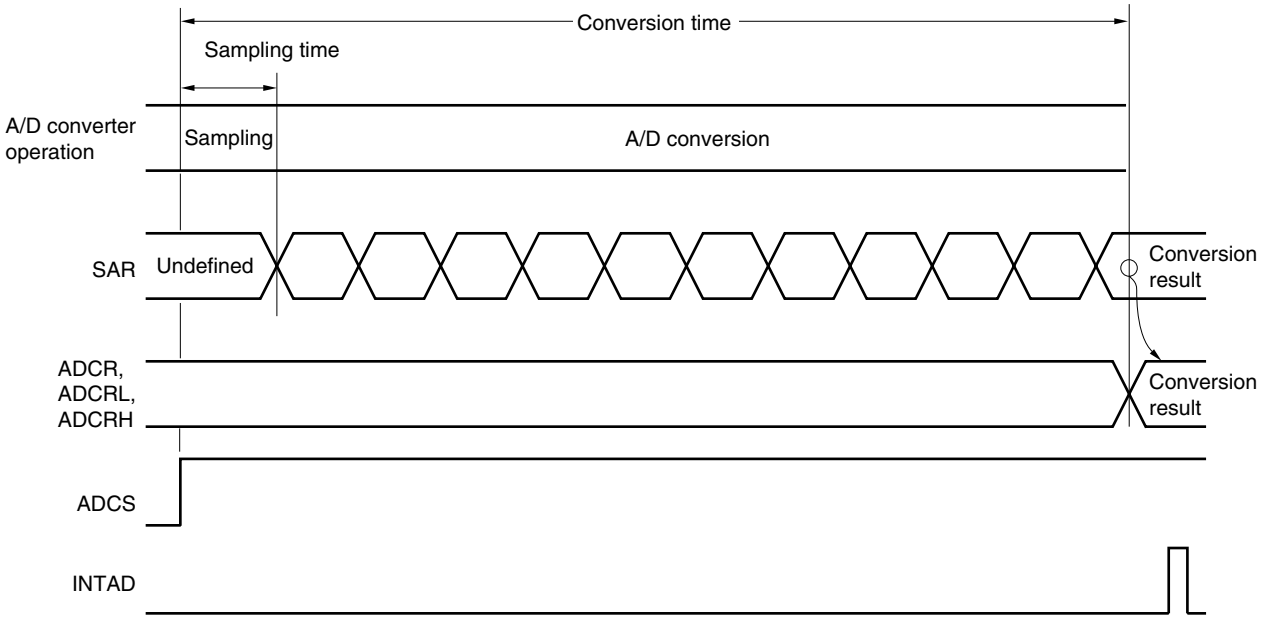
Cautions 1. Make sure the period of <2> to <6> is 1 μs or more.

2. If the timing of <2> is earlier than that of <4>, <2> may be performed any time.

Remark Three types of A/D conversion result registers are available.

- ADCR (16 bits): Store 10-bit A/D conversion value
- ADCRH (8 bits): Store the higher 8-bit A/D conversion value
- ADCRL (8 bits): Store the lower 8-bit A/D conversion value

Figure 12-13. Basic Operation of A/D Converter



A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register 0 (ADM0) is reset (0) by software.

If a write operation is performed to the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH, ADCRL) to 0000H or 00H.

The setting methods are described below.

<1> Set the A/D conversion time and the operation mode by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of the A/D converter mode register 0 (ADM0).
<2> Set bit 0 (ADCE) of ADM0 to 1.
<3> Set the channel to be used to analog input by using the A/D port configuration registers 0, 1 (ADPC0, ADPC1) and port mode registers 1, 2 (PM1, PM2).
<4> Set the PGA operation to set the PGA output or the single AMP operation to set the operational amplifier output for analog input. (refer to **CHAPTER 13 OPERATIONAL AMPLIFIERS**).
<5> Select a channel to be used by using the analog input channel specification register (ADS).
<6> Set bit 7 (ADCS) of ADM0 to 1 to start A/D conversion.
<7> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<8> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH, ADCRL).

<Change the channel>

<9> Set bit 0 (ADMK) of the interrupt mask flag register 1L (MK1L) to 1[Note].
<10> Change the channel by using ADS to start A/D conversion.
<11> Clear bit 0 (ADIF) of the interrupt request flag register 1L (IF1L) to 0.
<12> Clear ADMK to 0[Note].
<13> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<14> Transfer the A/D conversion data to the A/D conversion result register (ADCR, ADCRH, ADCRL).

<Complete A/D conversion>

<15> Clear ADCS to 0.
<16> Clear ADCE to 0.

Note Execute this only if interrupt servicing is used for A/D conversion.

Cautions 1. Make sure the period of <2> to <6> is 1 μs or more.
2. If the timing of <2> is earlier than that of <4>, <2> may be performed any time.
3. <2> can be omitted. However, ignore data of the first conversion after <6> in this case.
4. The period from <7> to <13> differs from the conversion time set using bits 5 to 1 (FR2 to FR0, LV1, LV0) of ADM0. The period from <10> to <13> is the conversion time set using FR2 to FR0, LV1, and LV0.

Figure 13-4. Format of A/D Port Configuration Register 0 (ADPC0)

(a) 78K0/KY2-L

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	ADPCS3	ADPCS2	ADPCS1	ADPCS0

(b) 78K0/KA2-L (20-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

(c) 78K0/KA2-L (25-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	ADPCS6	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

(d) 78K0/KA2-L (32-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	ADPCS7	ADPCS6	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

(e) 78K0/KB2-L

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	ADPCS3	ADPCS2	ADPCS1	ADPCS0

(f) 78K0/KC2-L (40-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	ADPCS6	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

(g) 78K0/KC2-L (44-pin and 48-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	ADPCS7	ADPCS6	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

ADPCSn	Digital I/O or analog I/O selection (n = 0 to 7)
0	Analog I/O
1	Digital I/O

13.4 Operational Amplifier Operations

The operational amplifiers 0 and 1 have the following mode.

- Single AMP mode (operational amplifiers 0 and 1)
- PGA (Programmable gain amplifier) mode (operational amplifier 0 only)

13.4.1 Single AMP mode (operational amplifiers 0 and 1)

Operational amplifiers 0 and 1 both have two input pins (the AMPn- pin and the AMPn+ pin) and one output pin (the AMPnOUT pin), and can be used as single-power supply amplifiers that can be externally connected.

The amplified voltage can be used as an analog input of the A/D converter, because the AMPnOUT pin is alternatively used with analog input pin of the A/D converter.

The procedure for starting operation in single amplifier mode is described below.

<1> Use the ADPCn register to set the pins (AMPn−, AMPn+, AMPnOUT) to be used in single amplifier mode as analog I/O.
<2> Use the PMx register to set the pins (AMPn−, AMPn+, AMPnOUT) to be used in single amplifier mode to input mode.
<3> Set (1) the OPAMPnE bit and enable operation in single amplifier mode.

Caution To use as an input of the A/D converter a voltage that has been amplified in single amplifier mode, enable operation in single amplifier mode before selecting an analog input channel by using the ADS register.

Remark Products with operational amplifier of the 78K0/KY2-L and 78K0/KA2-L: n = 0, x = 2
Products with operational amplifier of the 78K0/KB2-L and 78K0/KC2-L: n = 0, 1, x = 2, 1

13.4.2 PGA (Programmable gain amplifier) mode (operational amplifier 0 only)

In this mode, the analog voltage input from the PGAIN pin is amplified within the microcontroller. The gain can be selected from four types (×4, ×8, ×16, ×32).

The amplified voltage can be used as an analog input of the A/D converter.

The procedure for starting operation in PGA mode is described below.

<1> Use the ADPC0 register to set the pins (PGAIN) to be used in PGA mode as analog I/O.
<2> Use the PM2 register to set the pins (PGAIN) to be used in PGA mode to input mode.
<3> Use the AMP0VG0 and AMP0VG1 bits to select the gain (×4, ×8, ×16, ×32).
<4> Set (1) the PGAEN bit and enable operation in PGA mode.

Caution To use as an input of the A/D converter a voltage that has been amplified in PGA mode, enable operation in PGA mode before selecting an analog input channel by using the ADS register.

15.5.7 Canceling wait

The I^2C usually cancels a wait state by the following processing.

- Writing data to IICA shift register (IICA)
- Setting bit 5 (WREL0) of IICA control register 0 (IICACTL0) (canceling wait)
- Setting bit 1 (STT0) of IICACTL0 register (generating start condition)[Note]
- Setting bit 0 (SPT0) of IICACTL0 register (generating stop condition)[Note]

Note Master only

When the above wait canceling processing is executed, the I^2C cancels the wait state and communication is resumed.

To cancel a wait state and transmit data (including addresses), write the data to the IICA register.

To receive data after canceling a wait state, or to complete data transmission, set bit 5 (WREL0) of the IICA control register 0 (IICACTL0) to 1.

To generate a restart condition after canceling a wait state, set bit 1 (STT0) of the IICACTL0 register to 1.

To generate a stop condition after canceling a wait state, set bit 0 (SPT0) of the IICACTL0 register to 1.

Execute the canceling processing only once for one wait state.

If, for example, data is written to the IICA register after canceling a wait state by setting the WREL0 bit to 1, an incorrect value may be output to SDAA0 line because the timing for changing the SDAA0 line conflicts with the timing for writing the IICA register.

In addition to the above, communication is stopped if the IICE0 bit is cleared to 0 when communication has been aborted, so that the wait state can be canceled.

If the I^2C bus has deadlocked due to noise, processing is saved from communication by setting bit 6 (LREL0) of the IICACTL0 register, so that the wait state can be canceled.

Caution If a processing to cancel a wait state executed when WUP (bit 7 of the IICA control register 1 (IICACTL1)) = 1, the wait state will not be canceled.

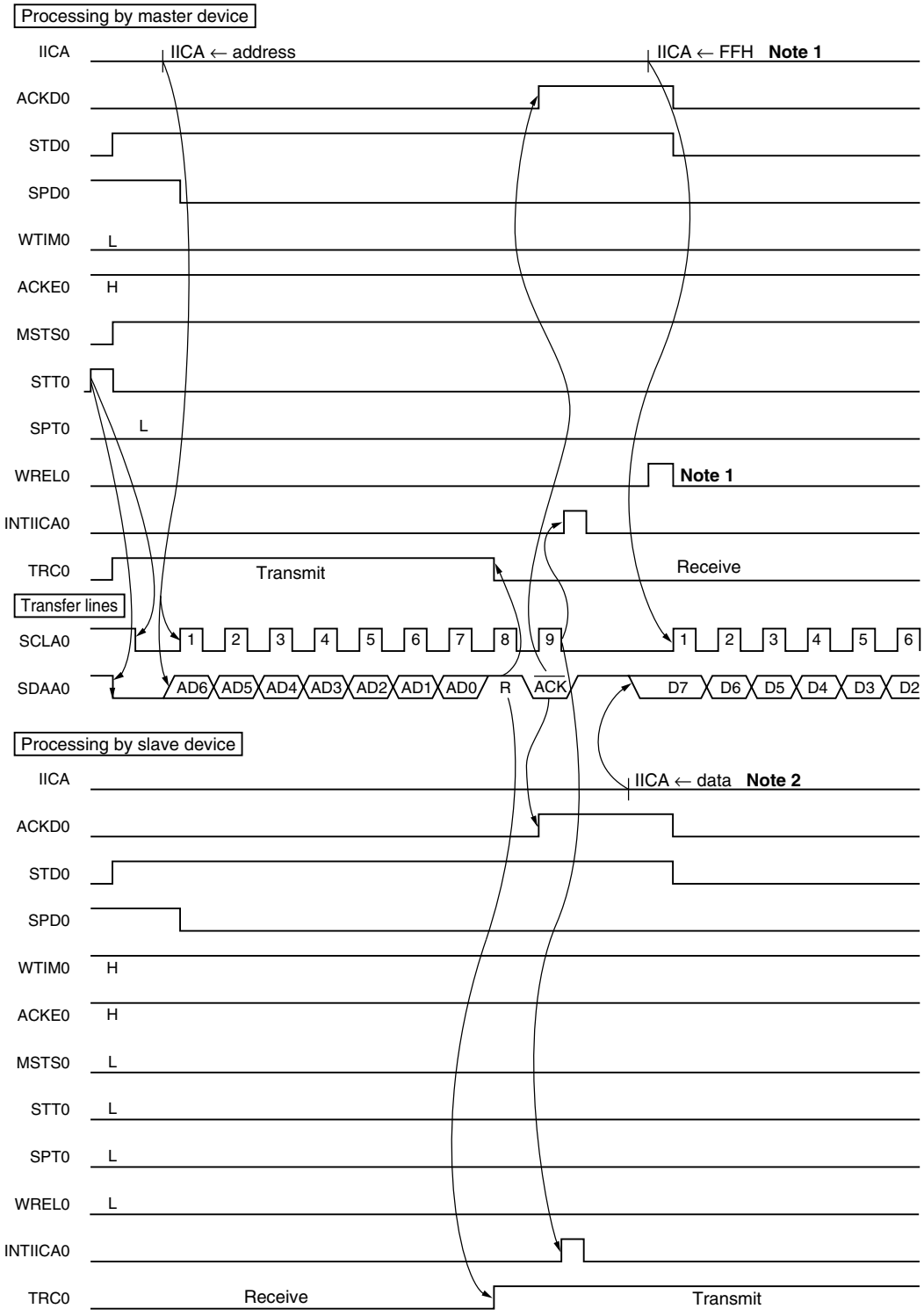
15.5.17 Timing of I²C interrupt request (INTIICA0) occurrence

The timing of transmitting or receiving data and generation of interrupt request signal INTIICA0, and the value of the IICAS0 register when the INTIICA0 signal is generated are shown below.

Remark ST: Start condition
AD6 to AD0: Address
R/$\overline{W}$: Transfer direction specification
$\overline{ACK}$: Acknowledge
D7 to D0: Data
SP: Stop condition

Figure 15-34. Example of Slave to Master Communication
(When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)

(1) Start condition ~ address



Notes 1. To cancel master wait, write “FFH” to IICA or set WREL0.

2. Write data to IICA, not setting WREL0, in order to cancel a wait state during slave transmission.

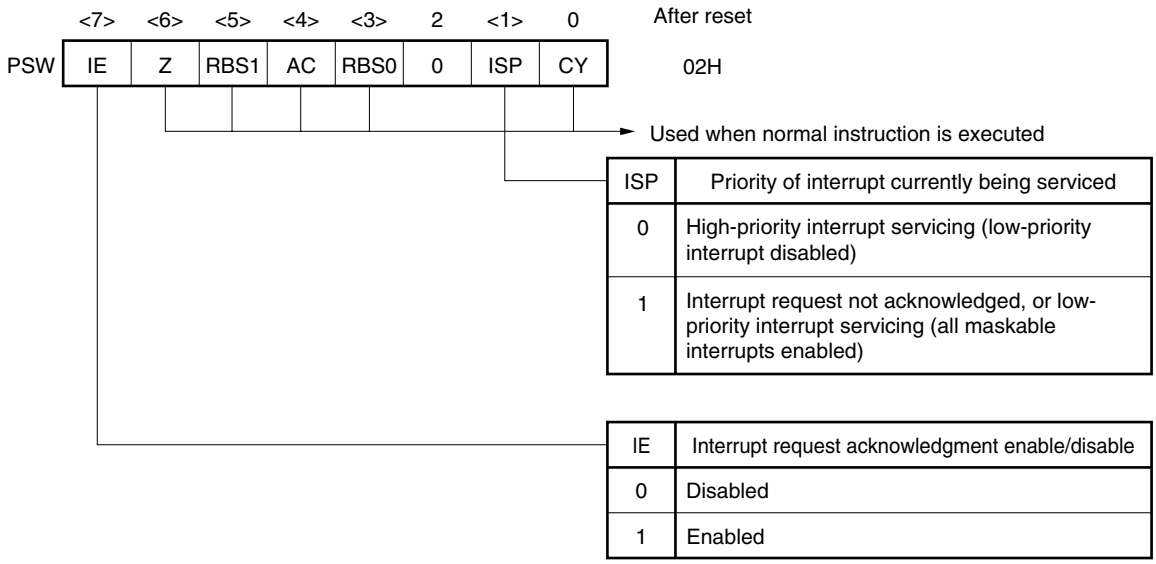
(5) Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for an interrupt request. The IE flag that sets maskable interrupt enable/disable and the ISP flag that controls multiple interrupt servicing are mapped to the PSW.

Besides 8-bit read/write, this register can carry out operations using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged, if the BRK instruction is executed, the contents of the PSW are automatically saved into a stack and the IE flag is reset to 0. If a maskable interrupt request is acknowledged, the contents of the priority specification flag of the acknowledged interrupt are transferred to the ISP flag. The PSW contents are also saved into the stack with the PUSH PSW instruction. They are restored from the stack with the RETI, RETB, and POP PSW instructions.

Reset signal generation sets PSW to 02H.

Figure 17-24. Format of Program Status Word



ISP	Priority of interrupt currently being serviced
0	High-priority interrupt servicing (low-priority interrupt disabled)
1	Interrupt request not acknowledged, or low-priority interrupt servicing (all maskable interrupts enabled)

IE	Interrupt request acknowledgment enable/disable
0	Disabled
1	Enabled

Cautions 1. To stop LVI, follow either of the procedures below.

- **When using 8-bit memory manipulation instruction: Write 00H to LVIM.**
- **When using 1-bit memory manipulation instruction: Clear LVION to 0.**

2. Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.

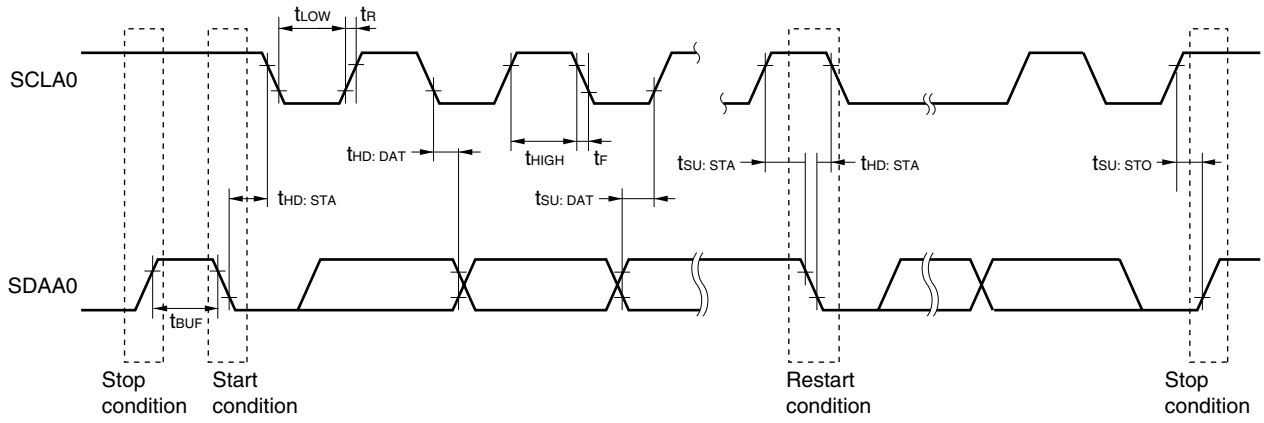
3. If LVI operation is disabled (clears LVION) when LVI is used in interrupt mode (LVIMD = 0), LVISEL is set to 0, and the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), or when LVI is used in interrupt mode (LVIMD = 0), LVISEL is set to 1, and input voltage of external input pin (EXLVI) is less than or equal to the detection voltage (V_{EXLVI})), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

4. For 78K0/KY2-L and 78K0/KA2-L, be sure to clear bit 2 to 0.

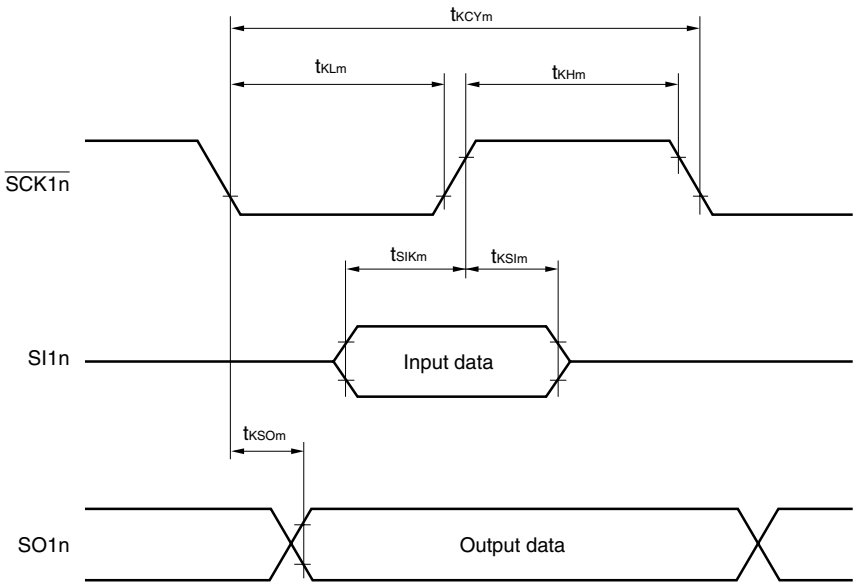
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Serial Transfer Timing

IICA:



CSI1n:

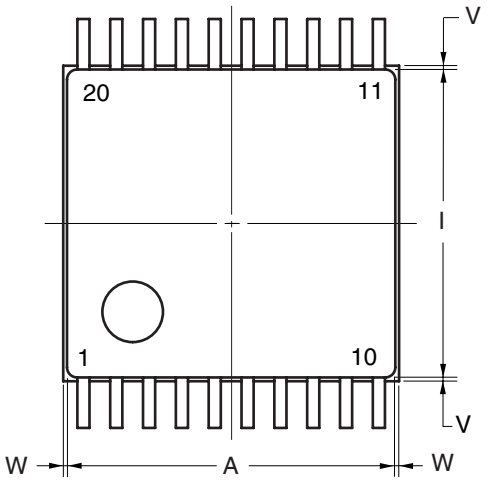


Remark m = 1, 2
n = 0, 1

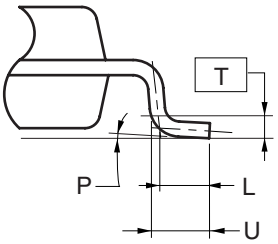
29.2 78K0/KA2-L

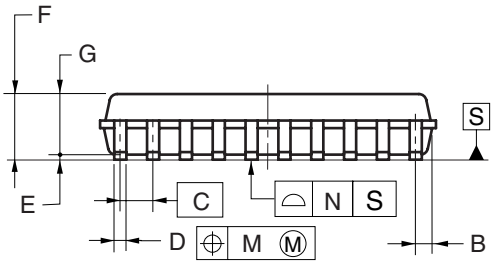
- μPD78F0560MC-CAA-AX, 78F0561MC-CAA-AX, 78F0562MC-CAA-AX, 78F0565MC-CAA-AX, 78F0566MC-CAA-AX, 78F0567MC-CAA-AX

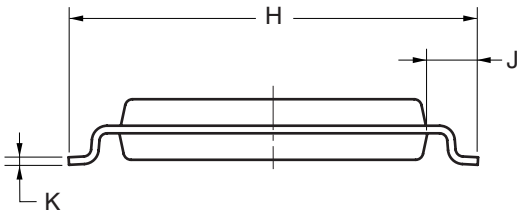
20-PIN PLASTIC SSOP (7.62 mm (300))



detail of lead end







(UNIT:mm)

ITEM	DIMENSIONS
A	6.50±0.10
B	0.325
C	0.65 (T.P.)
D	$0.22^{+0.10}_{-0.05}$
E	0.10±0.05
F	1.30±0.10
G	1.20
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.05}_{-0.01}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

P20MC-65-CAA

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

(5/8)

Edition	Description	Chapter
2nd Edition	Modification of **Caution** in **Figure 17-14 Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (78K0/KB2-L)** to **Figure 17-16 Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (48-pin products of 78K0/KC2-L)**	**CHAPTER 28 ELECTRICAL SPECIFICATIONS (TARGET VALUES)**
	• Addition of reset current (I_{DDrst})	
	(1) A/D Converter in **Analog Characteristics** • Modification of conversion time (t_{CONV}) in **<1> ANI0 to ANI7** • Addition of **<2> ANI8 to ANI10 (78K0/KB2-L and 78K0/KC2-L only)**	
	(3) Operational amplifier 0 in **Analog Characteristics** • Modification of V_{DD} range • Addition of phase margin and large-amplitude voltage gain (AV_{OP0}) • Modification of gain-bandwidth product (GBW_{OP0})	
	(4) Operational amplifier 1 in **Analog Characteristics** • Addition of phase margin and large-amplitude voltage gain (AV_{OP1}) • Modification of gain-bandwidth product (GBW_{OP1})	
	(7) LVI in **Analog Characteristics** • Addition of supply voltage level (V_{LVI14}) and supply voltage when power supply voltage is turned on (V_{DDLVI})	
	Flash Memory Programming Characteristics • Modification of V_{DD} range • Modification of system clock frequency (f_{CLK}) • Modification of Number of rewrites per chip (C_{erwr}) • Addition of **Note 1**	
	Modification of **29.1 78K0/KY2-L**	**CHAPTER 29 PACKAGE DRAWINGS**
	Addition of preliminary	**CHAPTER 30 RECOMMENDED SOLDERING CONDITIONS (PRELIMINARY)**
	Modification of URL of download site for development tools	**APPENDIX A DEVELOPMENT TOOLS**
	Addition of chapter	**APPENDIX B REGISTER INDEX**
	Addition of chapter	**APPENDIX C REVISION HISTORY**

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents