Renesas Electronics America Inc - UPD78F0567MC-CAA-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0567mc-caa-ax

(2) 25-pin plastic FLGA (3x3) (2/2)

Note μPD78F0565, 78F0566, 78F0567 (products with operational amplifier) only

Cautions 1. V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

3. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, and ANI3/P23 to ANI6/P26 are set in the analog input mode after release of reset.

4. $\overline{\text{RESET}}$/P125 immediately after release of reset is set in the external reset input.

5. Set P30 and P01 to output mode (PM30 = PM01 = 0) by using software after release of reset.

Remark Functions in parentheses ( ) in the figure above can be assigned by setting the port alternate switch control register (MUXSEL).

<R> **(3) 32-pin plastic WQFN (5x5) (1/2)**

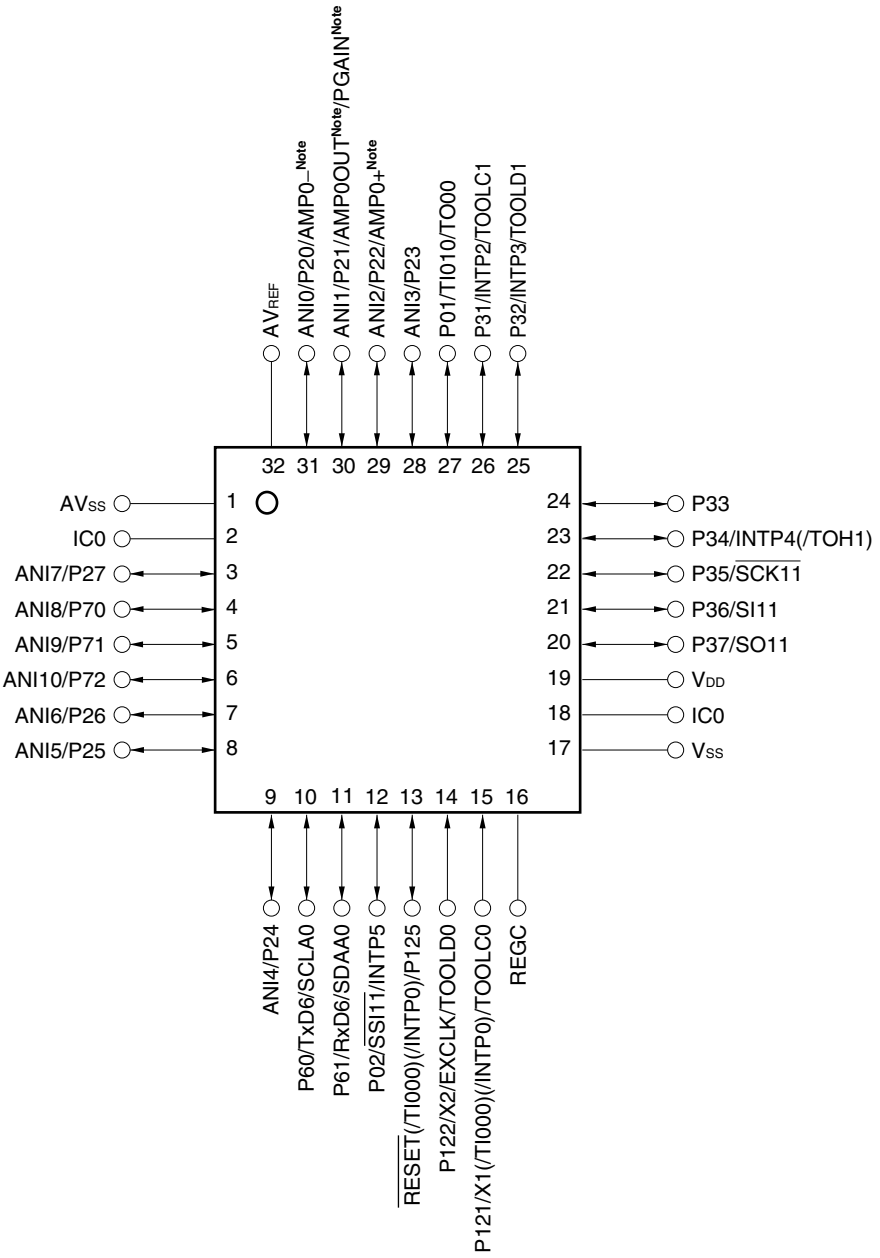
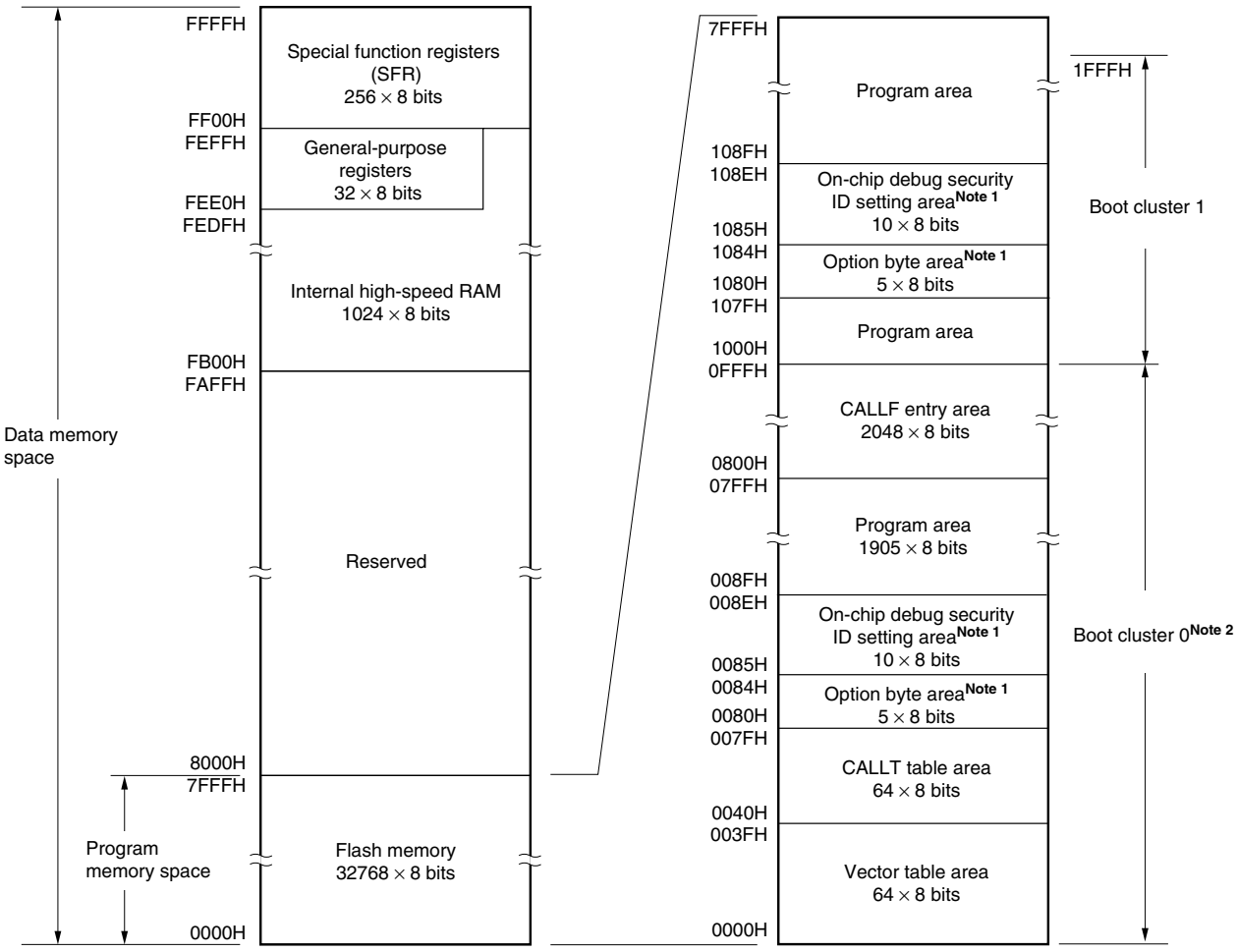


Figure 3-4. Memory Map (μPD78F0573, 78F0578, 78F0583, 78F0588)

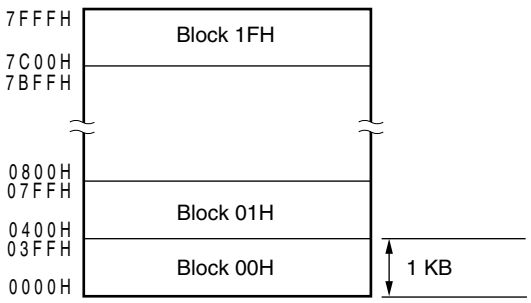


Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (refer to **25.6 Security Settings**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, refer to **Table 3-2 Correspondence Between Address Values and Block Numbers in Flash Memory**.



(2) CALLT instruction table area

The 64-byte area 0040H to 007FH can store the subroutine entry address of a 1-byte call instruction (CALLT).

(3) Option byte area

A 5-byte area of 0080H to 0084H and 1080H to 1084H can be used as an option byte area. Set the option byte at 0080H to 0084H when the boot swap is not used, and at 0080H to 0084H and 1080H to 1084H when the boot swap is used. For details, refer to **CHAPTER 24 OPTION BYTE**.

(4) On-chip debug security ID setting area

A 10-byte area of 0085H to 008EH and 1085H to 108EH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 0085H to 008EH when the boot swap is not used and at 0085H to 008EH and 1085H to 108EH when the boot swap is used. For details, refer to **CHAPTER 26 ON-CHIP DEBUG FUNCTION**.

(5) CALLF instruction entry area

The area 0800H to 0FFFH can perform a direct subroutine call with a 2-byte call instruction (CALLF).

3.1.2 Internal data memory space

78K0/Kx2-L microcontrollers incorporate the following RAMs.

(1) Internal high-speed RAM

Table 3-5. Internal High-Speed RAM Capacity

Product				Internal High-Speed RAM
78K0/KY2-L	78K0/KA2-L	78K0/KB2-L	78K0/KC2-L	
μPD78F0550, 78F0555	μPD78F0560, 78F0565	–	–	384 × 8 bits (FD80H to FEFFH)
μPD78F0551, 78F0556	μPD78F0561, 78F0566	μPD78F0571, 78F0576	μPD78F0581, 78F0586	512 × 8 bits (FD00H to FEFFH)
μPD78F0552, 78F0557	μPD78F0562, 78F0567	μPD78F0572, 78F0577	μPD78F0582, 78F0587	768 × 8 bits (FC00H to FEFFH)
–	–	μPD78F0573, 78F0578	μPD78F0583, 78F0588	1024 × 8 bits (FB00H to FEFFH)

The 32-byte area FEE0H to FEFFH is assigned to four general-purpose register banks consisting of eight 8-bit registers per bank.

This area cannot be used as a program area in which instructions are written and executed.

The internal high-speed RAM can also be used as a stack memory.

3.1.3 Special function register (SFR) area

On-chip peripheral hardware special function registers (SFRs) are allocated in the area FF00H to FFFFH (refer to **Tables 3-6 to 3-9 Special Function Register List** in **3.2.3 Special function registers (SFRs)**).

Caution Do not access addresses to which SFRs are not assigned.

4.2 Port Configuration

Ports include the following hardware.

<R>

Table 4-7. Port Configuration

Item	Configuration
Control registers	Port mode registers (PMxx): PM0, PM1[Note 1], PM2, PM3, PM4[Note 2], PM6, PM7[Note 3], PM12[Note 1] Port registers (Pxx): P0, P1[Note 1], P2, P3, P4[Note 2], P6, P7[Note 3], P12 Pull-up resistor option registers (PUxx): PU0, PU1[Note 1], PU3, PU4[Note 2], PU6, PU7[Note 4], PU12 Port input mode register 6 (PIM6) Port output mode register 6 (POM6) Reset pin mode register (RSTMASK) A/D port configuration register 0 (ADPC0) A/D port configuration register 1 (ADPC1)[Note 1] Port alternate switch control register (MUXSEL)[Note 5]
Port	• 78K0/KY2-L: Total: 12 (CMOS I/O: 9, CMOS input: 3) • 20-pin products of 78K0/KA2-L: Total: 16 (CMOS I/O: 13, CMOS input: 3) • 25-pin products of 78K0/KA2-L: Total: 21 (CMOS I/O: 18, CMOS input: 3) • 32-pin products of 78K0/KA2-L: Total: 25 (CMOS I/O: 22, CMOS input: 3) • 78K0/KB2-L: Total: 24 (CMOS I/O: 21, CMOS input: 3) • 40-pin products of 78K0/KC2-L: Total: 34 (CMOS I/O: 29, CMOS input: 5) • 44-pin products of 78K0/KC2-L: Total: 38 (CMOS I/O: 33, CMOS input: 5) • 48-pin products of 78K0/KC2-L: Total: 42 (CMOS I/O: 37, CMOS input: 5)
Pull-up resistor	• 78K0/KY2-L: Total: 6 • 20-pin products of 78K0/KA2-L: Total: 8 • 25-pin products of 78K0/KA2-L: Total: 12 • 32-pin products of 78K0/KA2-L: Total: 12 • 78K0/KB2-L: Total: 18 • 40-pin products of 78K0/KC2-L: Total: 22 • 44-pin products of 78K0/KC2-L: Total: 26 • 48-pin products of 78K0/KC2-L: Total: 30

Notes 1. 78K0/KB2-L and 78K0/KC2-L only

2. 78K0/KC2-L (44-pin and 48-pin products) only

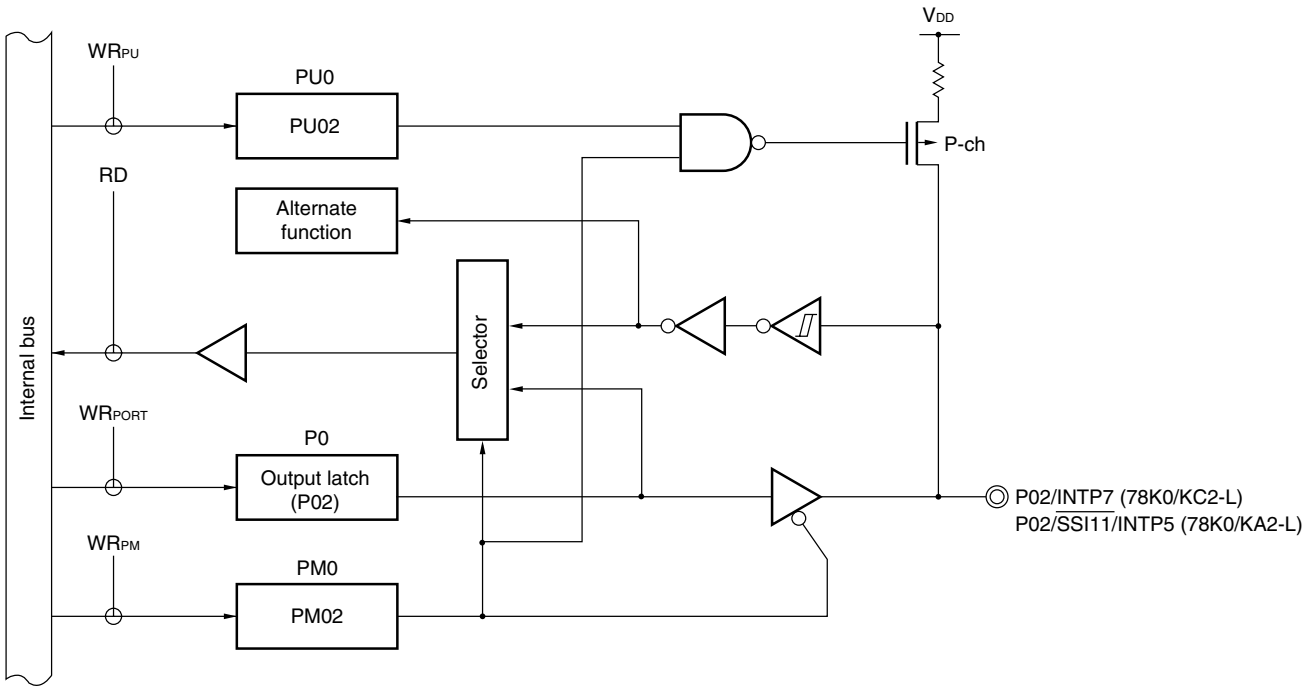
3. 78K0/KA2-L (32-pin products) and 78K0/KC2-L only

4. 78K0/KC2-L only

5. 78K0/KA2-L (25-pin and 32-pin products) and 78K0/KC2-L (44-pin and 48-pin products) only

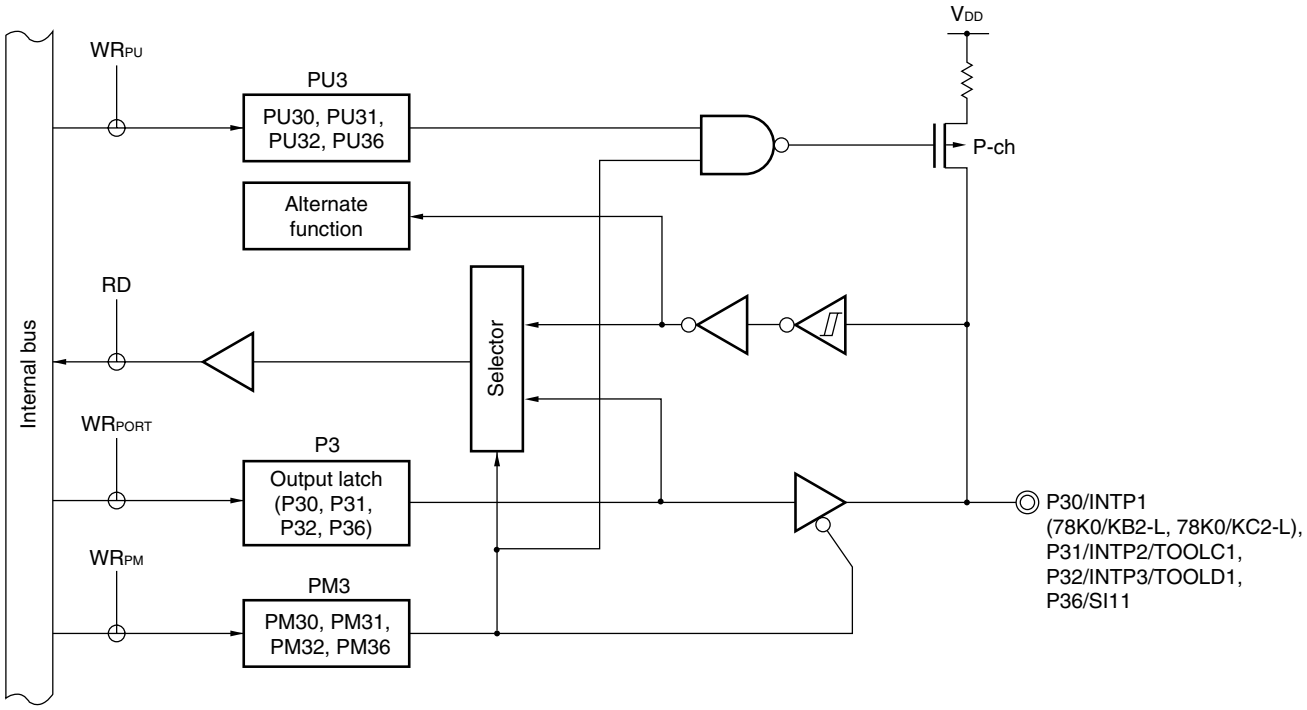
<R>

Figure 4-3. Block Diagram of P02



P0: Port register 0
PU0: Pull-up resistor option register 0
PM0: Port mode register 0
RD: Read signal
WR××: Write signal

Figure 4-16. Block Diagram of P30 (78K0/KB2-L, 78K0/KC2-L), P31, P32, P36



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

5.6.3 Example of controlling subsystem clock

The following two types of subsystem clocks[Note] are available.

- XT1 clock: Crystal/ceramic resonator is connected across the XT1 and XT2 pins.
- External subsystem clock: External clock is input to the EXCLKS pin.

When the subsystem clock is not used, the XT1/P123 and XT2/EXCLKS/P124 pins can be used as input port pins.

Note 78K0/KC2-L only

Cautions 1. The XT1/P123 and XT2/EXCLKS/P124 pins are in the input port mode after a reset release.

2. Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

The following describes examples of setting procedures for the following cases.

(1) When oscillating XT1 clock
(2) When using external subsystem clock
(3) When using subsystem clock as CPU clock
(4) When stopping subsystem clock

(1) Example of setting procedure when oscillating the XT1 clock

<1> Setting XT1 and XT2 pins and selecting operation mode (PCC and OSCCTL registers)
When a value is specified for XTSTART and EXCLKS and OSCSELS are set to the values below, the system switches from the port mode to the XT1 oscillation mode. set as any of the following, the mode is switched from port mode to XT1 oscillation mode.

XTSTART	EXCLKS	OSCSELS	Operation Mode of Subsystem Clock Pin	P123/XT1 Pin	P124/XT2/ EXCLKS Pin
0	0	1	XT1 oscillation mode	Crystal/ceramic resonator connection	
1	×	×			

Remark ×: don't care

<2> Waiting for the stabilization of the subsystem clock oscillation
Wait for the oscillation stabilization time of the subsystem clock by software, using a timer function.

Caution Do not change the value of XTSTART, EXCLKS, and OSCSELS while the subsystem clock is operating.

(2) Example of setting procedure when using the external subsystem clock

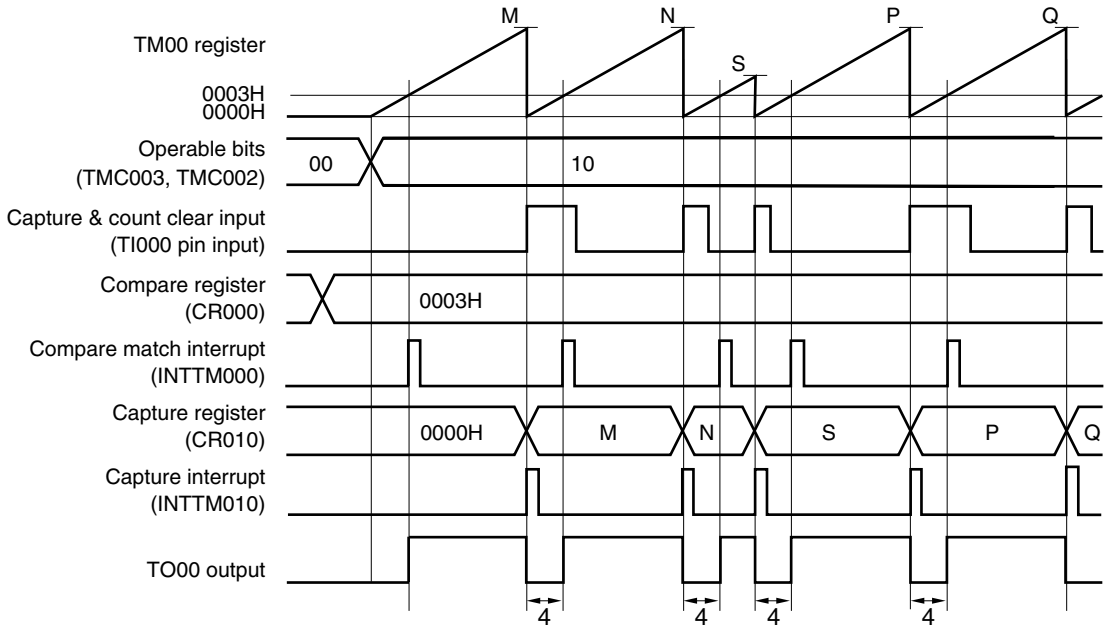
<1> Setting XT1 and XT2 pins, selecting XT1 clock/external clock and controlling oscillation (PCC and OSCCTL registers)
When XTSTART is cleared to 0 and EXCLKS and OSCSELS are set to 1, the mode is switched from port mode to external clock input mode. In this case, input the external clock to the EXCLKS/XT2/P124 pins.

XTSTART	EXCLKS	OSCSELS	Operation Mode of Subsystem Clock Pin	P123/XT1 Pin	P124/XT2/ EXCLKS Pin
0	1	1	External clock input mode	Input port	External clock input

Caution Do not change the value of XTSTART, EXCLKS, and OSCSELS while the subsystem clock is operating.

Figure 6-26. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (2/2)

(b) TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 0AH, CR000 = 0003H

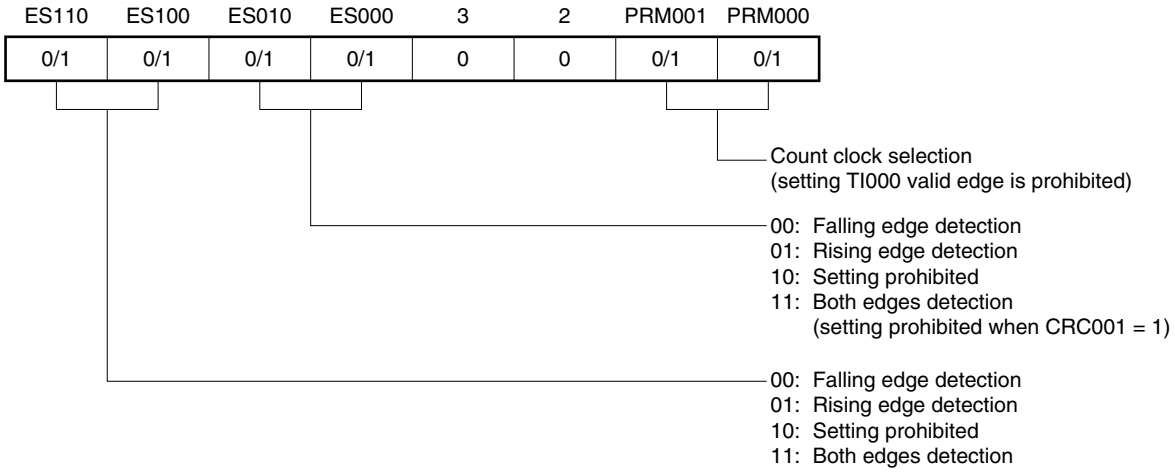


This is an application example where the width set to CR000 (4 clocks in this example) is to be output from the TO00 pin when the count value has been captured & cleared.

The count value is captured to CR010, a capture interrupt signal (INTTM010) is generated, TM00 is cleared (to 0000H), and the TO00 output level is inverted when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0003H (four clocks have been counted), a compare match interrupt signal (INTTM000) is generated and the TO00 output level is inverted.

Figure 6-39. Example of Register Settings in Free-Running Timer Mode (2/2)

(d) Prescaler mode register 00 (PRM00)



(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM000) is generated. The count value of TM00 is not cleared.

To use this register as a capture register, select either the TI000 or TI010 pin input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR000.

(g) 16-bit capture/compare register 010 (CR010)

When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM010) is generated. The count value of TM00 is not cleared.

When this register is used as a capture register, the TI000 pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR010.

(7) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code. If a value outside this range is set, the register value returns to the normal value after 1 period.

MIN can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-8. Format of Minute Count Register (MIN)

Address: FFB3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
MIN	0	MIN40	MIN20	MIN10	MIN8	MIN4	MIN2	MIN1

(8) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12, 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time counter control register 0 (RTCC0).

If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system.

If a value outside the range is set, the register value returns to the normal value after 1 period.

HOUR can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Figure 10-9. Format of Hour Count Register (HOUR)

Address: FFB4H After reset: 12H R/W

Symbol	7	6	5	4	3	2	1	0
HOUR	0	0	HOUR20	HOUR10	HOUR8	HOUR4	HOUR2	HOUR1

Caution Bit 5 (HOUR20) of HOUR indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

12.2 Configuration of A/D Converter

The A/D converter includes the following hardware.

(1) ANI0 to ANI10 pins

These are the analog input pins of the 11-channel A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

<R> **Remark** A/D converter analog input pins differ depending on products.

- 78K0/KY2-L: ANI0 to ANI3
- 78K0/KA2-L (20-pin products): ANI0 to ANI5
- 78K0/KA2-L (25-pin products): ANI0 to ANI6
- 78K0/KA2-L (32-pin products): ANI0 to ANI10
- 78K0/KB2-L: ANI0 to ANI3, ANI8 to ANI10
- 78K0/KC2-L (40-pin product): ANI0 to ANI6, ANI8 to ANI10
- 78K0/KC2-L (44-pin and 48-pin products): ANI0 to ANI10

(2) AMP0OUT pin (products with operational amplifier only)

AMP0OUT is the output pin of operational amplifier 0.

This functions alternately as ANI1. The A/D converter can perform A/D conversion by selecting the output signal of operational amplifier 0 as the analog input source.

(3) AMP1OUT pin (products with operational amplifier of 78K0/KB2-L and 78K0/KC2-L only)

AMP1OUT is the output pin of operational amplifier 1.

This functions alternately as ANI9. The A/D converter can perform A/D conversion by selecting the output signal of operational amplifier 1 as the analog input source.

<R> **(4) PGAOUT signal (products with operational amplifier only)**

PGAOUT is the output signal of PGA.

The A/D converter can perform A/D conversion by selecting the output signal of PGA as the analog input source.

(5) Sample & hold circuit

The sample & hold circuit samples each of the analog input voltages sequentially sent from the input circuit, and sends them to the A/D voltage comparator. This circuit also holds the sampled analog input voltage during A/D conversion.

(6) Comparison voltage generator

The comparison voltage generator is connected between AV_{REF} and AV_{SS}, and generates a voltage to be compared with an analog input. The operation of the comparison voltage generator is enabled or disabled by using the ADCS bit (bit 7 of the ADM0 register). The power consumption can be reduced by stopping the operation of the comparison voltage generator when A/D conversion is not performed.

(7) A/D voltage comparator

The A/D voltage comparator compares the sampled voltage values with the output voltage of the comparison voltage generator. The operation of the A/D voltage comparator is enabled or disabled by using the ADCE bit (bit 0 of the ADM0 register). The power consumption can be reduced by stopping the operation of the A/D voltage comparator when A/D conversion is not performed.

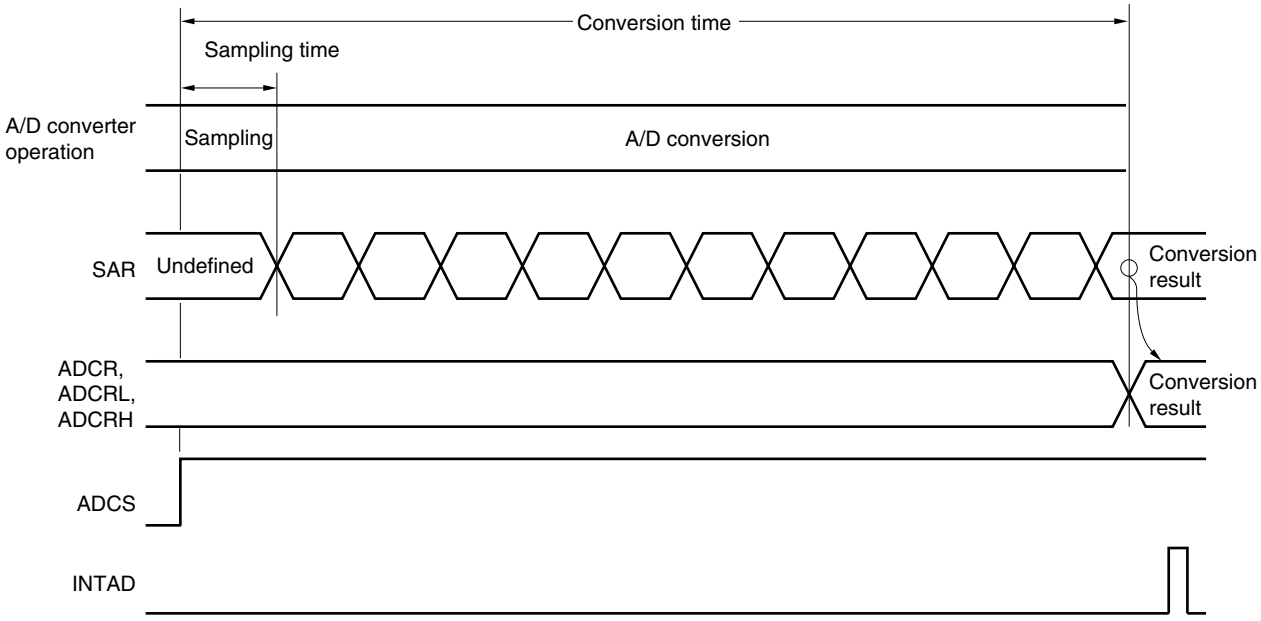
Cautions 1. Make sure the period of <2> to <6> is 1 μs or more.

2. If the timing of <2> is earlier than that of <4>, <2> may be performed any time.

Remark Three types of A/D conversion result registers are available.

- ADCR (16 bits): Store 10-bit A/D conversion value
- ADCRH (8 bits): Store the higher 8-bit A/D conversion value
- ADCRL (8 bits): Store the lower 8-bit A/D conversion value

Figure 12-13. Basic Operation of A/D Converter



A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register 0 (ADM0) is reset (0) by software.

If a write operation is performed to the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH, ADCRL) to 0000H or 00H.

12.6 Cautions for A/D Converter

(1) Operating current in STOP mode

To satisfy the DC characteristics of the power supply current in STOP mode, clear bits 7 (ADCS) and 0 (ADCE) of A/D converter mode register 0 (ADM0) to 0 before executing a STOP instruction.

To restart from the standby status, clear bit 0 (ADIF) of interrupt request flag register 1L (IF1L) to 0 and start operation.

(2) Input range of ANI0 to ANI10

Observe the rated range of the ANI0 to ANI10 input voltage. If a voltage of AV_{REF} or higher and AV_{SS} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

(3) Conflicting operations

<1> Conflict between A/D conversion result register (ADCR, ADCRL, ADCRH) write and ADCR, ADCRL, or ADCRH read by instruction upon the end of conversion

ADCR, ADCRL, or ADCRH read has priority. After the read operation, the new conversion result is written to ADCR, ADCRL, or ADCRH.

<2> Conflict between ADCR, ADCRL, or ADCRH write and A/D converter mode register 0 (ADM0) write, analog input channel specification register (ADS), or A/D port configuration registers 0, 1 (ADPC0, ADPC1) write upon the end of conversion

ADM0, ADS, ADPC0, or ADPC1 write has priority. ADCR, ADCRL, or ADCRH write is not performed, nor is the conversion end interrupt signal (INTAD) generated.

(4) Noise countermeasures

To maintain the 10-bit resolution, attention must be paid to noise input to the AV_{REF} pin and pins ANI0 to ANI10.

<1> Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external C as shown in Figure 12-22 is recommended.

<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

Figure 15-5. Format of IICA Control Register 0 (IICACTL0) (1/4)

Address: FFA7H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICACTL0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

IICE0	I^2C operation enable
0	Stop operation. Reset the IICA status register 0 (IICAS0)[Note 1]. Stop internal operation.
1	Enable operation.
Be sure to set this bit (1) while the SCLA0 and SDLA0 lines are at high level.	
Condition for clearing (IICE0 = 0)	Condition for setting (IICE0 = 1)
• Cleared by instruction • Reset	• Set by instruction

LREL0[Notes 2,3]	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCLA0 and SDAA0 lines are set to high impedance. The following flags of IICA control register 0 (IICACTL0) and IICA status register 0 (IICAS0) are cleared to 0. • STT0 • SPT0 • MSTS0 • EXC0 • COI0 • TRC0 • ACKD0 • STD0
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL0 = 0)	Condition for setting (LREL0 = 1)
• Automatically cleared after execution • Reset	• Set by instruction

WREL0[Notes 2,3]	Wait cancellation
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared after wait is canceled.
When WREL0 is set (wait canceled) during the wait period at the ninth clock pulse in the transmission status (TRC0 = 1), the SDAA0 line goes into the high impedance state (TRC0 = 0).	
Condition for clearing (WREL0 = 0)	Condition for setting (WREL0 = 1)
• Automatically cleared after execution • Reset	• Set by instruction

Notes 1. The IICAS0 register, the STCF and IICBSY bits of the IICAF0 register, and the CLD0 and DAD0 bits of the IICACTL1 register are reset.

2. The signals of these bits are invalid while the IICE0 bit is 0.

3. When the LREL0 and WREL0 bits are read, 0 is always read.

Caution If the operation of I^2C is enabled (IICE0 = 1) when the SCLA0 line is high level, the SDAA0 line is low level, and the digital filter is turned on (DFC0 of the IICACTL1 register = 1), a start condition will be inadvertently detected immediately. In this case, set (1) the LREL0 bit by using a 1-bit memory manipulation instruction immediately after enabling operation of I^2C (IICE0 = 1).

Table 16-2. Relationship Between Register Settings and Pins (4/4)

(d) Serial interface CSI11 (78K0/KA2-L (25-pin and 32-pin products))

CSIE11	TRMD11	SSE11	PM36	P36	PM37	P37	PM35	P35	PM02	P02	CSI11 Operation	Pin Function			
												SI11/P36	SO11/P37	$\overline{\text{SCK11}}$/P35	$\overline{\text{SSI11}}$/P02/INTP5
0	0	×	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	Stop	P36	P37	P35Note 2	P02/INTP5
1	0	0	1	×	×Note 1	×Note 1	1	×	×Note 1	×Note 1	Slave reception Note 3	SI11	P37	$\overline{\text{SCK11}}$ (input) Note 3	P02/INTP5
		1							1	×					$\overline{\text{SSI11}}$
1	1	0	×Note 1	×Note 1	0	0	1	×	×Note 1	×Note 1	Slave transmission Note 3	P36	SO11	$\overline{\text{SCK11}}$ (input) Note 3	P02/INTP5
		1							1	×					$\overline{\text{SSI11}}$
1	1	0	1	×	0	0	1	×	×Note 1	×Note 1	Slave transmission/ reception Note 3	SI11	SO11	$\overline{\text{SCK11}}$ (input) Note 3	P02/INTP5
		1							1	×					$\overline{\text{SSI11}}$
1	0	0	1	×	×Note 1	×Note 1	0	1	×Note 1	×Note 1	Master reception	SI11	P37	$\overline{\text{SCK11}}$ (output)	P02/INTP5
1	1	0	×Note 1	×Note 1	0	0	0	1	×Note 1	×Note 1	Master transmission	P36	SO11	$\overline{\text{SCK11}}$ (output)	P02/INTP5
1	1	0	1	×	0	0	0	1	×Note 1	×Note 1	Master transmission/ reception	SI11	SO11	$\overline{\text{SCK11}}$ (output)	P02/INTP5

Notes 1. Can be set as port function.

2. To use P37/$\overline{\text{SCK11}}$ as port pins, clear CKP11 to 0.

3. To use the slave mode, set CKS112, CKS111, and CKS110 to 1, 1, 1.

Remark ×: don't care

CSIE11: Bit 7 of serial operation mode register 11 (CSIM11)

TRMD11: Bit 6 of CSIM11

CKP11: Bit 4 of serial clock selection register 11 (CSIC11)

CKS112, CKS111, CKS110: Bits 2 to 0 of CSIC11

PM×: Port mode register

P×: Port output latch

Figure 17-7. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H)
(44-pin products of 78K0/KC2-L)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	CSIIF10	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
IF1L	PIF8	0	RTCIF	KRIF	TMIF51	RTCIIF	0	ADIF

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
IF1H	0	0	0	PIF11	PIF10	PIF9	CSIIF11	IICAIF0

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Caution Be sure to clear bits 1 and 6 of IF1L, and bits 5 to 7 of IF1H to 0.

CHAPTER 25 FLASH MEMORY

The 78K0/Kx2-L microcontrollers incorporates the flash memory to which a program can be written, erased, and overwritten while mounted on the board.

25.1 Internal Memory Size Switching Register

Select the internal memory capacity using the internal memory size switching register (IMS).
IMS is set by an 8-bit memory manipulation instruction.
Reset signal generation sets IMS to CFH.

Caution Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated Table 25-1 after release of reset.

Figure 25-1. Format of Internal Memory Size Switching Register (IMS)

Address: FFF0H After reset: CFH R/W

Symbol	7	6	5	4	3	2	1	0
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
0	0	0	768 bytes
0	1	0	512 bytes
0	1	1	384 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
0	0	0	1	4 KB
0	0	1	0	8 KB
0	1	0	0	16 KB
1	0	0	0	32 KB
1	1	1	1	(Default value)
Other than above				Setting prohibited

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (78K0/KY2-L, 78K0/KA2-L (20 pins), 78K0/KB2-L, 78K0/KC2-L) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	AV_{REF}		−0.5 to V_{DD} + 0.3 Note 1	V
	AV_{SS}		−0.5 to +0.3	V
REGC pin input voltage Note 2	V_{IREGC}		−0.5 to +3.6 and −0.5 to V_{DD} +0.3	V
Input voltage	V_{I1}	P00 to P02, P10 to P17, P30 to P33, P40 to P42, P60 to P63, P70 to P75, P120 to P125, X1, X2, XT1, XT2, $\overline{\text{RESET}}$	−0.3 to V_{DD} + 0.3 Note 1	V
	V_{I2}	P20 to P27	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V
Output voltage	V_{O1}	P00 to P02, P10 to P17, P30 to P33, P40 to P42, P60 to P63, P70 to P75, P120	−0.3 to V_{DD} + 0.3 Note 1	V
	V_{O2}	P20 to P27	−0.3 to AV_{REF} + 0.3 Note 1	V
Analog input voltage	V_{AN1}	ANI0 to ANI7, AMP0+, AMP0-	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V
	V_{AN2}	ANI8 to ANI10, AMP1+, AMP1-	−0.3 to V_{DD} + 0.3 Note 1	V

Notes 1. Must be 6.5 V or lower.

2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(b) IICA

Parameter	Symbol	Conditions	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: $f_{PRS} \geq 3.5$ MHz, Normal mode: $f_{PRS} \geq 1$ MHz	0	100	0	400	kHz
Setup time of start condition and stop condition	$t_{SU:STA}$		4.7	–	0.6	–	μs
Hold time[Note 1]	$t_{HD:STA}$		4.0	–	0.6	–	μs
Hold time when SCLA0 = "L"	t_{LOW}		4.7	–	1.3	–	μs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0	–	0.6	–	μs
Data setup time (reception)	$t_{SU:DAT}$		250	–	100	–	ns
Data hold time (transmission)[Notes 2,3]	$t_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		4.0	–	0.6	–	μs
Bus free time between stop condition and start condition	t_{BUF}		4.7	–	1.3	–	μs
Rise time of SDAA0 and SCLA0 signals	t_R			1000	2.0+ 0.1C_b	300	ns
Fall time of SDAA0 and SCLA0 signals	t_F			300	2.0+ 0.1C_b	300	ns
Total load capacitance value of each communication line (SCLA0, SDAA0)	C_b			400		400	pF

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

3. The data hold time differs depending on the setting of the IICA low-level width setting register (IICWL).

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.5[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.