Renesas Electronics America Inc - UPD78F0573MC-CAB-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0573mc-cab-ax

○ Timer

- 16-bit timer/event counter … PPG output, capture input, external event counter input
- 8-bit timer H … PWM output
- 8-bit timer/event counter 5 … PWM output, external event counter input
- Watchdog timer … Operable with low-speed internal oscillation clock
- Real-time counter … Available to count up in year, month, week, day, hour, minute, and second units

Item / Products	16-bit timer/event counter	8-bit timer	Watchdog timer	Real-time counter
78K0/KY2-L (16 pins)	1 ch	Timer H: 1 ch Timer 5: 1 ch	1 ch	–
78K0/KA2-L (20 pins)				
<R> 78K0/KA2-L (25 pins)				
<R> 78K0/KA2-L (32 pins)				
78K0/KB2-L (30 pins)		Timer H: 2 ch Timer 5: 2 ch		
<R> 78K0/KC2-L (40 pins)				1 ch
78K0/KC2-L (44 pins)				
78K0/KC2-L (48 pins)				

○ Serial interface

- UART … Asynchronous 2-wire serial interface
- IICA … Clock synchronous 2-wire serial interface, multimaster supported, standby can be released upon address match in slave mode
- CSI … Clock synchronous 3-wire serial interface

Item / Products	UART	IIC	CSI
78K0/KY2-L (16 pins)	1 ch	1 ch	–
78K0/KA2-L (20 pins)			
<R> 78K0/KA2-L (25 pins)			1 ch (CSI11[Note])
<R> 78K0/KA2-L (32 pins)			
78K0/KB2-L (30 pins)			1 ch (CSI10)
<R> 78K0/KC2-L (40 pins)			2 ch (CSI10, CSI11)
78K0/KC2-L (44 pins)			
78K0/KC2-L (48 pins)			2 ch (CSI10, CSI11[Note])

Note Can control by an enabled signal, when using CSI11 in the slave mode.

○ 10-bit resolution A/D conversion

- 78K0/KY2-L: 4 ch
- <R> 78K0/KA2-L (20 pins): 6 ch, 78K0/KA2-L (25 pins): 7 ch
  <R> 78K0/KA2-L (32 pins): 11 ch
- 78K0/KB2-L: 7 ch
- <R> 78K0/KC2-L (40 pins): 10 ch, 78K0/KC2-L (44 pins, 48 pins): 11 ch

○ Operational amplifier (products with operational amplifier only)

- 78K0/KY2-L, 78K0/KA2-L: 1 ch
- 78K0/KB2-L, 78K0/KC2-L: 2 ch

<R> **(3) Port functions: 78K0/KA2-L (25, 32 pins)**

Function Name	I/O	Function	After Reset	Alternate Function
P00[Note 1]	I/O	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000[Note 1]/INTP0[Note 1] (/TOH1)[Note 1] (/TI51)[Note 1]
P01[Note 2]				TO00[Note 2]/TI010[Note 2]
P02				$\overline{\text{SSI11}}$/INTP5
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0/AMP0-[Note 3]
P21				ANI1/AMP0OUT[Note 3]/ PGAIN[Note 3]
P22				ANI2/AMP0+[Note 3]
P23				ANI3
P24				ANI4
P25				ANI5
P26				ANI6
P27[Note 2]				ANI7[Note 2]
P31	I/O	Port 3. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP2/TOOLC1
P32				INTP3/TOOLD1
P33				–
P34				INTP4(/TOH1) (/TI51)[Note 1]
P35				$\overline{\text{SCK11}}$
P36				SI11
P37				SO11
P60	I/O	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Input can be set to SMBus input buffer in 1-bit units. Output can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TxD6/SCLA0
P61				RxD6/SDAA0
P70[Note 2]	I/O	Port 7. 3-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI8[Note 2]
P71[Note 2]				ANI9[Note 2]
P72[Note 2]				ANI10[Note 2]
P121	Input	Port 12. 3-bit I/O port. For only P125, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	X1/TOOLC0 (/TI000)(/INTP0)
P122				X2/EXCLK/ TOOLD0
P125			Reset input	$\overline{\text{RESET}}$(/TI000)[Note 2] (/INTP0)[Note 2]

Notes 1. 25-pin products only

2. 32-pin products only

3. μPD78F0565, 78F0566, and 78F0567 (products with operational amplifier) only

3.4.5 Special function register (SFR) addressing

[Function]

A memory-mapped special function register (SFR) is addressed with 8-bit immediate data in an instruction word.
This addressing is applied to the 240-byte spaces FF00H to FFCFH and FFE0H to FFFFH. However, the SFRs mapped at FF00H to FF1FH can be accessed with short direct addressing.

[Operand format]

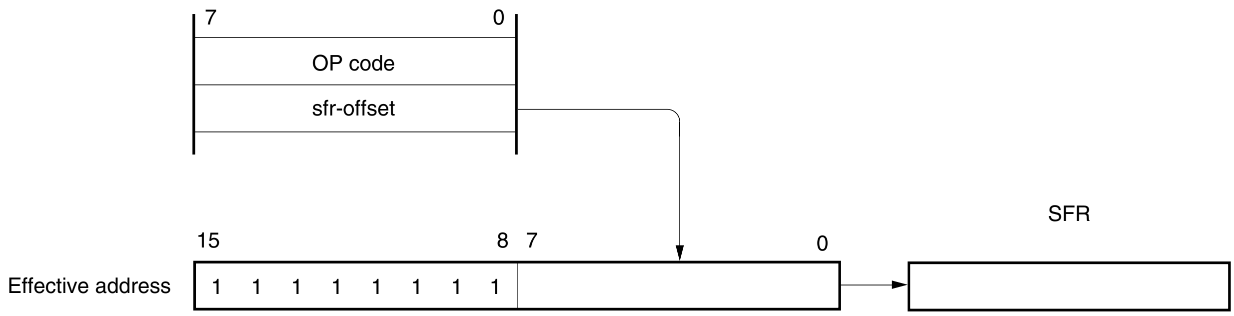
Identifier	Description
sfr	Special function register name
sfrp	16-bit manipulatable special function register name (even address only)

[Description example]

MOV PM0, A; when selecting PM0 (FF20H) as sfr

Operation code	1 1 1 1 0 1 1 0	OP code
	0 0 1 0 0 0 0 0	20H (sfr-offset)

[Illustration]



4.2.5 Port 4

<R>

78K0/KY2-L (μPD78F057x)	78K0/KA2-L (μPD78F056x)	78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)		
16 Pins	20, 25, 32 Pins	30 Pins	40 Pins	44 Pins	48 Pins
−	−	−	−	P40/RTCCL/ RTCDIV(/$\overline{\text{SCK11}}$)	P40/RTCCL/ RTCDIV(/$\overline{\text{SCK11}}$)
−	−	−	−	P41/RTC1HZ (/SI11)	P41/RTC1HZ (/SI11)
−	−	−	−	−	P42/PCL/$\overline{\text{SSI11}}$/ INTP6

Remark Functions in parentheses ( ) can be assigned by setting the port alternate switch control register (MUXSEL).

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P42 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 4 (PU4).

This port can also be used for external interrupt request input, real-time counter clock output, real-time counter correction clock output, and chip select input of serial interface.

The clock I/O and data input of the serial interface can be assigned to P40 and P41 of the 78K0/KC2-L (44-pin and 48-pin products) respectively by setting the port alternate switch control register (MUXSEL).

Reset signal generation sets port 4 to input mode.

Figures 4-19 to 4-21 show block diagrams of port 4.

<R> **Table 4-16. Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KA2-L (25-pin and 32-pin product)) (1/2)**

Pin Name	Alternate Function		MUXSEL	PMxx	Pxx
	Function Name	I/O			
P00[Note 1]	TI000[Note 1]	Input	TM00SEL0 = 0	1	×
	INTP0[Note 1]	Input	INTP0SEL0 = 0	1	×
	(TOH1)[Note 1]	Output	TMHSEL1, TMHSEL0 = 1, 0	0	0
	(TI51)[Note 1]	Input	TM5SEL1, TM5SEL0 = 1, 0	1	×
P01[Note 2]	TI010[Note 2]	Input	–	1	×
	TO00[Note 2]	Output	–	0	0
P20	ANI0[Note 3]	Input	–	1	×
	AMP0-[Notes 3, 4]	Input	–	1	×
P21	ANI1[Note 3]	Input	–	1	×
	AMP0OUT[Notes 3, 4]	Output	–	1	×
	PGAIN[Notes 3, 4]	Input	–	1	×
P22	ANI2[Note 3]	Input	–	1	×
	AMP0+[Notes 3, 4]	Input	–	1	×
P23 to P26	ANI3 to ANI6[Note 3]	Input	–	1	×
P27[Note 2]	ANI7[Notes 2, 3]	Input	–	1	×
P31	INTP2	Input	–	1	×
	TOOLC1	Input	–	×	×
P32	INTP3	Input	–	1	×
	TOOLD1	Input	–	×	×
P34	INTP4	I/O	–	1	×
	(TOH1)	Output	TMHSEL1[Note 1], TMHSEL0 = 0, 1	0	0
	(TI51)[Note 1]	Input	TM5SEL1, TM5SEL0 = 0, 1	1	×
P35	$\overline{\text{SCK11}}$	Input	–	1	×
		Output	–	0	1
P36	SI11	Input	–	1	×
P37	SO11	Input	–	0	0

Notes 1. 25-pin products only
2. 32-pin products only
3. The pin function can be selected by using ADPC0 register, PM2 register, ADS register, OPAMP0E bit, and PGAIN bit. Refer to **Tables 4-10** to **4-12** of **4.2.3 Port 2**.
4. μPD78F0565, 78F0566, and 78F0567 (products with operational amplifier) only

Remarks 1. ×: Don't care
PMxx: Port mode register
Pxx: Port output latch
2. Functions in parentheses ( ) can be assigned by setting MUXSEL register.

CHAPTER 5 CLOCK GENERATOR

5.1 Functions of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.
The following three kinds of system clocks and clock oscillators are selectable.

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 1 to 10 MHz by connecting a resonator to X1 and X2.
Oscillation can be stopped by executing the STOP instruction or using the main OSC control register (MOC).

<2> Internal high-speed oscillator

This circuit oscillates a clock of f_{IH} = 4 MHz (TYP.)/8 MHz (TYP.). After a reset release, the CPU always starts operating with this internal high-speed oscillation clock. Oscillation can be stopped by executing the STOP instruction or using the internal oscillation mode register (RCM).

An external main system clock (f_{EXCLK} = 1 to 10 MHz) can also be supplied from the EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or using RCM.
As the main system clock, a high-speed system clock (X1 clock or external main system clock) or internal high-speed oscillation clock can be selected by using the main clock mode register (MCM).

(2) Subsystem clock[Note]

- **Subsystem clock oscillator**

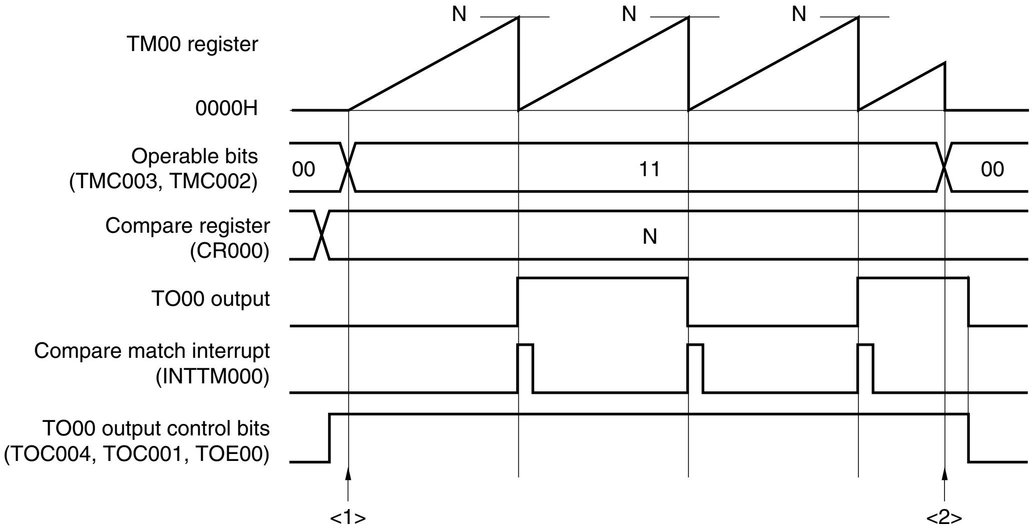
  This circuit oscillates at a frequency of f_{XT} = 32.768 kHz by connecting a 32.768 kHz resonator across XT1 and XT2. Oscillation can be stopped by using the processor clock control register (PCC) and clock operation mode select register (OSCCTL).

An external subsystem clock (f_{EXCLKS} = 32.768 kHz) can also be supplied from the EXCLKS/XT2/P124 pin. An external subsystem clock input can be disabled by setting PCC and OSCCTL.

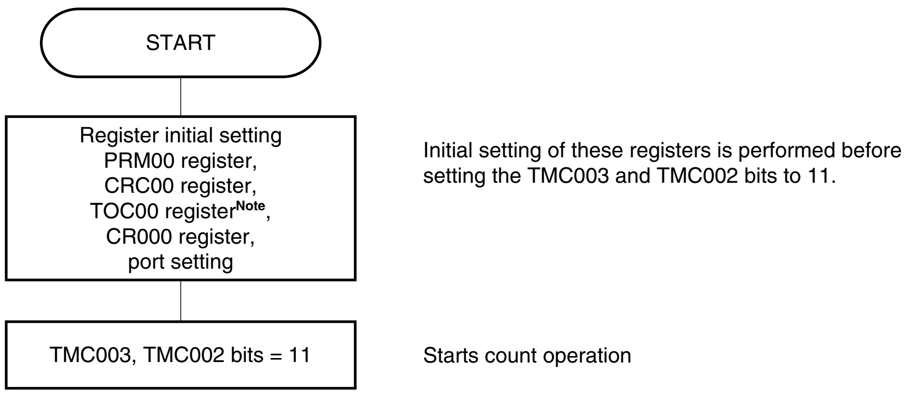
Note 78K0/KC2-L only

Remark f_X: X1 clock oscillation frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{EXCLK}: External main system clock frequency
f_{XT}: XT1 clock oscillation frequency
f_{EXCLKS}: External subsystem clock frequency

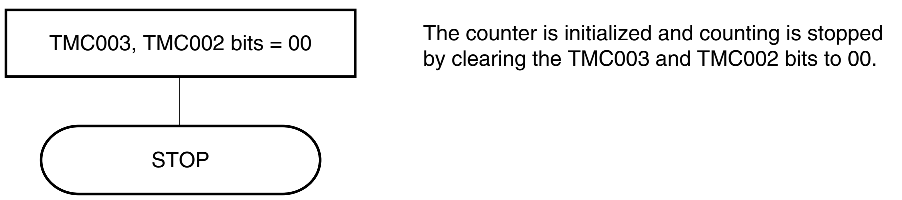
Figure 6-22. Example of Software Processing in External Event Counter Mode



<1> Count operation start flow



<2> Count operation stop flow



Note Care must be exercised when setting TOC00. For details, refer to **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

Figure 8-5. Format of 8-Bit Timer H Mode Register 0 (TMHMD0) (78K0/KB2-L, 78K0/KC2-L Only)

Address: FF69H After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD0	TMHE0	CKS02	CKS01	CKS00	TMMD01	TMMD00	TOLEV0	TOEN0

TMHE0	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS02	CKS01	CKS00	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	f_{PRS}	2 MHz	5 MHz	10 MHz
0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	0	0	$f_{PRS}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz
1	0	1	TM50 output[Note 2]			
Other than above			Setting prohibited			

TMMD01	TMMD00	Timer operation mode
0	0	Interval timer mode
1	0	PWM output mode
Other than above		Setting prohibited

TOLEV0	Timer output level control (in default mode)
0	Low level
1	High level

TOEN0	Timer output control
0	Disables output
1	Enables output

Note 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq 10$ MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq 5$ MHz

8.4.2 Operation as PWM output

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

The 8-bit timer compare register 0n (CMP0n) controls the cycle of timer output (TOHn). Rewriting the CMP0n register during timer operation is prohibited.

The 8-bit timer compare register 1n (CMP1n) controls the duty of timer output (TOHn). Rewriting the CMP1n register during timer operation is possible.

The operation in PWM output mode is as follows.

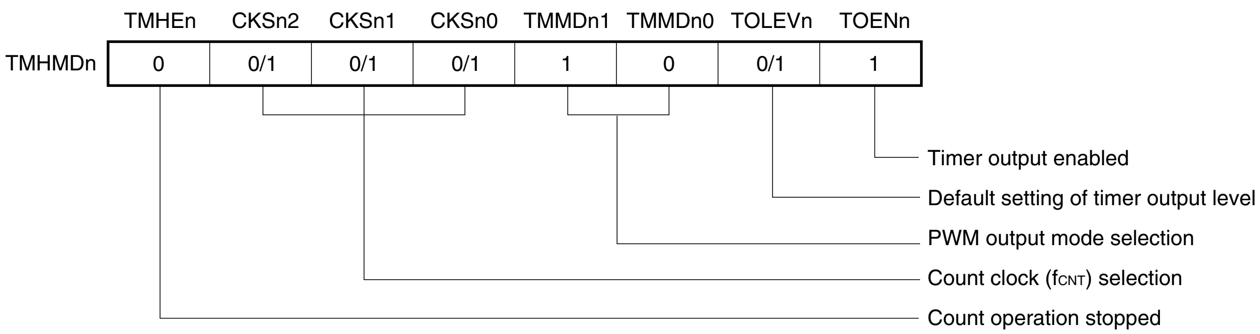
PWM output (TOHn output) outputs an active level and 8-bit timer counter Hn is cleared to 0 when 8-bit timer counter Hn and the CMP0n register match after the timer count is started. PWM output (TOHn output) outputs an inactive level when 8-bit timer counter Hn and the CMP1n register match.

Setting

<1> Set each register.

Figure 8-14. Register Setting in PWM Output Mode

(i) Setting timer H mode register n (TMHMDn)



(ii) Setting CMP0n register

- Compare value (N): Cycle setting

(iii) Setting CMP1n register

- Compare value (M): Duty setting

Remarks 1. 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

2. 00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

<2> The count operation starts when TMHEn = 1.

<3> The CMP0n register is the compare register that is to be compared first after counter operation is enabled. When the values of the 8-bit timer counter Hn and the CMP0n register match, the 8-bit timer counter Hn is cleared, an interrupt request signal (INTTMHn) is generated, and an active level is output. At the same time, the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP0n register to the CMP1n register.

<4> When the 8-bit timer counter Hn and the CMP1n register match, an inactive level is output and the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP1n register to the CMP0n register. At this time, the 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

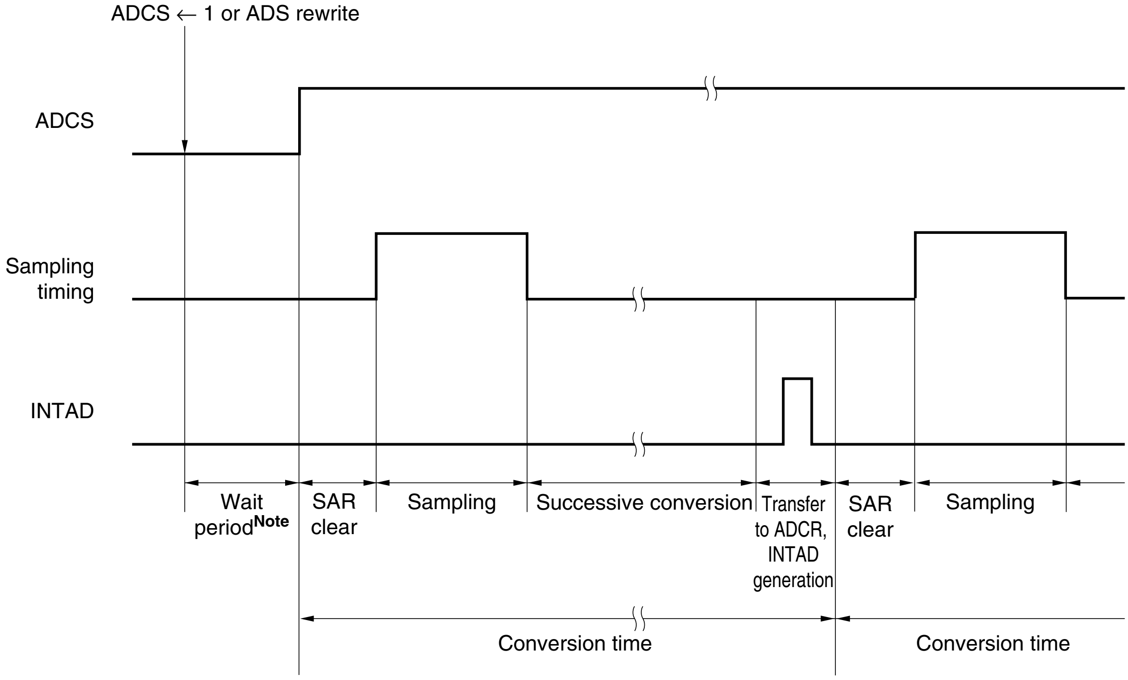
Remark If the overflow time is set to $2^{17}/f_{IL}$, the window close time and open time are as follows.

	Setting of Window Open Period			
	25%	50%	75%	100%
Window close time	0 to 3.64 s	0 to 2.43 s	0 to 1.21 s	None
Window open time	3.64 to 3.97 s	2.43 to 3.97 s	1.21 to 3.97 s	0 to 3.97 s

<When window open period is 25%>

- Overflow time:
  $2^{17}/f_{IL}$ (MAX.) = 2^{17}/33 kHz (MAX.) = 3.97 s
- Window close time:
  0 to $2^{17}/f_{IL}$ (MIN.) × (1 − 0.25) = 0 to 2^{17}/27 kHz (MIN.) × 0.75 = 0 to 3.64 s
- Window open time:
  $2^{17}/f_{IL}$ (MIN.) × (1 − 0.25) to $2^{17}/f_{IL}$ (MAX.) = $2^{17}/f_{IL}$ /27 kHz (MIN.) × 0.75 to 2^{17}/33 kHz (MAX.) = 3.64 to 3.97 s

Figure 12-4. A/D Converter Sampling and A/D Conversion Timing



Note For details of wait period, refer to **CHAPTER 31 CAUTIONS FOR WAIT**.

(2) 10-bit A/D conversion result register (ADCR)

This register is a 16-bit register that stores the A/D conversion result. The higher 6 bits are fixed to 0. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register. The higher 2 bits of the conversion result are stored in FF09H and the lower 8 bits of the conversion result are stored in FF08H.

ADCR can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 12-5. Format of 10-Bit A/D Conversion Result Register (ADCR)

Address: FF08H, FF09H After reset: 0000H R

Symbol	FF09H								FF08H							
ADCR	0	0	0	0	0	0										

Cautions 1. When writing to the A/D converter mode register 0 (ADM0), analog input channel specification register (ADS), and A/D port configuration registers 0, 1 (ADPC0, ADPC1), the contents of ADCR may become undefined. Read the conversion result following conversion completion before writing to ADM0, ADS, ADPC0, and ADPC1. Using timing other than the above may cause an incorrect conversion result to be read.

2. If data is read from ADCR, a wait cycle is generated. Do not read data from ADCR when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 31 CAUTIONS FOR WAIT.

CHAPTER 14 SERIAL INTERFACE UART6

14.1 Functions of Serial Interface UART6

Serial interface UART6 are mounted onto all 78K0/Kx2-L microcontroller products.
Serial interface UART6 has the following two modes.

(1) Operation stop mode

This mode is used when serial communication is not executed and can enable a reduction in the power consumption.
For details, refer to **14.4.1 Operation stop mode**.

(2) Asynchronous serial interface (UART) mode

This mode supports the LIN (Local Interconnect Network)-bus. The functions of this mode are outlined below.
For details, refer to **14.4.2 Asynchronous serial interface (UART) mode** and **14.4.3 Dedicated baud rate generator**.

- Maximum transfer rate: 625 kbps
- Two-pin configuration TxD6: Transmit data output pin
  RxD6: Receive data input pin
- Data length of communication data can be selected from 7 or 8 bits.
- Dedicated internal 8-bit baud rate generator allowing any baud rate to be set
- Transmission and reception can be performed independently (full duplex operation).
- MSB- or LSB-first communication selectable
- Inverted transmission operation
- Sync break field transmission from 13 to 20 bits
- More than 11 bits can be identified for sync break field reception (SBF reception flag provided).

Cautions 1. The TxD6 output inversion function inverts only the transmission side and not the reception side. To use this function, the reception side must be ready for reception of inverted data.

2. If clock supply to serial interface UART6 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART6 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD6 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER6 = 0, RXE6 = 0, and TXE6 = 0.

3. Set POWER6 = 1 and then set TXE6 = 1 (transmission) or RXE6 = 1 (reception) to start communication.

4. TXE6 and RXE6 are synchronized by the base clock (f_{XCLK6}) set by CKSR6. To enable transmission or reception again, set TXE6 or RXE6 to 1 at least two clocks of the base clock after TXE6 or RXE6 has been cleared to 0. If TXE6 or RXE6 is set within two clocks of the base clock, the transmission circuit or reception circuit may not be initialized.

5. Set transmit data to TXB6 at least one base clock (f_{XCLK6}) after setting TXE6 = 1.

6. If data is continuously transmitted, the communication timing from the stop bit to the next start bit is extended two operating clocks of the macro. However, this does not affect the result of communication because the reception side initializes the timing when it has detected a start bit. Do not use the continuous transmission function if the interface is used in LIN communication operation.

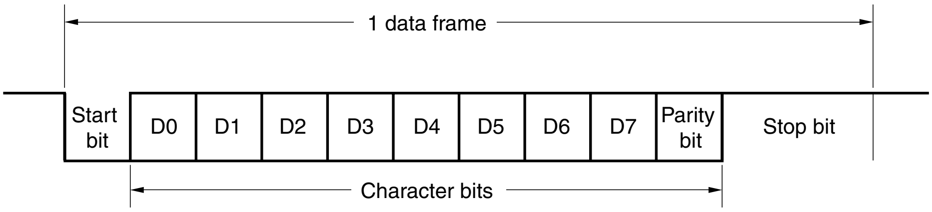
(2) Communication operation

(a) Format and waveform example of normal transmit/receive data

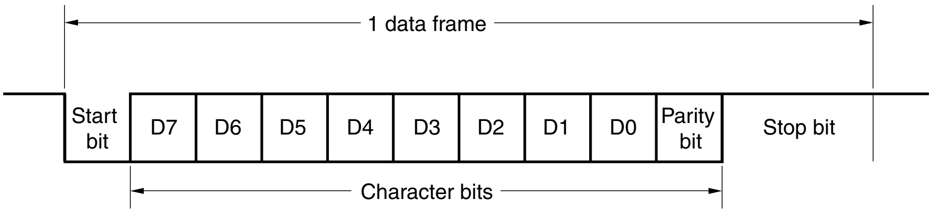
Figures 14-15 and 14-16 show the format and waveform example of the normal transmit/receive data.

Figure 14-15. Format of Normal UART Transmit/Receive Data

1. LSB-first transmission/reception



2. MSB-first transmission/reception



One data frame consists of the following bits.

- Start bit ... 1 bit
- Character bits ... 7 or 8 bits
- Parity bit ... Even parity, odd parity, 0 parity, or no parity
- Stop bit ... 1 or 2 bits

The character bit length, parity, and stop bit length in one data frame are specified by asynchronous serial interface operation mode register 6 (ASIM6).

Whether data is communicated with the LSB or MSB first is specified by bit 1 (DIR6) of asynchronous serial interface control register 6 (ASICL6).

Whether the TxD6 pin outputs normal or inverted data is specified by bit 0 (TXDLV6) of ASICL6.

(i) SBF reception

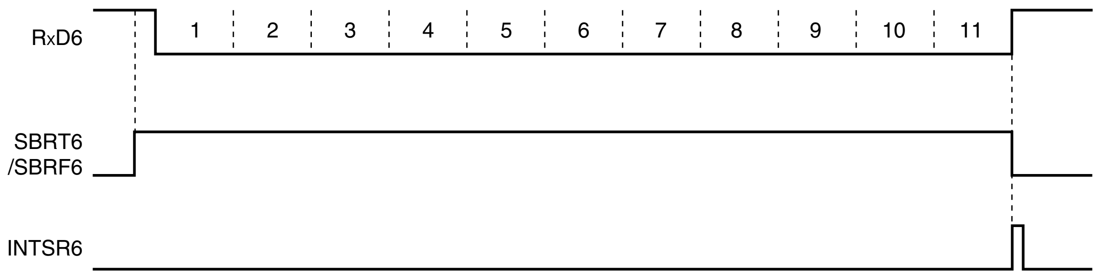
When the device is used in LIN communication operation, the SBF (Synchronous Break Field) reception control function is used for reception. For the reception operation of LIN, refer to **Figure 14-2 LIN Reception Operation**.

Reception is enabled when bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and then bit 5 (RXE6) of ASIM6 is set to 1. SBF reception is enabled when bit 6 (SBRT6) of asynchronous serial interface control register 6 (ASICL6) is set to 1. In the SBF reception enabled status, the RxD6 pin is sampled and the start bit is detected in the same manner as the normal reception enable status.

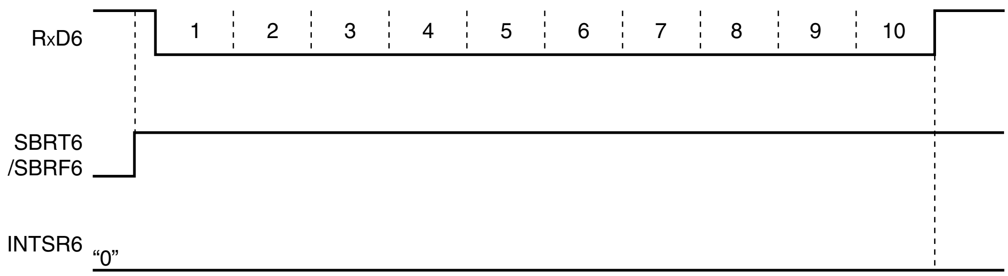
When the start bit has been detected, reception is started, and serial data is sequentially stored in the receive shift register 6 (RXS6) at the set baud rate. When the stop bit is received and if the width of SBF is 11 bits or more, a reception completion interrupt request (INTSR6) is generated as normal processing. At this time, the SBRF6 and SBRT6 bits are automatically cleared, and SBF reception ends. Detection of errors, such as OVE6, PE6, and FE6 (bits 0 to 2 of asynchronous serial interface reception error status register 6 (ASIS6)) is suppressed, and error detection processing of UART communication is not performed. In addition, data transfer between receive shift register 6 (RXS6) and receive buffer register 6 (RXB6) is not performed, and the reset value of FFH is retained. If the width of SBF is 10 bits or less, an interrupt does not occur as error processing after the stop bit has been received, and the SBF reception mode is restored. In this case, the SBRF6 and SBRT6 bits are not cleared.

Figure 14-25. SBF Reception

1. Normal SBF reception (stop bit is detected with a width of more than 10.5 bits)



2. SBF reception error (stop bit is detected with a width of 10.5 bits or less)

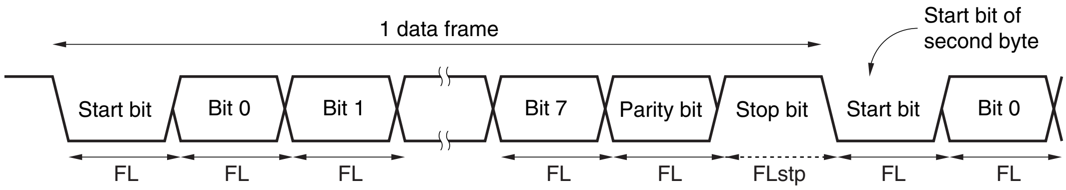


Remark RxD6: RxD6 pin (input)
SBRT6: Bit 6 of asynchronous serial interface control register 6 (ASICL6)
SBRF6: Bit 7 of ASICL6
INTSR6: Reception completion interrupt request

(5) Data frame length during continuous transmission

When data is continuously transmitted, the data frame length from a stop bit to the next start bit is extended by two clocks of base clock from the normal value. However, the result of communication is not affected because the timing is initialized on the reception side when the start bit is detected.

Figure 14-28. Data Frame Length During Continuous Transmission



Where the 1-bit data length is FL, the stop bit length is FLstp, and base clock frequency is f_{XCLK6}, the following expression is satisfied.

$FLstp = FL + 2/f_{XCLK6}$

Therefore, the data frame length during continuous transmission is:

$\text{Data frame length} = 11 \times FL + 2/f_{XCLK6}$

(c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

(i) When WTIM0 = 0

SPT0 = 1
↓

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 ▲4 △5

▲1: IICAS0 = 1010×110B
▲2: IICAS0 = 1010×000B
▲3: IICAS0 = 1010×000B (Sets WTIM0 to 1)[Note]
▲4: IICAS0 = 1010××00B (Sets SPT0 to 1)
△5: IICAS0 = 00000001B

Note To generate a stop condition, set WTIM0 to 1 and change the timing for generating the INTIICA0 interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don’t care

(ii) When WTIM0 = 1

SPT0 = 1
↓

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 △4

▲1: IICAS0 = 1010×110B
▲2: IICAS0 = 1010×100B
▲3: IICAS0 = 1010××00B (Sets SPT0 to 1)
△4: IICAS0 = 00001001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don’t care

Table 16-2. Relationship Between Register Settings and Pins (3/4)

(c) Serial interface CSI11 (CSISEL = 1) (78K0/KC2-L)

CSIE11	TRMD11	SSE11	PM41	P41	PM 120	P120	PM40	P40	PM42	P42	CSI11 Operation	Pin Function			
												SI11/P41/ RTC1HZ	SO11/ P120/ EXLVI/ INTP0	$\overline{\text{SCK11}}$/ P40/ RTCCL/ RTCDIV	$\overline{\text{SSI11}}$/ P42/PCL/ INTP6
0	0	×	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	Stop	P41/ RTC1HZ	P120/ EXLVI/ INTP0	P40/ RTCCL/ RTCDIV Note 2	P42/ PCL/ INTP6
1	0	0	1	×	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	1	×	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	Slave reception$^{\text{Note 3}}$	SI11	P120/ EXLVI/ INTP0	$\overline{\text{SCK11}}$ (input) Note 3	P42/ PCL/ INTP6
		1							1	×					$\overline{\text{SSI11}}$
1	1	0	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	0	0	1	×	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	Slave transmission Note 3	P41/ RTC1HZ	SO11	$\overline{\text{SCK11}}$ (input) Note 3	P42/ PCL/ INTP6
		1							1	×					$\overline{\text{SSI11}}$
1	1	0	1	×	0	0	1	×	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	Slave transmission/ reception$^{\text{Note 3}}$	SI11	SO11	$\overline{\text{SCK11}}$ (input) Note 3	P42/ PCL/ INTP6
		1							1	×					$\overline{\text{SSI11}}$
1	0	0	1	×	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	0	1	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	Master reception	SI11	P120/ EXLVI/ INTP0	$\overline{\text{SCK11}}$ (output)	P42/ PCL/ INTP6
1	1	0	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	0	0	0	1	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	Master transmission	P41/ RTC1HZ	SO11	$\overline{\text{SCK11}}$ (output)	P42/ PCL/ INTP6
1	1	0	1	×	0	0	0	1	×$^{\text{Note 1}}$	×$^{\text{Note 1}}$	Master transmission/ reception	SI11	SO11	$\overline{\text{SCK11}}$ (output)	P42/ PCL/ INTP6

Notes 1. Can be set as port function.

2. To use P40/$\overline{\text{SCK11}}$/RTCCL/RTCDIV as port pins, clear CKP11 to 0.

3. To use the slave mode, set CKS112, CKS111, and CKS110 to 1, 1, 1.

Remarks 1.

×:	don't care
CSIE11:	Bit 7 of serial operation mode register 11 (CSIM11)
TRMD11:	Bit 6 of CSIM11
CKP11:	Bit 4 of serial clock selection register 11 (CSIC11)
CKS112, CKS111, CKS110:	Bits 2 to 0 of CSIC11
PM×:	Port mode register
P×:	Port output latch

2. The $\overline{\text{SSI11}}$ pin is available only in 48-pin products of 78K0/KC2-L.

Figure 17-14. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (44-pin products of 78K0/KC2-L)

Address: FFE4H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	SREMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK

Address: FFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK010	TMMK000	TMMK50	TMMKH0	TMMKH1	CSIMK10	STMK6	SRMK6

Address: FFE6H After reset: FFH R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
MK1L	PMK8	1	RTCMK	KRMK	TMMK51	RTCIMK	1	ADMK

Address: FFE7H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
MK1H	1	1	1	PMK11	PMK10	PMK9	CSIMK11	IICAMK0

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution Be sure to set bits 1 and 6 of MK1L, and bits 5 to 7 of MK1H to 1.

Figure 17-23. Format of External Interrupt Rising Edge Enable Registers (EGPCTL0, EGPCTL1) and External Interrupt Falling Edge Enable Registers (EGNCTL0, EGNCTL1) (4/5)

(f) 44-pin products of 78K0/KC2-L

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGPCTL0	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGNCTL0	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

Address: FF4AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGPCTL1	0	0	0	0	EGP11	EGP10	EGP9	EGP8

Address: FF4BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGNCTL1	0	0	0	0	EGN11	EGN10	EGP9	EGP8

EGPn	EGNn	INTPn pin valid edge selection
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Caution Be sure to clear bits 6 and 7 of EGPCTL0 and EGNCTL0, and bits 4 to 7 of EGPCTL1 and EGNCTL1 to 0 in the 44-pin products of 78K0/KC2-L.

Remark n = 0 to 5, 8 to 11: 44-pin products of 78K0/KC2-L

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
Conditional branch	**BT**	saddr.bit, $addr16	3	8	9	PC ← PC + 3 + jdisp8 if (saddr.bit) = 1	
		sfr.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if sfr.bit = 1	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 1	
		PSW.bit, $addr16	3	–	9	PC ← PC + 3 + jdisp8 if PSW.bit = 1	
		[HL].bit, $addr16	3	10	11	PC ← PC + 3 + jdisp8 if (HL).bit = 1	
	BF	saddr.bit, $addr16	4	10	11	PC ← PC + 4 + jdisp8 if (saddr.bit) = 0	
		sfr.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if sfr.bit = 0	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 0	
		PSW.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
		[HL].bit, $addr16	3	10	11	PC ← PC + 3 + jdisp8 if (HL).bit = 0	
	BTCLR	saddr.bit, $addr16	4	10	12	PC ← PC + 4 + jdisp8 if (saddr.bit) = 1 then reset (saddr.bit)	
		sfr.bit, $addr16	4	–	12	PC ← PC + 4 + jdisp8 if sfr.bit = 1 then reset sfr.bit	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 1 then reset A.bit	
		PSW.bit, $addr16	4	–	12	PC ← PC + 4 + jdisp8 if PSW.bit = 1 then reset PSW.bit	× × ×
		[HL].bit, $addr16	3	10	12	PC ← PC + 3 + jdisp8 if (HL).bit = 1 then reset (HL).bit	
	DBNZ	B, $addr16	2	6	–	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
		C, $addr16	2	6	–	C ← C –1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
		saddr, $addr16	3	8	10	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
CPU control	**SEL**	RBn	2	4	–	RBS1, 0 ← n	
	NOP		1	2	–	No Operation	
	EI		2	–	6	IE ← 1 (Enable Interrupt)	
	DI		2	–	6	IE ← 0 (Disable Interrupt)	
	HALT		2	6	–	Set HALT Mode	
	STOP		2	6	–	Set STOP Mode	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.