Renesas Electronics America Inc - UPD78F0577MC-CAB-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0577mc-cab-ax

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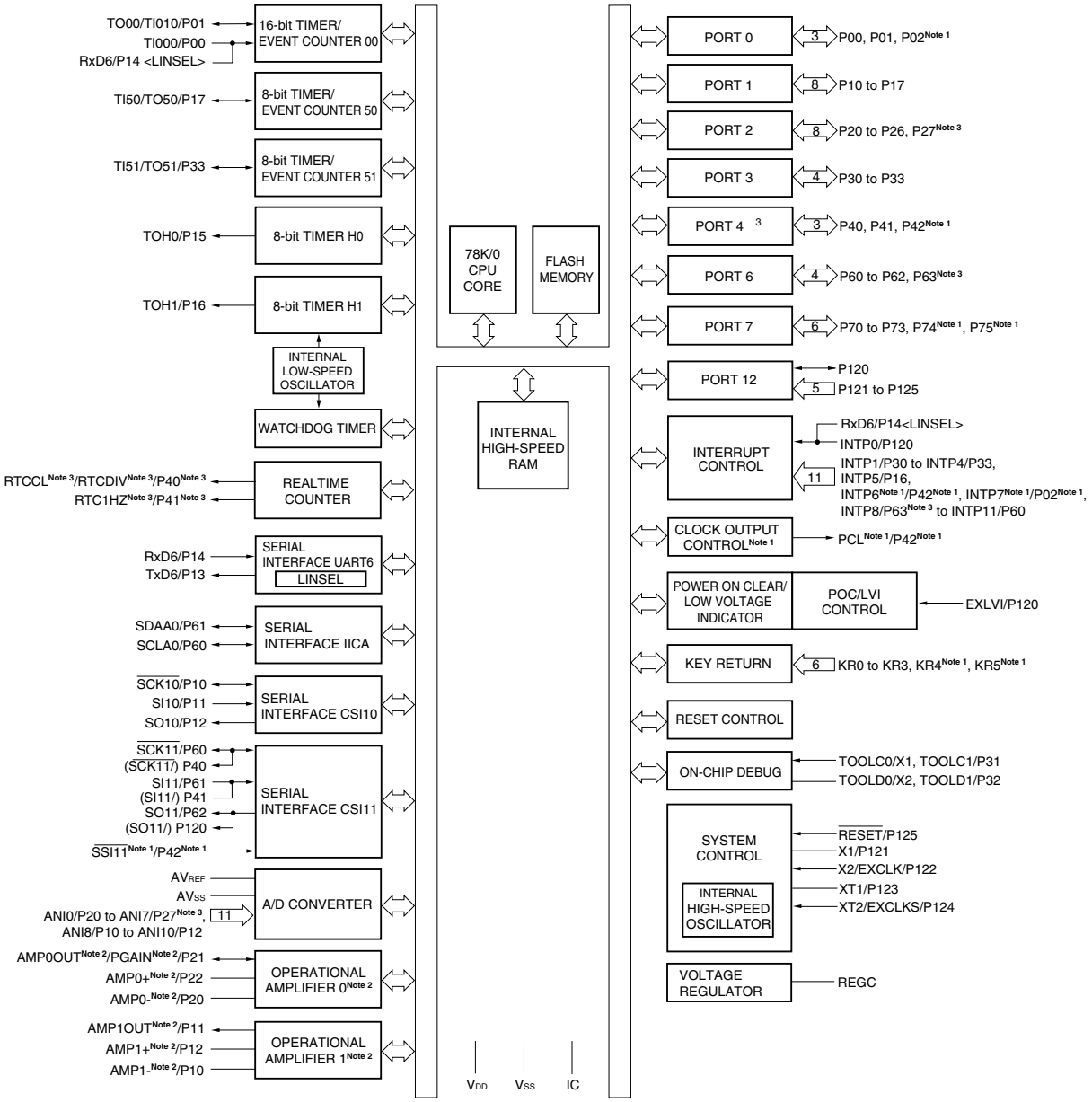


Notes 1. 48-pin products only

2. μPD78F0586, 78F0587, 78F0588 (products with operational amplifier) only

3. 44-pin and 48-pin products only

Cautions 1. Leave the IC (Internally Connected) pin open.

2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

3. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, and ANI3/P23 to ANI7/P27 are set in the analog input mode, P10/ANI8/AMP1-/SCK10, P11/ANI9/AMP1OUT/SI10, and P12/ANI10/AMP1+/SO10 are set in the digital input mode after release of reset.

4. RESET/P125 immediately after release of reset is set in the external reset input.

5. For 40-pin products, set P40, P41, and P63 to output mode (PM40 = PM41 = PM63 = 0) by using software after release of reset.

Remark Functions in parentheses ( ) in the figure above can be assigned by setting the port alternate switch control register (MUXSEL).

(1) Port mode

P20 to P27 function as an I/O port. P20 to P27 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P27 function as A/D converter analog input, operational amplifier I/O, and PGA input.

(a) ANI0 to ANI7

These are A/D converter analog input pins. When using these pins as analog input pins, refer to **(5) ANI0/P20 to ANI7/P27 and ANI8/P10 to ANI10/P12** in **12.6 Cautions for A/D Converter**.

(b) AMP0+, AMP0-

These are operational amplifier 0 input pins.

(c) AMP0OUT

This is an operational amplifier 0 output pin.

(d) PGAIN

This is a PGA (Programmable gain amplifier) input pin.

Caution ANI0/P20 to ANI7/P27 are set in the analog input mode after release of reset.

2.2.4 P30 to P37 (port 3)

P30 to P37 function as an I/O port. These pins also function as pins for external interrupt request input, timer I/O, clock input and data I/O for flash memory programmer/on-chip debugger, and clock I/O and data I/O for serial interface.

The timer I/O can be assigned to P34 of the 78K0/KA2-L (25-pin and 32-pin products) by setting the port alternate switch control register (MUXSEL).

<R>

78K0/KY2-L (μPD78F055x)	78K0/KA2-L (μPD78F056x)			78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)		
16 Pins	20 Pins	25 Pins	32 Pins	30 Pins	40 Pins	44 Pins	48 Pins
P30/TOH1/ TI51/INTP1	P30/TOH1/ TI51/INTP1	–	–	P30/INTP1	P30/INTP1	P30/INTP1	P30/INTP1
–	P31/INTP2/ TOOLC1	P31/INTP2/ TOOLC1	P31/INTP2/ TOOLC1	P31/INTP2/ TOOLC1	P31/INTP2/ TOOLC1	P31/INTP2/ TOOLC1	P31/INTP2/ TOOLC1
–	P32/INTP3/ TOOLD1	P32/INTP3/ TOOLD1	P32/INTP3/ TOOLD1	P32/INTP3/ TOOLD1	P32/INTP3/ TOOLD1	P32/INTP3/ TOOLD1	P32/INTP3/ TOOLD1
–	–	P33	P33	P33/TI51/ TO51/INTP4	P33/TI51/ TO51/INTP4	P33/TI51/ TO51/INTP4	P33/TI51/ TO51/INTP4
–	–	P34/INTP4 (/TOH1) (/TI51)	P34/INTP4 (/TOH1)	–	–	–	–
–	–	P35/$\overline{\text{SCK11}}$	P35/$\overline{\text{SCK11}}$	–	–	–	–
–	–	P36/SI11	P36/SI11	–	–	–	–
–	–	P37/SO11	P37/SO11	–	–	–	–

<R> **Table 4-4. Port Functions (78K0/KA2-L (25-pin and 32-pin products))**

Function Name	I/O	Function	After Reset	Alternate Function
P00 Note 1	I/O	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000 Note 1/INTP0 Note 1 (/TOH1) Note 1 (/TI51) Note 1
P01 Note 2				TO00 Note 2/TI010 Note 2
P02				$\overline{SSI11}$/INTP5
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0/AMP0- Note 3
P21				ANI1/AMP0OUT Note 3/ PGAIN Note 3
P22				ANI2/AMP0+ Note 3
P23				ANI3
P24				ANI4
P25				ANI5
P26				ANI6
P27 Note 2				ANI7 Note 2
P31	I/O	Port 3. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP2/TOOLC1
P32				INTP3/TOOLD1
P33				–
P34				INTP4(/TOH1) (/TI51) Note 1
P35				$\overline{SCK11}$
P36				SI11
P37				SO11
P60	I/O	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Input can be set to SMBus input buffer in 1-bit units. Output can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TxD6/SCLA0
P61				RxD6/SDAA0
P70 Note 2	I/O	Port 7. 3-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI8 Note 2
P71 Note 2				ANI9 Note 2
P72 Note 2				ANI10 Note 2
P121	Input	Port 12. 3-bit I/O port. For only P125, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	X1/TOOLC0 (/TI000)(/INTP0)
P122				X2/EXCLK/ TOOLD0
P125			Reset input	$\overline{RESET}$(/TI000) Note 2 (/INTP0) Note 2

Notes 1. 25-pin products only

2. 32-pin products only

3. μPD78F0565, 78F0566, and 78F0567 (products with operational amplifier) only

Figure 5-6. Format of Processor Clock Control Register (PCC)
(78K0/KC2-L)

Address: FFFBH After reset: 01H R/W[Note 1]

Symbol	7	6	<5>	<4>	3	2	1	0
PCC	0	XTSTART[Note 2]	CLS	CSS	0	PCC2	PCC1	PCC0

CLS	CPU clock status
0	Main system clock
1	Subsystem clock

CSS	PCC2	PCC1	PCC0	CPU clock (f_{CPU}) selection
0	0	0	0	f_{XP}
	0	0	1	f_{XP}/2 (default)
	0	1	0	$f_{XP}/2^2$
	0	1	1	$f_{XP}/2^3$
	1	0	0	$f_{XP}/2^4$
1	0	0	0	f_{SUB}/2
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Other than above				Setting prohibited

Notes 1. Bit 5 is read-only.

2. XTSTART is used in combination with EXCLKS and OSCSELS (bits 5 and 4 of the clock operation mode select register (OSCCTL)). Refer to **(3) Setting of operation mode for subsystem clock pin**.

Cautions 1. Be sure to clear bits 3 and 7 to "0".

2. The peripheral hardware clock (f_{PRS}) is not divided when the division ratio of the PCC is set.

Remark f_{XP}: Main system clock oscillation frequency
f_{SUB}: Subsystem clock oscillation frequency

The fastest instruction can be executed in 2 clocks of the CPU clock in the 78K0/Kx2-L microcontrollers. Therefore, the relationship between the CPU clock (f_{CPU}) and the minimum instruction execution time is as shown in Table 5-2.

(3) Example of setting procedure when using the subsystem clock as the CPU clock

<1> Setting subsystem clock oscillation[Note]

(Refer to **5.6.3 (1) Example of setting procedure when oscillating the XT1 clock** and **(2) Example of setting procedure when using the external subsystem clock**.)

Note The setting of <1> is not necessary when while the subsystem clock is operating.

<2> Switching the CPU clock (PCC register)

When CSS is set to 1, the subsystem clock is supplied to the CPU.

CSS	PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
1	0	0	0	f_{SUB}
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
	Other than above			Setting prohibited

(4) Example of setting procedure when stopping the subsystem clock

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the subsystem clock.

When CLS = 1, the subsystem clock is supplied to the CPU, so change the CPU clock to a clock other than the subsystem clock.

CLS	MCS	CPU Clock Status
0	0	Internal high-speed oscillation clock
0	1	High-speed system clock
1	×	Subsystem clock

<2> Stopping the subsystem clock (OSCCTL register)

When OSCSELS is cleared to 0, XT1 oscillation is stopped (the input of the external clock is disabled).

Cautions 1. Be sure to confirm that CLS = 0 when clearing OSCSELS to 0. In addition, stop the watch timer if it is operating on the subsystem clock.

2. The subsystem clock oscillation cannot be stopped using the STOP instruction.

Table 5-6. CPU Clock Transition and SFR Register Setting Examples (2/4)

(4) CPU clock changing from internal high-speed oscillation clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL[Note]	MCM0
(B) → (C) (X1 clock)	0	1	0	Must be checked	1	1
(B) → (C) (external main system clock)	1	1	0	Must not be checked	1	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Note The value of this flag can be changed only once after a reset release. This setting is not necessary if it has already been set.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (refer to CHAPTER 28 ELECTRICAL SPECIFICATIONS).

(5) CPU clock changing from internal high-speed oscillation clock (B) to subsystem clock (D)[Note]

Note 78K0/KC2-L only

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	XTSTART	EXCLKS	OSCSELS	Waiting for Oscillation Stabilization	CSS
(B) → (D) (XT1 clock)	0	0	1	Necessary	1
	1	×	×		
(B) → (D) (external subsystem clock)	0	1	1	Unnecessary	1

Unnecessary if the CPU is operating with the subsystem clock

Remarks 1. (A) to (I) in Table 5-6 correspond to (A) to (I) in Figures 5-18 and 5-19.

2. EXCLK, OSCSEL, EXCLKS, OSCSELS: Bits 7 to 4 of the clock operation mode select register (OSCCTL)
MSTOP: Bit 7 of the main OSC control register (MOC)
XSEL, MCM0: Bits 2 and 0 of the main clock mode register (MCM)
XTSTART, CSS: Bits 6 and 4 of the processor clock control register (PCC)
×: Don't care

Figure 6-8. Format of 16-Bit Timer Output Control Register 00 (TOC00)

Address: FFBDH After reset: 00H R/W

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>
TOC00	0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00

OSPT00	One-shot pulse output trigger via software
0	–
1	One-shot pulse output
The value of this bit is always “0” when it is read. Do not set this bit to 1 in a mode other than the one-shot pulse output mode. If it is set to 1, TM00 is cleared and started.	

OSPE00	One-shot pulse output operation control
0	Successive pulse output
1	One-shot pulse output
One-shot pulse output operates correctly in the free-running timer mode or clear & start mode entered by TI000 pin valid edge input. The one-shot pulse cannot be output in the clear & start mode entered upon a match between TM00 and CR000.	

TOC004	TO00 output control on match between CR010 and TM00
0	Disables inversion operation
1	Enables inversion operation
The interrupt signal (INTTM010) is generated even when TOC004 = 0.	

LVS00	LVR00	Setting of TO00 output status
0	0	No change
0	1	Initial value of TO00 output is low level (TO00 output is cleared to 0).
1	0	Initial value of TO00 output is high level (TO00 output is set to 1).
1	1	Setting prohibited

- LVS00 and LVR00 can be used to set the initial value of the TO00 output level. If the initial value does not have to be set, leave LVS00 and LVR00 as 00.
- Be sure to set LVS00 and LVR00 when TOE00 = 1.
  LVS00, LVR00, and TOE00 being simultaneously set to 1 is prohibited.
- LVS00 and LVR00 are trigger bits. By setting these bits to 1, the initial value of the TO00 output level can be set. Even if these bits are cleared to 0, TO00 output is not affected.
- The values of LVS00 and LVR00 are always 0 when they are read.
- For how to set LVS00 and LVR00, refer to **6.5.2 Setting LVS00 and LVR00**.
- The actual TO00/TI010/P01 pin output is determined depending on PM01 and P01, besides TO00 output.

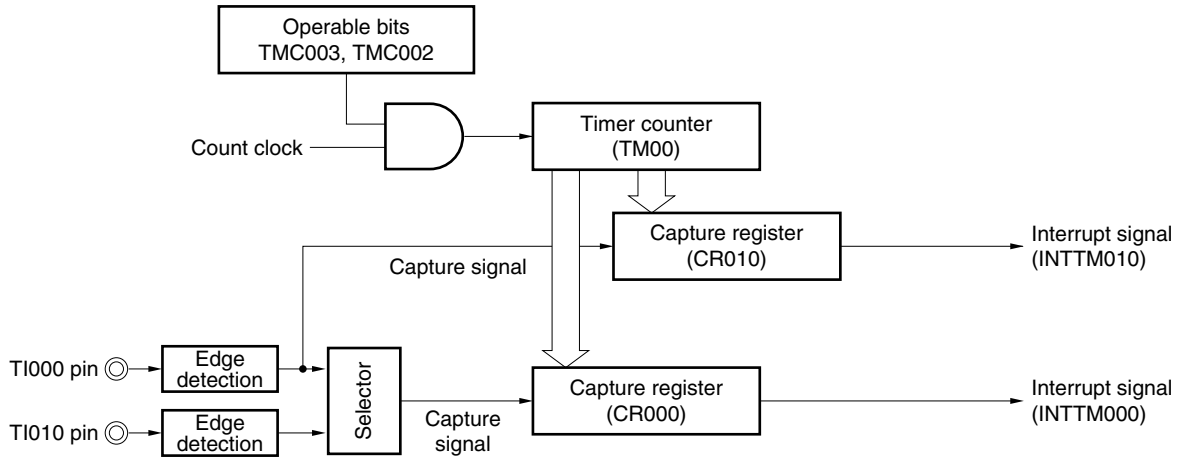
TOC001	TO00 output control on match between CR000 and TM00
0	Disables inversion operation
1	Enables inversion operation
The interrupt signal (INTTM000) is generated even when TOC001 = 0.	

TOE00	TO00 output control
0	Disables output (TO00 output fixed to low level)
1	Enables output

(3) Free-running timer mode operation

(CR000: capture register, CR010: capture register)

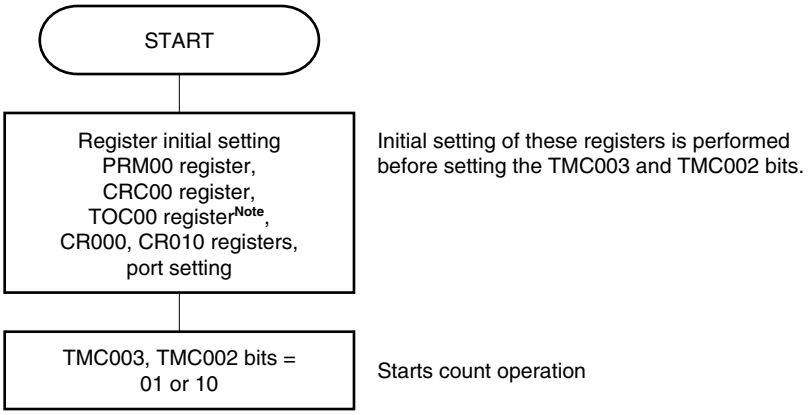
Figure 6-37. Block Diagram of Free-Running Timer Mode
(CR000: Capture Register, CR010: Capture Register)



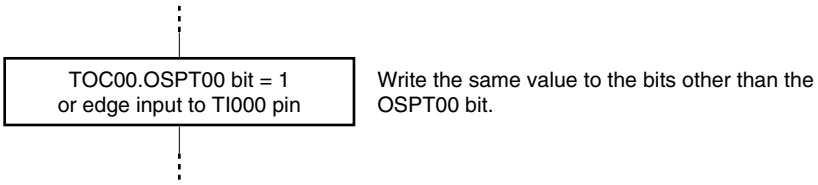
Remark If both CR000 and CR010 are used as capture registers in the free-running timer mode, the TO00 output level is not inverted.
However, it can be inverted each time the valid edge of the TI000 pin is detected if bit 1 (TMC001) of 16-bit timer mode control register 00 (TMC00) is set to 1.

Figure 6-46. Example of Software Processing for One-Shot Pulse Output Operation (2/2)

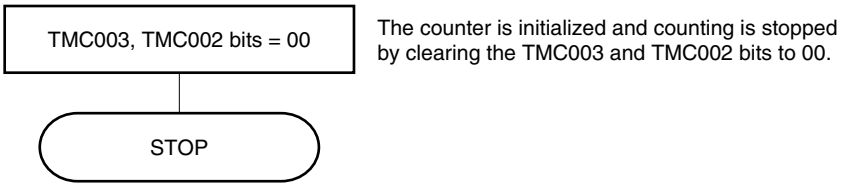
<1> Count operation start flow



<2> One-shot trigger input flow



<3> Count operation stop flow



Note Care must be exercised when setting TOC00. For details, refer to **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

6.6 Cautions for 16-Bit Timer/Event Counter 00

(1) Restrictions for each channel of 16-bit timer/event counter 00

Table 6-3 shows the restrictions for each channel.

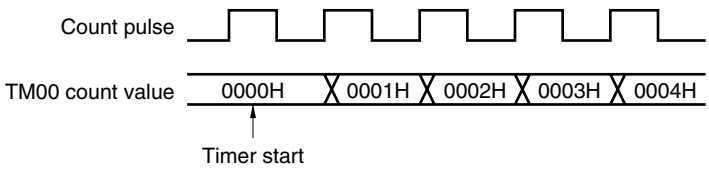
Table 6-3. Restrictions for Each Channel of 16-Bit Timer/Event Counter 00

Operation	Restriction
As interval timer	–
As square-wave output	
As external event counter	
As clear & start mode entered by TI000 pin valid edge input	Using timer output (TO00) is prohibited when detection of the valid edge of the TI010 pin is used. (TOC00 = 00H)
As free-running timer	–
As PPG output	0000H ≤ CP010 < CR000 ≤ FFFFH
As one-shot pulse output	Setting the same value to CR000 and CP010 is prohibited.
As pulse width measurement	Using timer output (TO00) is prohibited (TOC00 = 00H)

(2) Timer start errors

An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because counting TM00 is started asynchronously to the count pulse.

Figure 6-56. Start Timing of TM00 Count



(3) Setting of CR000 and CR010 (clear & start mode entered upon a match between TM00 and CR000)

Set a value other than 0000H to CR000 and CR010 (TM00 cannot count one pulse when it is used as an external event counter).

When using P10/ANI8/AMP1-, P11/ANI9/AMP1OUT, or P12/ANI10/AMP1+ in the 78K0/KB2-L and 78K0/KC2-L, set the registers according to the pin function to be used (refer to **Tables 12-3** and **12-4**).

Table 12-3. Setting Functions of P10/ANI8/AMP1-, P12/ANI10/AMP1+ Pins

ADPC1 Register	PM1 Register	OPAMP1E bit	ADS Register (n = 8, 10)	P10/ANI8/AMP1-, P12/ANI10/AMP1+ Pins
Analog input selection	Input mode	0	Selects ANIn.	Analog input (to be converted into digital signals)
			Does not select ANIn.	Analog input (not to be converted into digital signals)
		1	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Operational amplifier 1 input
	Output mode	–	–	Setting prohibited
Digital I/O selection	Input mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital input
	Output mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital output

Table 12-4. Setting Functions of P11/ANI9/AMP1OUT Pin

ADPC1 Register	PM1 Register	OPAMP1E bit	ADS Register	P11/ANI9/AMP1OUT Pin
Analog I/O selection	Input mode	0	Selects ANI9.	Analog input (to be converted into digital signals)
			Does not select ANI9.	Analog input (not to be converted into digital signals)
		1	Selects ANI9.	Operational amplifier 1 output (to be converted into digital signals)
			Does not select ANI9.	Operational amplifier 1 output (not to be converted into digital signals)
	Output mode	–	–	Setting prohibited
Digital I/O selection	Input mode	0	Selects ANI9.	Setting prohibited
			Does not select ANI9.	Digital input
		1	–	Setting prohibited
	Output mode	0	Selects ANI9.	Setting prohibited
			Does not select ANI9.	Digital output
		1	–	Setting prohibited

Remark ADPC1: A/D port configuration register 1
PM1: Port mode register 1
OPAMP1E: Bit 7 of operational amplifier 1 control register (AMP1M)
ADS: Analog input channel specification register

CHAPTER 15 SERIAL INTERFACE IICA

15.1 Functions of Serial Interface IICA

Serial interface IICA is mounted onto all 78K0/Kx2-L microcontroller products.
Serial interface IICA has the following three modes.

(1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

(2) I^2C bus mode (multimaster supported)

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLA0) line and a serial data bus (SDAA0) line.

This mode complies with the I^2C bus format and the master device can generated “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I^2C bus.

Since the SCLA0 and SDAA0 pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.

(3) Wakeup mode

The STOP mode can be released by generating an interrupt request signal (INTIICA0) when an extension code from the master device or a local address has been received while in STOP mode. This can be set by using the WUP bit of the IICA control register 1 (IICACTL1).

Figure 15-1 shows a block diagram of serial interface IICA.

Figure 15-4. Format of Slave Address Register 0 (SVA0)

Address: FFA6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SVA0								0[Note]

Note Bit 0 is fixed to 0.

(3) SO latch

The SO latch is used to retain the SDAA0 pin's output level.

(4) Wakeup controller

This circuit generates an interrupt request (INTIICA0) when the address received by this register matches the address value set to the slave address register 0 (SVA0) or when an extension code is received.

(5) Serial clock counter

This counter counts the serial clocks that are output or input during transmit/receive operations and is used to verify that 8-bit data was transmitted or received.

(6) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIICA0).

An I^2C interrupt request is generated by the following two triggers.

- Falling edge of eighth or ninth clock of the serial clock (set by WTIM0 bit)
- Interrupt request generated when a stop condition is detected (set by SPIE0 bit)

Remark WTIM0 bit: Bit 3 of IICA control register 0 (IICACTL0)
SPIE0 bit: Bit 4 of IICA control register 0 (IICACTL0)

(7) Serial clock controller

In master mode, this circuit generates the clock output via the SCLA0 pin from a sampling clock.

(8) Serial clock wait controller

This circuit controls the wait timing.

(9) ACK generator, stop condition detector, start condition detector, and ACK detector

These circuits generate and detect each status.

(10) Data hold time correction circuit

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

(11) Start condition generator

This circuit generates a start condition when the STT0 bit is set to 1.

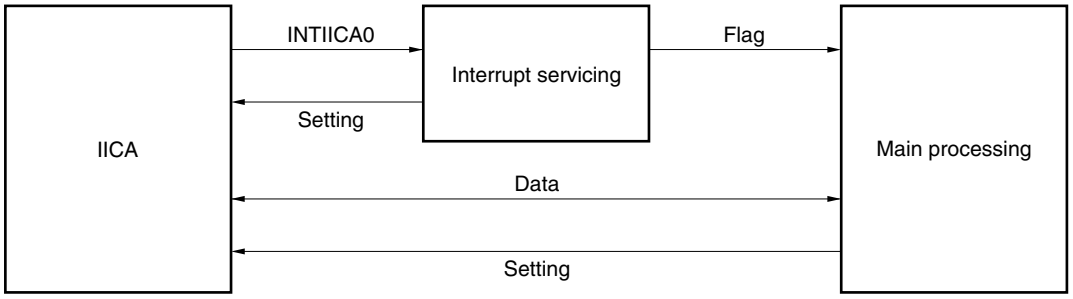
However, in the communication reservation disabled status (IICRSV bit = 1), when the bus is not released (IICBSY bit = 1), start condition requests are ignored and the STCF bit is set to 1.

(12) Stop condition generator

This circuit generates a stop condition when the SPT0 bit is set to 1.

Basically, the slave operation is event-driven. Therefore, processing by the INTIICA0 interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICA0 interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICA0.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

<2> Ready flag

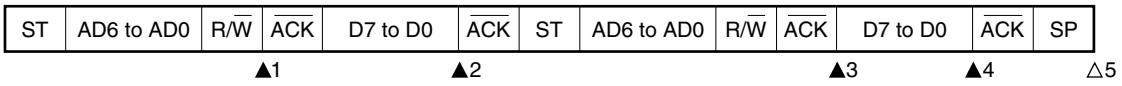
This flag indicates that data communication is enabled. Its function is the same as the INTIICA0 interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as the TRC0 bit.

(b) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

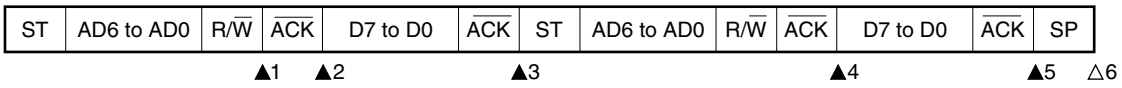
(i) When WTIM0 = 0 (after restart, matches SVA0)



▲1: IICAS0 = 0010×010B
▲2: IICAS0 = 0010×000B
▲3: IICAS0 = 0001×110B
▲4: IICAS0 = 0001×000B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, matches SVA0)



▲1: IICAS0 = 0010×010B
▲2: IICAS0 = 0010×110B
▲3: IICAS0 = 0010××00B
▲4: IICAS0 = 0001×110B
▲5: IICAS0 = 0001××00B
△6: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Cautions 1. To use the peripheral hardware that stops operation in the STOP mode, and the peripheral hardware for which the clock that stops oscillating in the STOP mode after the STOP mode is released, restart the peripheral hardware.

<R> **2. When transitioning to the STOP mode, it is possible to achieve low power consumption by setting RMC = 56H.**

3. Even if "internal low-speed oscillator can be stopped by software" is selected by the option byte, the internal low-speed oscillation clock continues in the STOP mode in the status before the STOP mode is set. To stop the internal low-speed oscillator's oscillation in the STOP mode, stop it by software and then execute the STOP instruction.

4. To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), switch the CPU clock to the internal high-speed oscillation clock before the execution of the STOP instruction using the following procedure.

<1> Set RSTOP to 0 (starting oscillation of the internal high-speed oscillator) → <2> Set MCM0 to 0 (switching the CPU from X1 oscillation to internal high-speed oscillation) → <3> Check that MCS is 0 (checking the CPU clock) → <4> Check that RSTS is 1 (checking internal high-speed oscillation operation) → <5> Execute the STOP instruction

Before changing the CPU clock from the internal high-speed oscillation clock to the high-speed system clock (X1 oscillation) after the STOP mode is released, check the oscillation stabilization time with the oscillation stabilization time counter status register (OSTC).

5. Execute the STOP instruction after having confirmed that the internal high-speed oscillator is operating stably (RSTS = 1).

CHAPTER 20 RESET FUNCTION

The reset function is mounted onto all 78K0/Kx2-L microcontroller products.

The following four operations are available to generate a reset signal.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
(4) Internal reset by comparison of supply voltage of the low-voltage detector (LVI) or input voltage from external input pin (EXLVI pin), and detection voltage

External and internal resets start program execution from the address at 0000H and 0001H when the reset signal is generated.

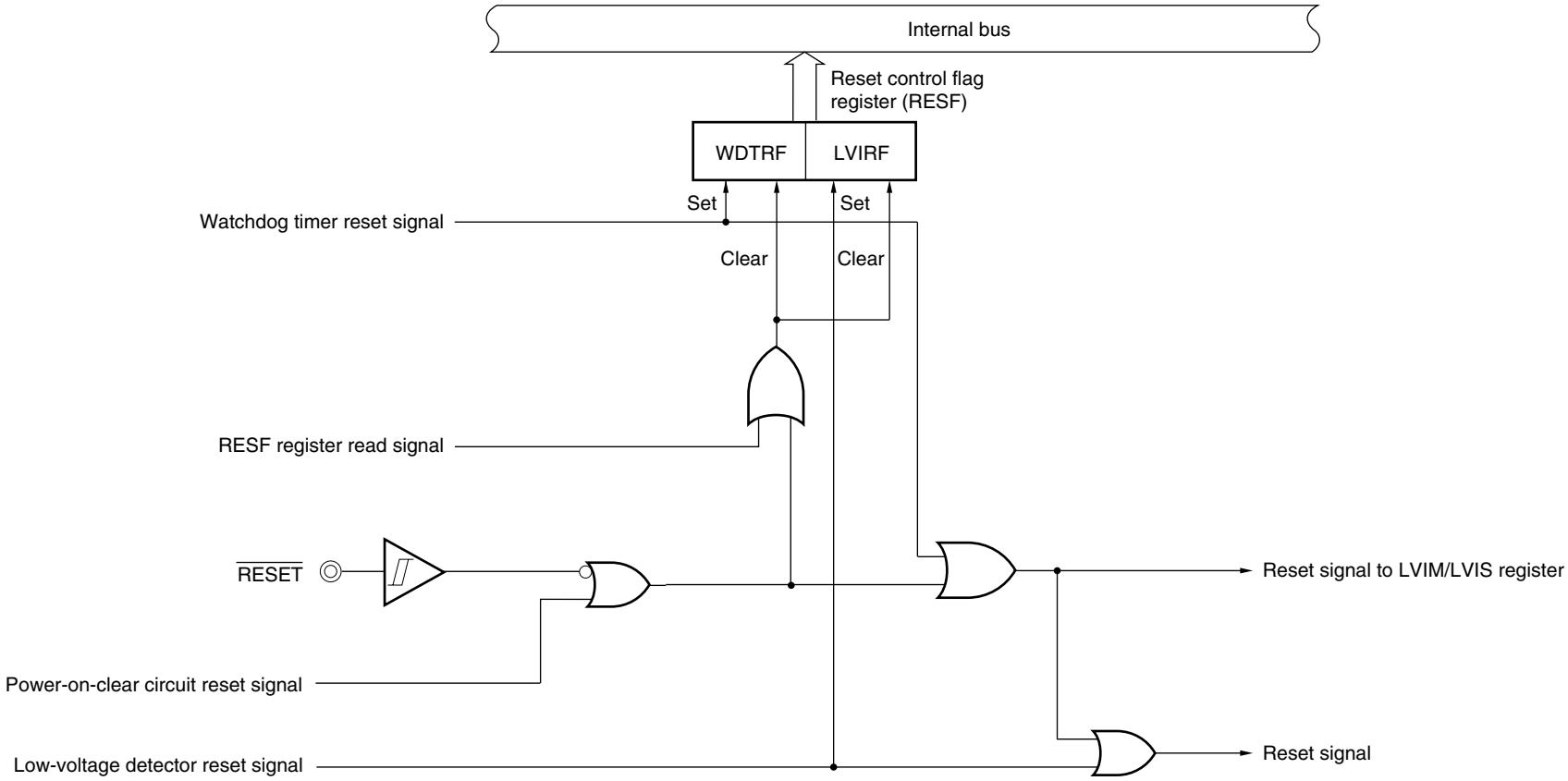
A reset is applied when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POC and LVI circuit voltage detection, and each item of hardware is set to the status shown in Tables 20-1 and 20-2. Each pin is high impedance during reset signal generation or during the oscillation stabilization time just after a reset release.

When a low level is input to the $\overline{\text{RESET}}$ pin, the device is reset. It is released from the reset status when a high level is input to the $\overline{\text{RESET}}$ pin and program execution is started with the internal high-speed oscillation clock after reset processing. A reset by the watchdog timer is automatically released, and program execution starts using the internal high-speed oscillation clock (refer to **Figures 20-2** to **20-4**) after reset processing. Reset by POC and LVI circuit power supply detection is automatically released when $V_{DD} \geq V_{POR}$ or $V_{DD} \geq V_{LVI}$ after the reset, and program execution starts using the internal high-speed oscillation clock (refer to **CHAPTER 21 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 22 LOW-VOLTAGE DETECTOR**) after reset processing.

Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.
(If an external reset is effected upon power application, the period during which the supply voltage is outside the operating range (V_{DD} < 1.8 V) is not counted in the 10 μs. However, the low-level input may be continued before POC is released.)
2. During reset signal generation, the X1 clock, XT1 clock[Note], internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input and external subsystem clock[Note] input become invalid.
3. When the STOP mode is released by a reset, the RAM contents in the STOP mode are held during reset input. However, because SFR is initialized, the port pins become high-impedance.

Note 78K0/KC2-L only

Figure 20-1. Block Diagram of Reset Function



Caution An LVI circuit internal reset does not reset the LVI circuit.

Remarks 1. LVIM: Low-voltage detection register

2. LVIS: Low-voltage detection level selection register

(2/8)

Edition	Description	Chapter
2nd Edition	Modification of **Figure 4-45 Format of A/D Port Configuration Register 0 (ADPC0)**	**CHAPTER 4 PORT FUNCTIONS**
	Modification of **Figure 4-46 Format of A/D Port Configuration Register 1 (ADPC1) (78K0/KB2-L and 78K0/KC2-L Only)**	
	Modification of PM×× and P×× value of P125 pin in **Table 4-12 Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KY2-L)** to **Table 4-15 Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KC2-L)**	
	Modification of **Table 4-14 Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KB2-L) (1/2)** and **Table 4-15 Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KC2-L) (1/3)**	
	Modification of **Figure 5-2 Block Diagram of Clock Generator (78K0/KC2-L)**	**CHAPTER 5 CLOCK GENERATOR**
	Modification of and addition of **Caution 3** to **Figure 5-4 Format of Clock Operation Mode Select Register (OSCCTL) (78K0/KC2-L)**	
	Modification of **Caution 1** in **5.4 System Clock Oscillator**	
	Modification of **Figure 6-9 Format of Prescaler Mode Register 00 (PRM00)**	**CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00**
	Modification of **Figure 6-13 (d) Prescaler mode register 00 (PRM00)**	
	Modification of **Figure 6-17 (d) Prescaler mode register 00 (PRM00)**	
	Modification of **Figure 6-20 (d) Prescaler mode register 00 (PRM00)**	
	Modification of **Figure 6-30 (d) Prescaler mode register 00 (PRM00)**	
	Modification of **Figure 6-38 (d) Prescaler mode register 00 (PRM00)**	
	Modification of **Figure 6-41 (d) Prescaler mode register 00 (PRM00)** and **(f) 16-bit capture/compare register 000 (CR000)**	
	Modification of **Figure 6-44 (d) Prescaler mode register 00 (PRM00)**	
	Modification of **Figure 6-51 (d) Prescaler mode register 00 (PRM00)**	
	Modification of **Figure 7-2 Block Diagram of 8-bit Timer 51 (78K0/KY2-L, 78K0/KA2-L)** and **Figure 7-3 Block Diagram of 8-bit Timer 51 (78K0/KB2-L, 78K0/KC2-L)**	**CHAPTER 7 8-BIT TIMER/EVENT COUNTERS 50 AND 51**
	Modification of **Figure 7-7 Format of Timer Clock Selection Register 51 (TCL51)**	
	Deletion of **Caution 2** from and modification of **Remark** in **Table 9-4 Setting Window Open Period of Watchdog Timer**	**CHAPTER 9 WATCHDOG TIMER**
	• Modification of the number of channels in the 78K0/KB2-L and 78K0/KC2-L • Addition of 8-bit A/D conversion result register L (ADCRL)	**CHAPTER 12 A/D CONVERTER**
	Modification of **Table 12-2 A/D Conversion Time Selection**	
	Partial deletion of description in **12.3 (2) 10-bit A/D conversion result register (ADCR)**	
	Modification of **Figure 12-9 Format of A/D Port Configuration Register 0 (ADPC0)**	
	Modification of **Figure 12-10 Format of A/D Port Configuration Register 1 (ADPC1) (78K0/KB2-L and 78K0/KC2-L Only)**	

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents