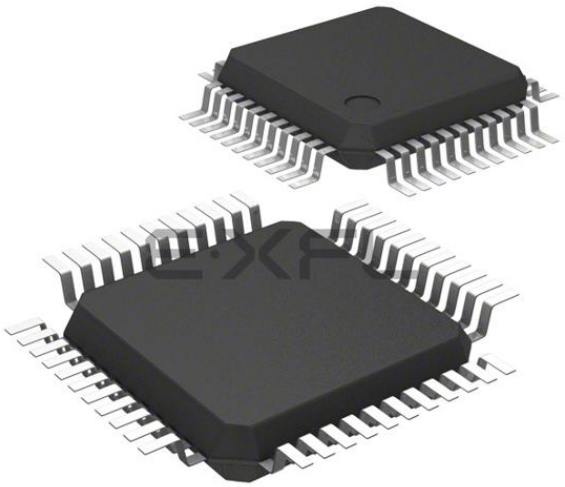

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0581gb-gaf-ax

2.1.3 78K0/KB2-L

(1) Port functions: 78K0/KB2-L

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000
P01				TI010/TO00
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	ANI8/AMP1-Note/$\overline{\text{SCK10}}$
P11				ANI9/AMP1OUTNote/SI10
P12				ANI10/AMP1+Note/SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50
P20	I/O	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0/AMP0-Note
P21				ANI1/AMP0OUTNote/PGAINNote
P22				ANI2/AMP0+Note
P23				ANI3
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1
P31				INTP2/TOOLC1
P32				INTP3/TOOLD1
P33				TI51/TO51/INTP4
P60	I/O	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Input can be set to SMBus input buffer in 1-bit units. Output can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCLA0/INTP11
P61				SDAA0/INTP10
P120	I/O	Port 12. 1-bit I/O port and 3-bit input port. For only P120 and P125, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	EXLVI/INTP0
P121	Input			X1/TOOLC0
P122				X2/EXCLK/TOOLD0
<R> P125			Reset input	$\overline{\text{RESET}}$

Note μPD78F0576, 78F0577, and 78F0578 (products with operational amplifier) only

3.3.3 Table indirect addressing

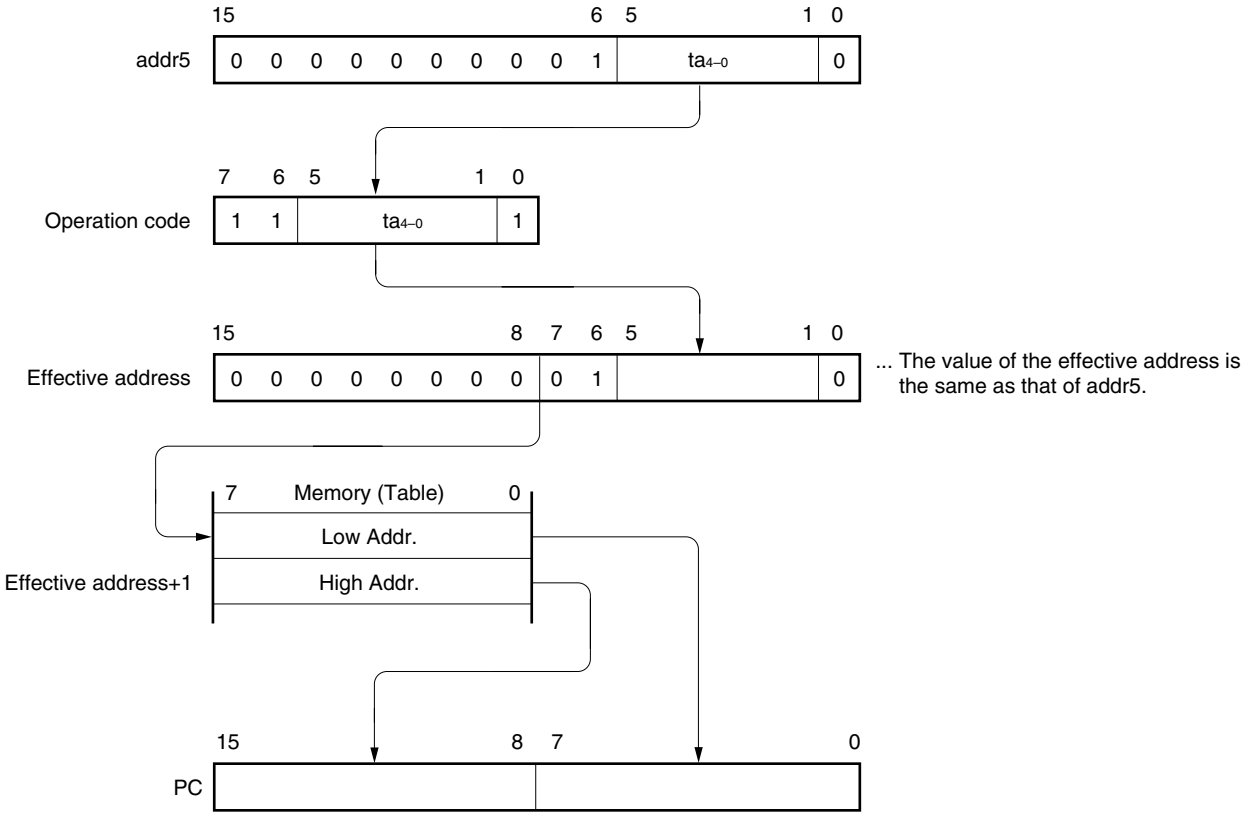
[Function]

Table contents (branch destination address) of the particular location to be addressed by bits 1 to 5 of the immediate data of an operation code are transferred to the program counter (PC) and branched.

This function is carried out when the CALLT [addr5] instruction is executed.

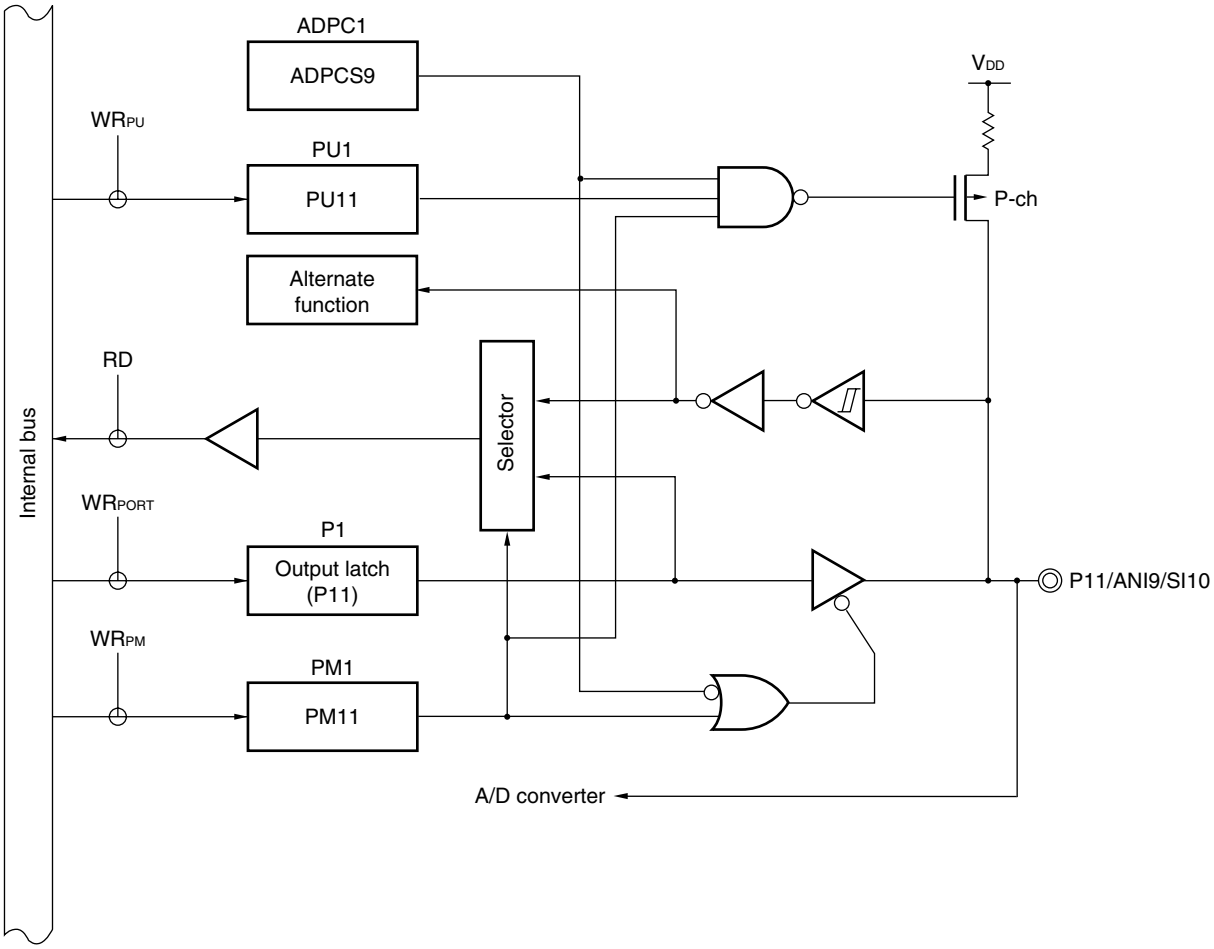
This instruction references the address that is indicated by addr5 and is stored in the memory table from 0040H to 007FH, and allows branching to the entire memory space.

[Illustration]



<R> **Figure 4-5. Block Diagram of P11 (1/2)**

(1) Products without operational amplifier of 78K0/KB2-L and 78K0/KC2-L



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
ADPC1: A/D port configuration register 1
RD: Read signal
WR××: Write signal

<R> **Table 4-18. Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KC2-L) (2/3)**

Pin Name	Alternate Function		MUXSEL	PM××	P××
	Function Name	I/O			
P20	ANI0[Note 1]	Input	–	1	×
	AMP0-[Notes 1, 2]	Input	–	1	×
P21	ANI1[Note 1]	Input	–	1	×
	AMP0OUT[Notes 1, 2]	Output	–	1	×
	PGAIN[Notes 1, 2]	Input	–	1	×
P22	ANI2[Note 1]	Input	–	1	×
	AMP0+[Notes 1, 2]	Input	–	1	×
P23 to P26, P27[Note 3]	ANI3 to ANI6[Note 1], ANI7[Notes 1, 3]	Input	–	1	×
P30	INTP1	Input	–	1	×
P31	INTP2	Input	–	1	×
	TOOLC1	Input	–	×	×
P32	INTP3	Input	–	1	×
	TOOLD1	I/O	–	×	×
P33	INTP4	Input	–	1	×
	TI51	Input	–	1	×
	TO51	Output	–	0	0
P40[Note 3]	RTCCL[Note 3]	Output	–	0	0
	RTCDIV[Note 3]	Output	–	0	0
	($\overline{SCK11}$)[Note 3]	Input	CSISEL = 1	1	×
		Output	CSISEL = 1	0	1
P41[Note 3]	RTC1HZ[Note 3]	Output	–	0	0
	(SI11)[Note 3]	Input	CSISEL = 1	1	×
P42[Note 4]	PCL[Note 4]	Output	–	0	0
	$\overline{SSI11}$[Note 4]	Input	–	1	×
	INTP6[Note 4]	Input	–	1	×
P60	SCLA0[Notes 5, 6]	I/O	–	0	1
	$\overline{SCK11}$	Input	CSISEL = 0	1	×
		Output	CSISEL = 0	0	1
	INTP11	Input	–	1	×

Notes 1. The pin function can be selected by using ADPC0 register, PM2 register, ADS register, OPAMP0E bit, and PGAIN bit. Refer to **Tables 4-10** to **4-12** of **4.2.3 Port 2**.

2. μPD78F0586, 78F0587, 78F0588 (products with operational amplifier) only

3. 44-pin and 48-pin products only

4. 48-pin products only

5. During I^2C communication, set SCLA0 and SDAA0 to N-ch open drain output (V_{DD} tolerance) mode by using POM6 register (refer to **4.3 (5) Port output mode register 6 (POM6)**).

6. When using an input compliant with the SMBus specifications in I^2C communication, select the SMBus input buffer by using PIM6 register (refer to **4.3 (4) Port input mode register 6 (PIM6)**).

Remarks 1. ×: Don't care
PM××: Port mode register
P××: Port output latch

2. Functions in parentheses ( ) can be assigned by setting MUXSEL register.

5.6.3 Example of controlling subsystem clock

The following two types of subsystem clocks[Note] are available.

- XT1 clock: Crystal/ceramic resonator is connected across the XT1 and XT2 pins.
- External subsystem clock: External clock is input to the EXCLKS pin.

When the subsystem clock is not used, the XT1/P123 and XT2/EXCLKS/P124 pins can be used as input port pins.

Note 78K0/KC2-L only

Cautions 1. The XT1/P123 and XT2/EXCLKS/P124 pins are in the input port mode after a reset release.

2. Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

The following describes examples of setting procedures for the following cases.

(1) When oscillating XT1 clock
(2) When using external subsystem clock
(3) When using subsystem clock as CPU clock
(4) When stopping subsystem clock

(1) Example of setting procedure when oscillating the XT1 clock

<1> Setting XT1 and XT2 pins and selecting operation mode (PCC and OSCCTL registers)
When a value is specified for XTSTART and EXCLKS and OSCSELS are set to the values below, the system switches from the port mode to the XT1 oscillation mode. set as any of the following, the mode is switched from port mode to XT1 oscillation mode.

XTSTART	EXCLKS	OSCSELS	Operation Mode of Subsystem Clock Pin	P123/XT1 Pin	P124/XT2/ EXCLKS Pin
0	0	1	XT1 oscillation mode	Crystal/ceramic resonator connection	
1	×	×			

Remark ×: don't care

<2> Waiting for the stabilization of the subsystem clock oscillation
Wait for the oscillation stabilization time of the subsystem clock by software, using a timer function.

Caution Do not change the value of XTSTART, EXCLKS, and OSCSELS while the subsystem clock is operating.

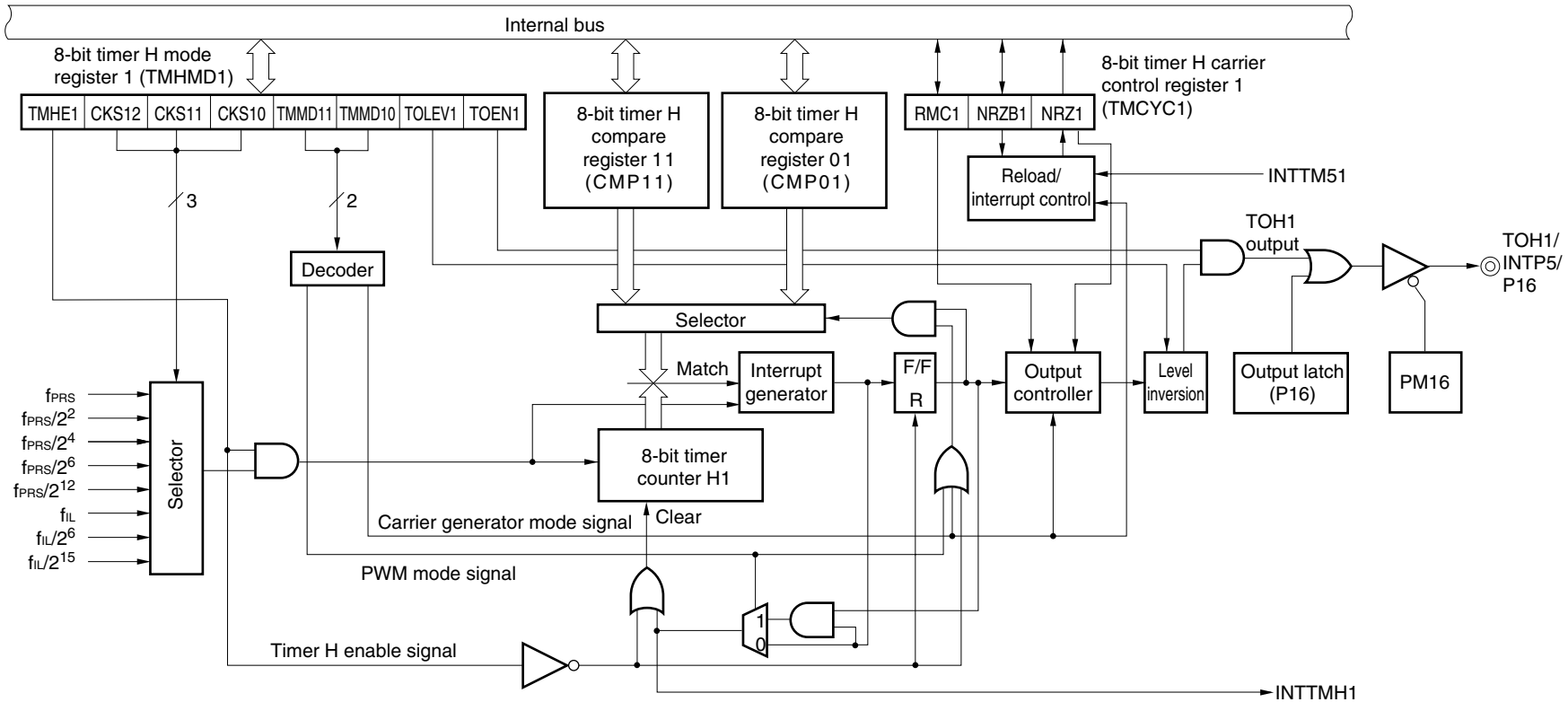
(2) Example of setting procedure when using the external subsystem clock

<1> Setting XT1 and XT2 pins, selecting XT1 clock/external clock and controlling oscillation (PCC and OSCCTL registers)
When XTSTART is cleared to 0 and EXCLKS and OSCSELS are set to 1, the mode is switched from port mode to external clock input mode. In this case, input the external clock to the EXCLKS/XT2/P124 pins.

XTSTART	EXCLKS	OSCSELS	Operation Mode of Subsystem Clock Pin	P123/XT1 Pin	P124/XT2/ EXCLKS Pin
0	1	1	External clock input mode	Input port	External clock input

Caution Do not change the value of XTSTART, EXCLKS, and OSCSELS while the subsystem clock is operating.

Figure 8-2. Block Diagram of 8-Bit Timer H1

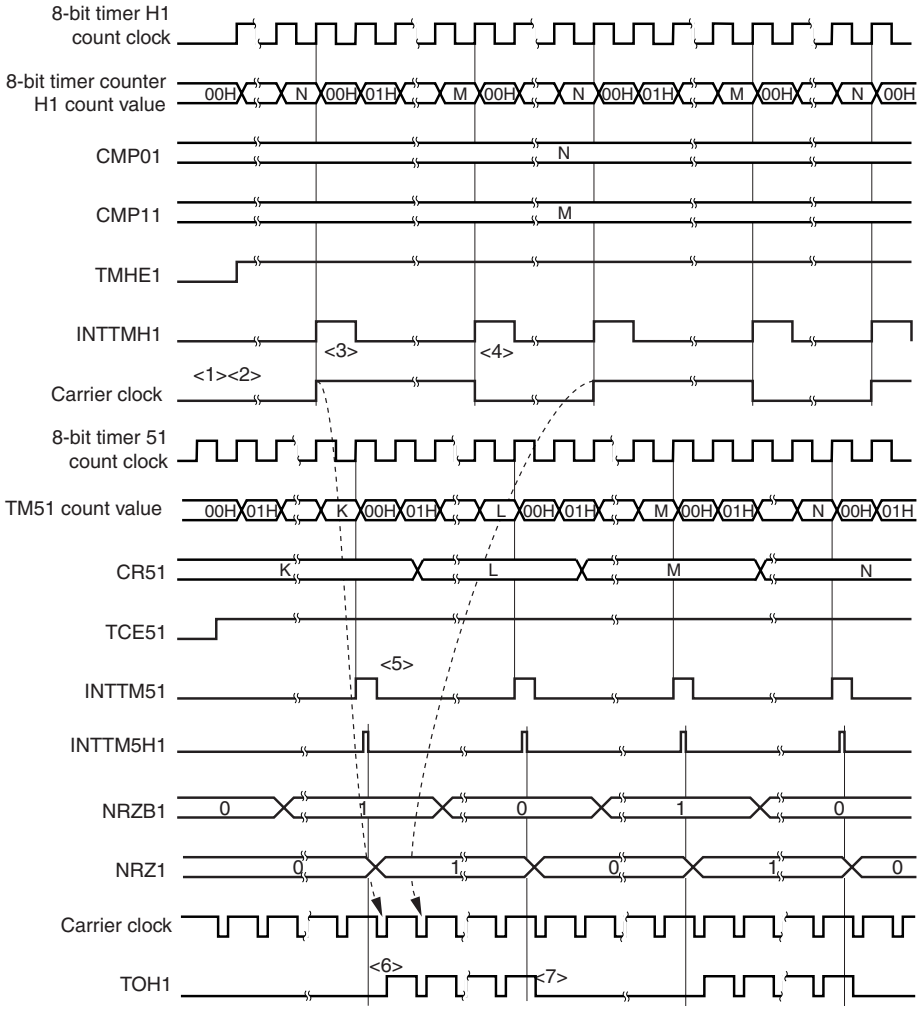


<R> **Remark** 78K0/KY2-L, 78K0/KA2-L (20-pin products): TOH1/TI51/INTP1/P30

78K0/KA2-L (25-pin products):	(TOH1)/(TI51)/INTP4/P34	(When TMHSEL1,TMHSEL0 = 0, 1)
	(TOH1)/(TI51)/INTP0/TI00/P00	(When TMHSEL1,TMHSEL0 = 1, 0)
78K0/KA2-L (32-pin products):	(TOH1)/INTP4/P34	(When TMHSEL0 = 1)
78K0/KB2-L, 78K0/KC2-L:	TOH1/INTP5/P16	

Figure 8-18. Carrier Generator Mode Operation Timing (2/3)

(b) Operation when CMP01 = N, CMP11 = M



<1> When TMHE1 = 0 and TCE51 = 0, the 8-bit timer counter H1 operation is stopped.

<2> When TMHE1 = 1 is set, the 8-bit timer counter H1 starts a count operation. At that time, the carrier clock remains default.

<3> When the count value of the 8-bit timer counter H1 matches the CMP01 register value, the first INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP01 register to the CMP11 register. The 8-bit timer counter H1 is cleared to 00H.

<4> When the count value of the 8-bit timer counter H1 matches the CMP11 register value, the INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP11 register to the CMP01 register. The 8-bit timer counter H1 is cleared to 00H. By performing procedures <3> and <4> repeatedly, a carrier clock with duty fixed to other than 50% is generated.

<5> When the INTTM51 signal is generated, it is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal.

<6> A carrier signal is output at the first rising edge of the carrier clock if NRZ1 is set to 1.

<7> When NRZ1 = 0, the TOH1 output is held at the high level and is not changed to low level while the carrier clock is high level (from <6> and <7>, the high-level width of the carrier clock waveform is guaranteed).

Remark INTTM5H1 is an internal signal and not an interrupt source.

Correction example <2>

Example of correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm)

[Measuring the oscillation frequency]

The oscillation frequency[Note] of each product is measured by outputting about 32 kHz from the RTCCL pin or outputting about 1 Hz from the RTC1HZ pin when the watch error correction register is set to its initial value (00H).

Note Refer to **10.4.5 1 Hz output of real-time counter** for the setting procedure of outputting about 1 Hz from the RTC1HZ pin, and **10.4.6 32.768 kHz output of real-time counter** for the setting procedure of outputting about 32 kHz from the RTCCL pin.

[Calculating the correction value]

(When the output frequency from the RTCCL pin is 0.9999817 Hz)

Oscillation frequency = 32768 × 0.9999817 ≈ 32767.4 Hz

Assume the target frequency to be 32768 Hz (32767.4 Hz + 18.3 ppm) and DEV to be 1.

The expression for calculating the correction value when DEV is 1 is applied.

Correction value = Number of correction counts in 1 minute
= (Oscillation frequency ÷ Target frequency − 1) × 32768 × 60
= (32767.4 ÷ 32768 − 1) × 32768 × 60
= −36

[Calculating the values to be set to (F6 to F0)]

(When the correction value is −36)

If the correction value is 0 or less (when quickening), assume F6 to be 1.

Calculate (F5, F4, F3, F2, F1, F0) from the correction value.

− {(/F5, /F4, /F3, /F2, /F1, /F0) − 1} × 2	= −36
(/F5, /F4, /F3, /F2, /F1, /F0)	= 17
(/F5, /F4, /F3, /F2, /F1, /F0)	= (0, 1, 0, 0, 0, 1)
(F5, F4, F3, F2, F1, F0)	= (1, 0, 1, 1, 1, 0)

Consequently, when correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm), setting the correction register such that DEV is 1 and the correction value is −36 (bits 6 to 0 of SUBCUD: 1101110) results in 32768 Hz (0 ppm).

Figure 10-28 shows the operation when (DEV, F6, F5, F4, F3, F2, F1, F0) is (1, 1, 1, 0, 1, 1, 1, 0).

<R> **Figure 12-9. Format of A/D Port Configuration Registers 0, 1 (ADPC0, ADPC1) (3/3)**

(g) 78K0/KC2-L (44-pin and 48-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	ADPCS7	ADPCS6	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

Address: FF2FH After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC1	0	0	0	0	0	ADPCS10	ADPCS9	ADPCS8

ADPCSn	Digital I/O or analog I/O selection (n = 0 to 10)
0	Analog I/O
1	Digital I/O

Cautions 1. Set the pin set to analog I/O to the input mode by using port mode registers 1, 2, 7 (PM1, PM2, PM7).

2. If data is written to ADPC0 and ADPC1, a wait cycle is generated. Do not write data to ADPC0 and ADPC1 when the peripheral hardware clock is stopped. For details, refer to CHAPTER 31 CAUTIONS FOR WAIT.

(7) Port mode registers 1, 2, 7 (PM1, PM2, PM7)

<R> When using the ANI8/AMP1-/P10 to ANI10/AMP1+/P12, ANI0/AMP0-/P20 to ANI7/P27, and ANI8/P70 to ANI10/P72 pins for analog input port, set PM10 to PM12, PM20 to PM27, PM70 to PM72 to 1. The output latches of P10 to P12, P20 to P27, and P70 to P72 at this time may be 0 or 1.

If PM10 to PM12, PM20 to PM27, and P70 to P72 are set to 0, they cannot be used as analog input port pins.

PM1, PM2, and PM7 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Remark A/D converter analog input pins differ depending on products.

- 78K0/KY2-L: ANI0 to ANI3
- 78K0/KA2-L (20-pin products): ANI0 to ANI5
- 78K0/KA2-L (25-pin products): ANI0 to ANI6
- 78K0/KA2-L (32-pin products): ANI0 to ANI10
- 78K0/KB2-L: ANI0 to ANI3, ANI8 to ANI10
- 78K0/KC2-L (40-pin product): ANI0 to ANI6, ANI8 to ANI10
- 78K0/KC2-L (44-pin and 48-pin products): ANI0 to ANI10

(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale – 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

(7) Differential linearity error

While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

Figure 12-18. Zero-Scale Error

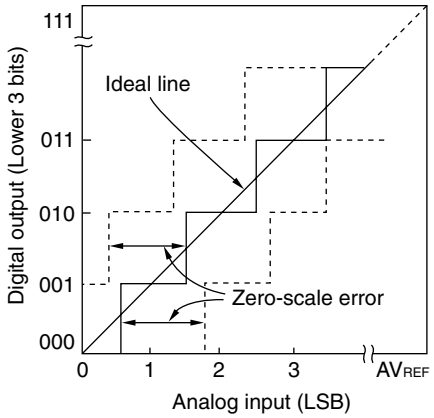


Figure 12-19. Full-Scale Error

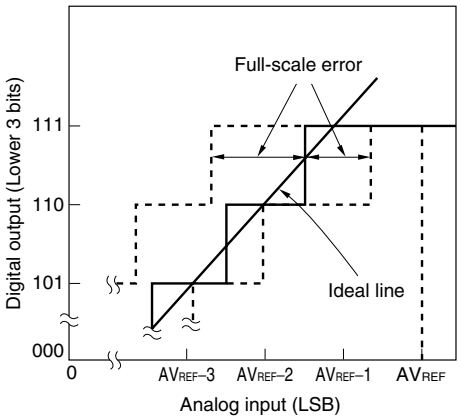


Figure 12-20. Integral Linearity Error

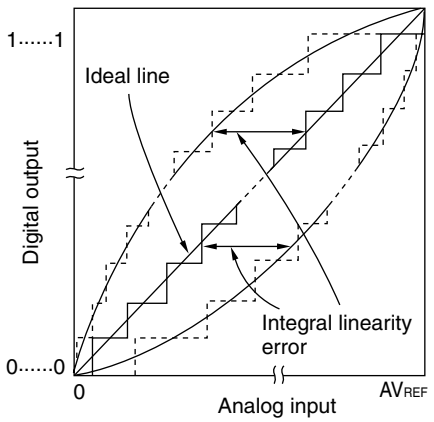
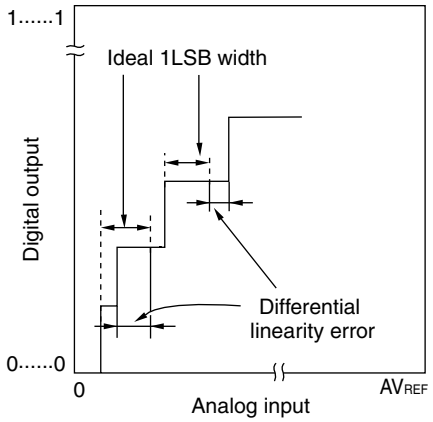


Figure 12-21. Differential Linearity Error



(8) Conversion time

This expresses the time from the start of sampling to when the digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.

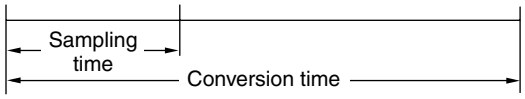
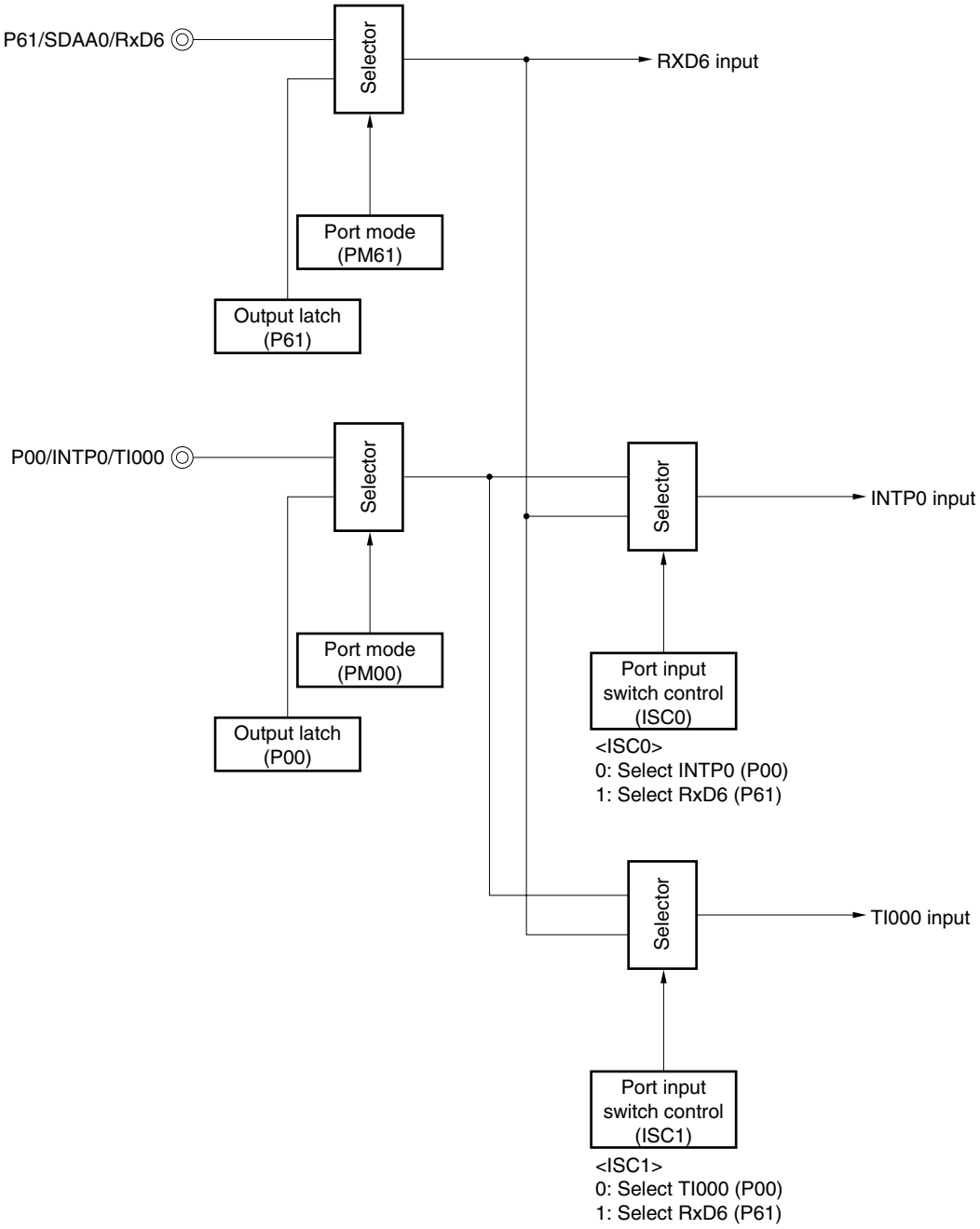


Figure 14-3. Port Configuration for LIN Reception Operation (1/2)

(1) 78K0/KY2-L and 78K0/KA2-L



Remark ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (refer to **Figure 14-11**)

Figure 14-8. Format of Clock Selection Register 6 (CKSR6)

Address: FF56H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CKSR6	0	0	0	0	TPS63	TPS62	TPS61	TPS60

TPS63	TPS62	TPS61	TPS60	Base clock (f_{XCLK6}) selection[Note 1]			
					f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	0	f_{PRS}	2 MHz	5 MHz	10 MHz
0	0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
0	0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	0	1	1	$f_{PRS}/2^3$	250 kHz	625 kHz	1.25 MHz
0	1	0	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz
0	1	0	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	312.5 kHz
0	1	1	0	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
0	1	1	1	$f_{PRS}/2^7$	15.625 kHz	39.06 kHz	78.13 kHz
1	0	0	0	$f_{PRS}/2^8$	7.813 kHz	19.53 kHz	39.06 kHz
1	0	0	1	$f_{PRS}/2^9$	3.906 kHz	9.77 kHz	19.53 kHz
1	0	1	0	$f_{PRS}/2^{10}$	1.953 kHz	4.88 kHz	9.77 kHz
1	0	1	1	TM50 output[Notes 2, 3]			
Other than above				Setting prohibited			

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. Note the following points when selecting the TM50 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

3. 78K0/KB2-L and 78K0/KC2-L only

Caution Make sure POWER6 = 0 when rewriting TPS63 to TPS60.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. TMC506: Bit 6 of 8-bit timer mode control register 50 (TMC50)
TMC501: Bit 1 of TMC50

14.4.4 Calculation of baud rate

(1) Baud rate calculation expression

The baud rate can be calculated by the following expression.

- Baud rate = $\frac{f_{XCLK6}}{2 \times k}$ [bps]

f_{XCLK6}: Frequency of base clock selected by TPS63 to TPS60 bits of CKSR6 register

k: Value set by MDL67 to MDL60 bits of BRGC6 register (k = 4, 5, 6, ..., 255)

Table 14-4. Set Value of TPS63 to TPS60

TPS63	TPS62	TPS61	TPS60	Base Clock (f_{XCLK6}) Selection[Note 1]			
					f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	0	f_{PRS}	2 MHz	5 MHz	10 MHz
0	0	0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
0	0	1	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	0	1	1	$f_{PRS}/2^3$	250 kHz	625 kHz	1.25 MHz
0	1	0	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz
0	1	0	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	312.5 kHz
0	1	1	0	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
0	1	1	1	$f_{PRS}/2^7$	15.625 kHz	39.06 kHz	78.13 kHz
1	0	0	0	$f_{PRS}/2^8$	7.813 kHz	19.53 kHz	39.06 kHz
1	0	0	1	$f_{PRS}/2^9$	3.906 kHz	9.77 kHz	19.53 kHz
1	0	1	0	$f_{PRS}/2^{10}$	1.953 kHz	4.88 kHz	9.77 kHz
1	0	1	1	TM50 output[Note 2]			
Other than above				Setting prohibited			

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. Note the following points when selecting the TM50 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)

  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)

  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

Table 16-2. Relationship Between Register Settings and Pins (4/4)

(d) Serial interface CSI11 (78K0/KA2-L (25-pin and 32-pin products))

CSIE11	TRMD11	SSE11	PM36	P36	PM37	P37	PM35	P35	PM02	P02	CSI11 Operation	Pin Function			
												SI11/P36	SO11/P37	$\overline{\text{SCK11}}$/P35	$\overline{\text{SSI11}}$/P02/INTP5
0	0	×	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	Stop	P36	P37	P35Note 2	P02/INTP5
1	0	0	1	×	×Note 1	×Note 1	1	×	×Note 1	×Note 1	Slave reception Note 3	SI11	P37	$\overline{\text{SCK11}}$ (input) Note 3	P02/INTP5
		1							1	×					$\overline{\text{SSI11}}$
1	1	0	×Note 1	×Note 1	0	0	1	×	×Note 1	×Note 1	Slave transmission Note 3	P36	SO11	$\overline{\text{SCK11}}$ (input) Note 3	P02/INTP5
		1							1	×					$\overline{\text{SSI11}}$
1	1	0	1	×	0	0	1	×	×Note 1	×Note 1	Slave transmission/ reception Note 3	SI11	SO11	$\overline{\text{SCK11}}$ (input) Note 3	P02/INTP5
		1							1	×					$\overline{\text{SSI11}}$
1	0	0	1	×	×Note 1	×Note 1	0	1	×Note 1	×Note 1	Master reception	SI11	P37	$\overline{\text{SCK11}}$ (output)	P02/INTP5
1	1	0	×Note 1	×Note 1	0	0	0	1	×Note 1	×Note 1	Master transmission	P36	SO11	$\overline{\text{SCK11}}$ (output)	P02/INTP5
1	1	0	1	×	0	0	0	1	×Note 1	×Note 1	Master transmission/ reception	SI11	SO11	$\overline{\text{SCK11}}$ (output)	P02/INTP5

Notes 1. Can be set as port function.

2. To use P37/$\overline{\text{SCK11}}$ as port pins, clear CKP11 to 0.

3. To use the slave mode, set CKS112, CKS111, and CKS110 to 1, 1, 1.

Remark ×: don't care

CSIE11: Bit 7 of serial operation mode register 11 (CSIM11)

TRMD11: Bit 6 of CSIM11

CKP11: Bit 4 of serial clock selection register 11 (CSIC11)

CKS112, CKS111, CKS110: Bits 2 to 0 of CSIC11

PM×: Port mode register

P×: Port output latch

Figure 17-8. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H)
(48-pin products of 78K0/KC2-L)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIF50	TMIFH0	TMIFH1	CSIIF10	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF1L	PIF8	PIF7	RTCIF	KRIF	TMIF51	RTCIIF	PIF6	ADIF

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
IF1H	0	0	0	PIF11	PIF10	PIF9	CSIIF11	IICAIF0

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Caution Be sure to clear bits 5 to 7 of IF1H to 0.

Figure 17-23. Format of External Interrupt Rising Edge Enable Registers (EGPCTL0, EGPCTL1) and External Interrupt Falling Edge Enable Registers (EGNCTL0, EGNCTL1) (4/5)

(f) 44-pin products of 78K0/KC2-L

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGPCTL0	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGNCTL0	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

Address: FF4AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGPCTL1	0	0	0	0	EGP11	EGP10	EGP9	EGP8

Address: FF4BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGNCTL1	0	0	0	0	EGN11	EGN10	EGP9	EGP8

EGPn	EGNn	INTPn pin valid edge selection
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Caution Be sure to clear bits 6 and 7 of EGPCTL0 and EGNCTL0, and bits 4 to 7 of EGPCTL1 and EGNCTL1 to 0 in the 44-pin products of 78K0/KC2-L.

Remark n = 0 to 5, 8 to 11: 44-pin products of 78K0/KC2-L

Table 19-1. Operating Statuses in HALT Mode (1/2)

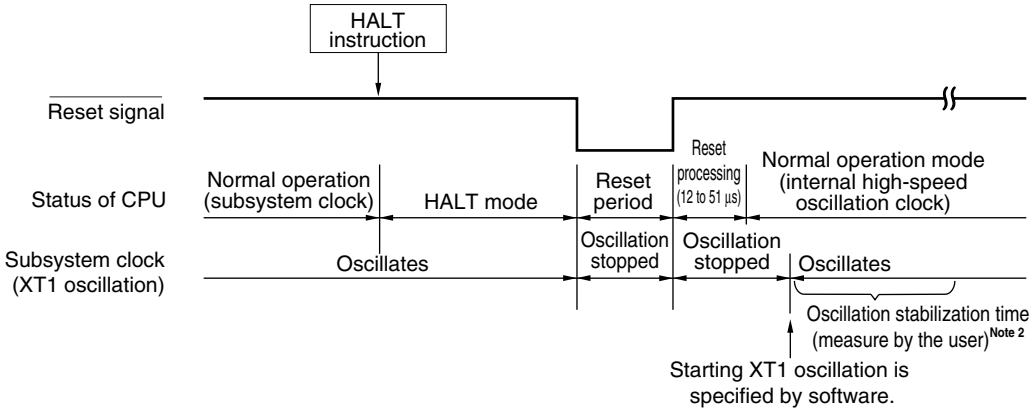
HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EXCLK})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}	Operation continues (cannot be stopped)	Status before HALT mode was set is retained	
		f_X	Status before HALT mode was set is retained	Operation continues (cannot be stopped)	Status before HALT mode was set is retained
		f_{EXCLK}	Operates or stops by external clock input		Operation continues (cannot be stopped)
	Subsystem clock	f_{XT}	Status before HALT mode was set is retained		
		f_{EXCLKS}	Operates or stops by external clock input		
	f_{IL}		Status before HALT mode was set is retained		
CPU			Operation stopped		
Flash memory					
RAM			Status before HALT mode was set is retained		
Port (latch)					
16-bit timer/event counter 00			Operable		
8-bit timer/event counter		50			
		51			
8-bit timer		H0			
		H1			
Real-time counter (RTC)					
Watchdog timer			Operable. Clock supply to watchdog timer stops when “internal low-speed oscillator can be stopped by software” is set by option byte.		
Clock output			Operable		
A/D converter					
Operational amplifiers 0, 1					
Serial interface		UART6			
		CSI10			
		CSI11			
		IICA			
Key interrupt					
Power-on-clear function					
Low-voltage detection function					
External interrupt					

Remarks 1. f_{IH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{XT}: XT1 clock
f_{EXCLKS}: External subsystem clock, f_{IL}: Internal low-speed oscillation clock

2. The functions mounted depend on the product. Refer to **1.4 Block Diagram** and **1.5 Outline of Functions**.

Figure 19-4. HALT Mode Release by Reset (2/2)

(3) When subsystem clock is used as CPU clock[Note1]



Notes 1. 78K0/KC2-L only

2. Oscillation stabilization time is not required when using the external subsystem clock (f_{EXCLKS}) as the subsystem clock.

Table 19-2. Operation in Response to Interrupt Request in HALT Mode

Release Source	MK××	PR××	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	HALT mode held
Reset	–	–	×	×	Reset processing

×: don't care

19.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the main system clock.

Caution Because the interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.

The operating statuses in the STOP mode are shown below.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (78K0/KY2-L, 78K0/KA2-L (20 pins), 78K0/KB2-L, 78K0/KC2-L) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	AV_{REF}		−0.5 to V_{DD} + 0.3 Note 1	V
	AV_{SS}		−0.5 to +0.3	V
REGC pin input voltage Note 2	V_{IREGC}		−0.5 to +3.6 and −0.5 to V_{DD} +0.3	V
Input voltage	V_{I1}	P00 to P02, P10 to P17, P30 to P33, P40 to P42, P60 to P63, P70 to P75, P120 to P125, X1, X2, XT1, XT2, $\overline{\text{RESET}}$	−0.3 to V_{DD} + 0.3 Note 1	V
	V_{I2}	P20 to P27	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V
Output voltage	V_{O1}	P00 to P02, P10 to P17, P30 to P33, P40 to P42, P60 to P63, P70 to P75, P120	−0.3 to V_{DD} + 0.3 Note 1	V
	V_{O2}	P20 to P27	−0.3 to AV_{REF} + 0.3 Note 1	V
Analog input voltage	V_{AN1}	ANI0 to ANI7, AMP0+, AMP0-	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V
	V_{AN2}	ANI8 to ANI10, AMP1+, AMP1-	−0.3 to V_{DD} + 0.3 Note 1	V

Notes 1. Must be 6.5 V or lower.

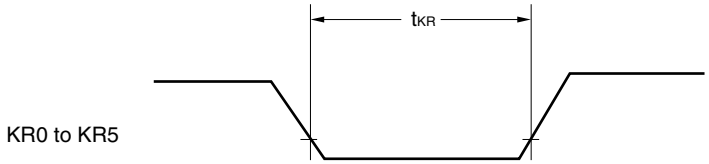
2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing