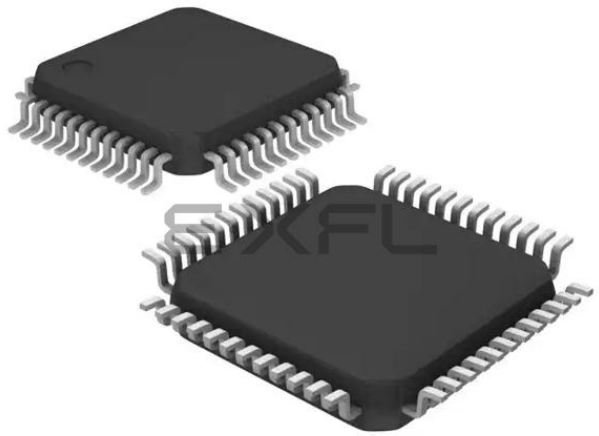
Renesas Electronics America Inc - UPD78F0582GA-GAM-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0582ga-gam-ax

<R>

Figure 2-1. Pin I/O Circuit List (4/4)

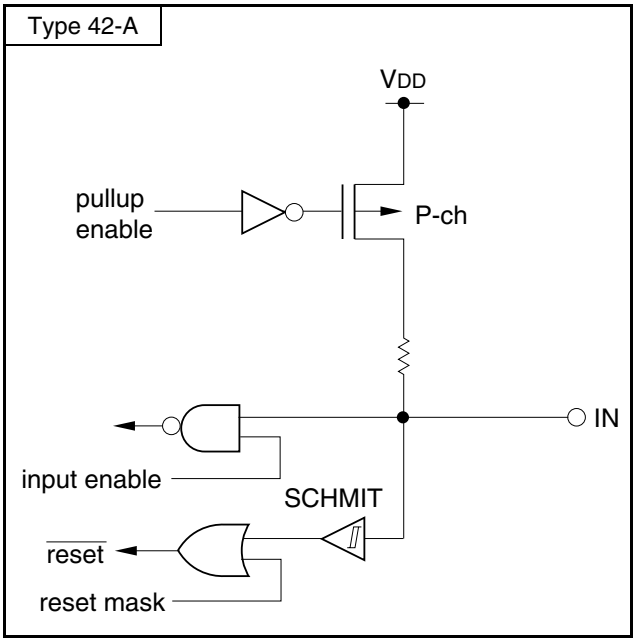
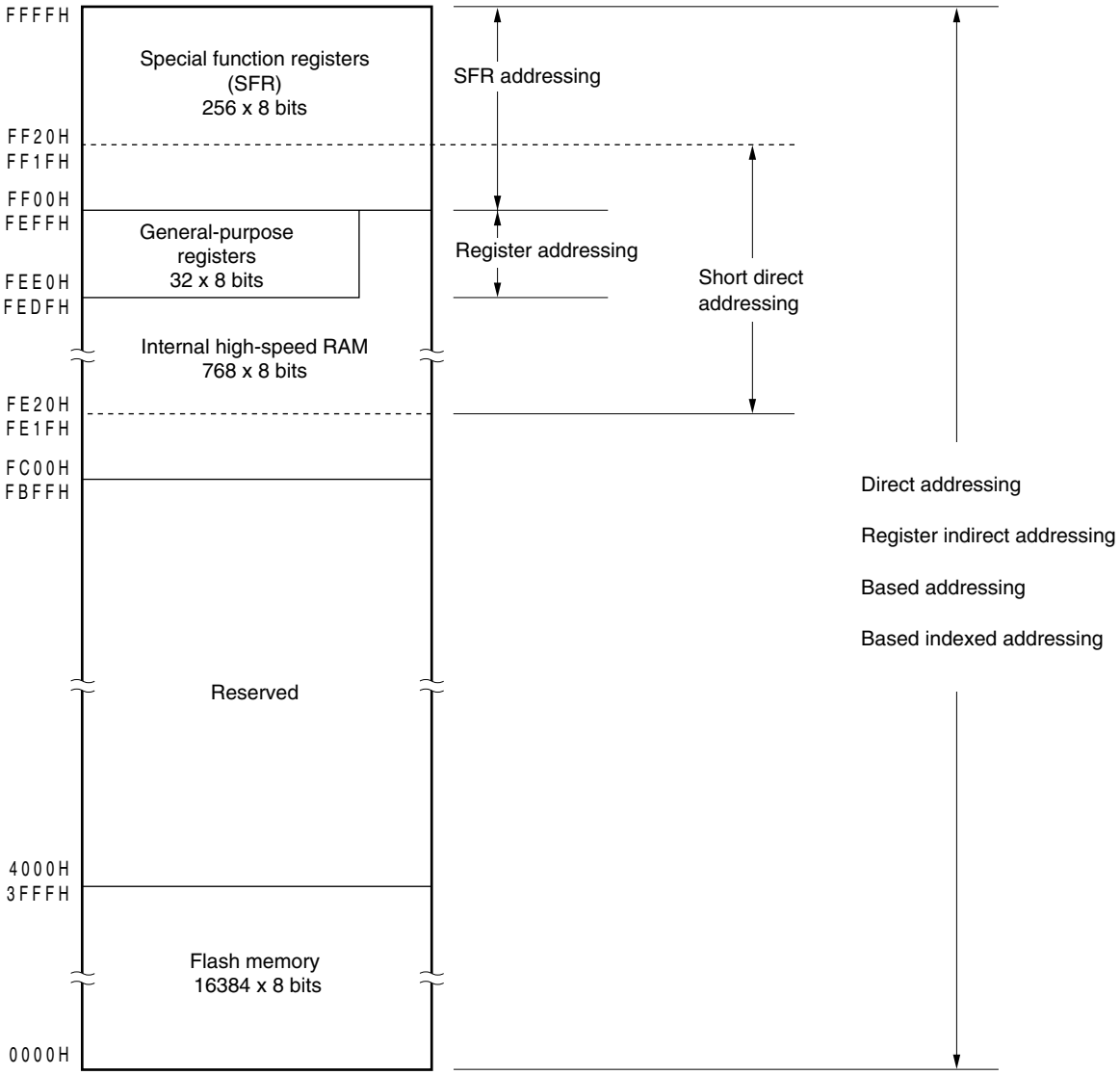


Figure 3-7. Correspondence Between Data Memory and Addressing
(μPD78F0552, 78F0557, 78F0562, 78F0567, 78F0572, 78F0577, 78F0582, 78F0587)



3.4.3 Direct addressing

[Function]

The memory to be manipulated is directly addressed with immediate data in an instruction word becoming an operand address.

This addressing can be carried out for all of the memory spaces.

[Operand format]

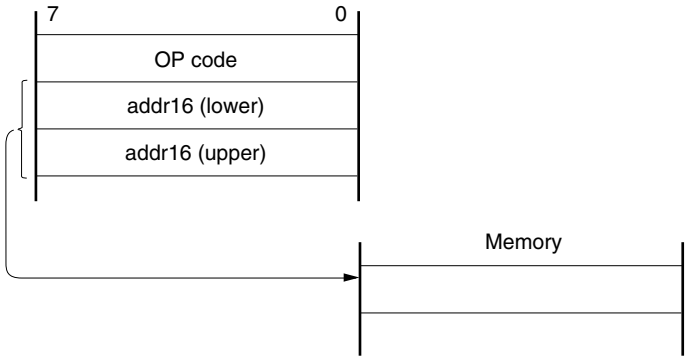
Identifier	Description
addr16	Label or 16-bit immediate data

[Description example]

MOV A, !0FE00H; when setting !addr16 to FE00H

Operation code	1 0 0 0 1 1 1 0	OP code
	0 0 0 0 0 0 0 0	00H
	1 1 1 1 1 1 1 0	FEH

[Illustration]



<R> **Table 4-18. Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/KC2-L) (1/3)**

Pin Name	Alternate Function		MUXSEL	PM××	P××
	Function Name	I/O			
P00	TI000	Input	–	1	×
P01	TI010	Input	–	1	×
	TO00	Output	–	0	0
P02[Note 1]	INTP7[Note 1]	Input	–	1	×
P10	ANI8[Note 3]	Input	–	1	×
	AMP1-[Notes 2, 3]	Input	–	1	×
	$\overline{\text{SCK10}}$	Input	–	1	×
		Output	–	0	1
P11	ANI9[Note 3]	Input	–	1	×
	AMP1OUT[Notes 2, 3]	Output	–	1	×
	SI10	Input	–	1	×
P12	ANI10[Note 3]	Input	–	1	×
	AMP1+[Notes 2, 3]	Input	–	1	×
	SO10	Output	–	0	0
P13	TxD6	Output	–	0	1
P14	RxD6	Input	–	1	×
P15	TOH0	Output	–	0	0
P16	TOH1	Output	–	0	0
	INTP5	Input	–	1	×
P17	TI50	Input	–	1	×
	TO50	Output	–	0	0

Notes 1. 48-pin products only

2. μPD78F0586, 78F0587, 78F0588 (products with operational amplifier) only

3. The pin function can be selected by using ADPC1 register, PM1 register, ADS register, and OPAMP1E bit. Refer to **Tables 4-8** and **4-9** of **4.2.2 Port 1**.

Remark ×: Don't care
PM××: Port mode register
P××: Port output latch

5.6.3 Example of controlling subsystem clock

The following two types of subsystem clocks[Note] are available.

- XT1 clock: Crystal/ceramic resonator is connected across the XT1 and XT2 pins.
- External subsystem clock: External clock is input to the EXCLKS pin.

When the subsystem clock is not used, the XT1/P123 and XT2/EXCLKS/P124 pins can be used as input port pins.

Note 78K0/KC2-L only

Cautions 1. The XT1/P123 and XT2/EXCLKS/P124 pins are in the input port mode after a reset release.

2. Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

The following describes examples of setting procedures for the following cases.

(1) When oscillating XT1 clock
(2) When using external subsystem clock
(3) When using subsystem clock as CPU clock
(4) When stopping subsystem clock

(1) Example of setting procedure when oscillating the XT1 clock

<1> Setting XT1 and XT2 pins and selecting operation mode (PCC and OSCCTL registers)
When a value is specified for XTSTART and EXCLKS and OSCSELS are set to the values below, the system switches from the port mode to the XT1 oscillation mode. set as any of the following, the mode is switched from port mode to XT1 oscillation mode.

XTSTART	EXCLKS	OSCSELS	Operation Mode of Subsystem Clock Pin	P123/XT1 Pin	P124/XT2/ EXCLKS Pin
0	0	1	XT1 oscillation mode	Crystal/ceramic resonator connection	
1	×	×			

Remark ×: don't care

<2> Waiting for the stabilization of the subsystem clock oscillation
Wait for the oscillation stabilization time of the subsystem clock by software, using a timer function.

Caution Do not change the value of XTSTART, EXCLKS, and OSCSELS while the subsystem clock is operating.

(2) Example of setting procedure when using the external subsystem clock

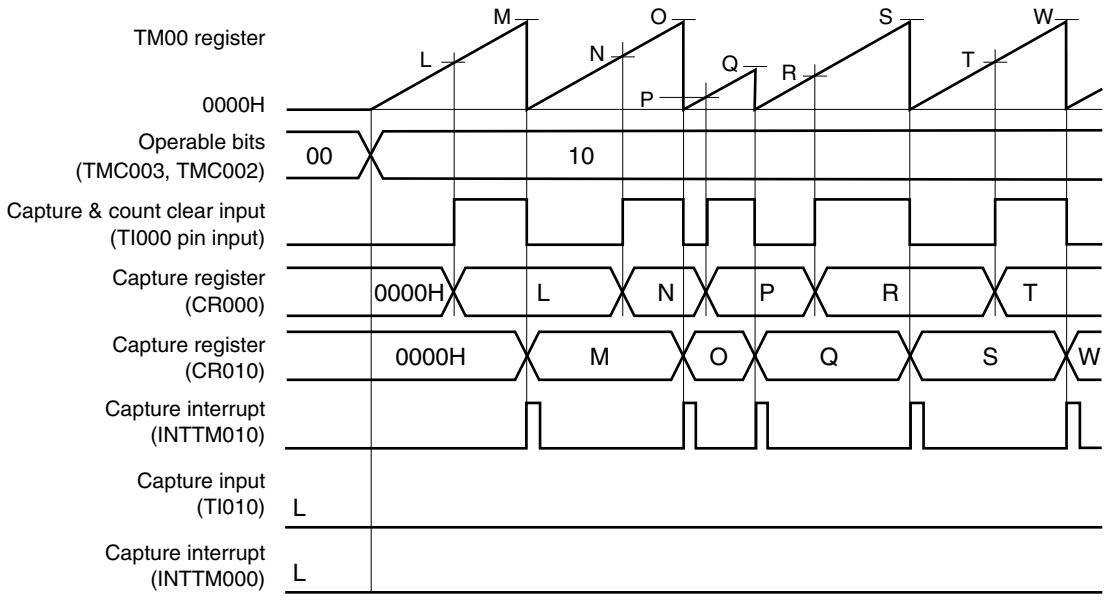
<1> Setting XT1 and XT2 pins, selecting XT1 clock/external clock and controlling oscillation (PCC and OSCCTL registers)
When XTSTART is cleared to 0 and EXCLKS and OSCSELS are set to 1, the mode is switched from port mode to external clock input mode. In this case, input the external clock to the EXCLKS/XT2/P124 pins.

XTSTART	EXCLKS	OSCSELS	Operation Mode of Subsystem Clock Pin	P123/XT1 Pin	P124/XT2/ EXCLKS Pin
0	1	1	External clock input mode	Input port	External clock input

Caution Do not change the value of XTSTART, EXCLKS, and OSCSELS while the subsystem clock is operating.

Figure 6-30. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Capture Register) (3/3)

(c) TOC00 = 13H, PRM00 = 00H, CRC00 = 07H, TMC00 = 0AH



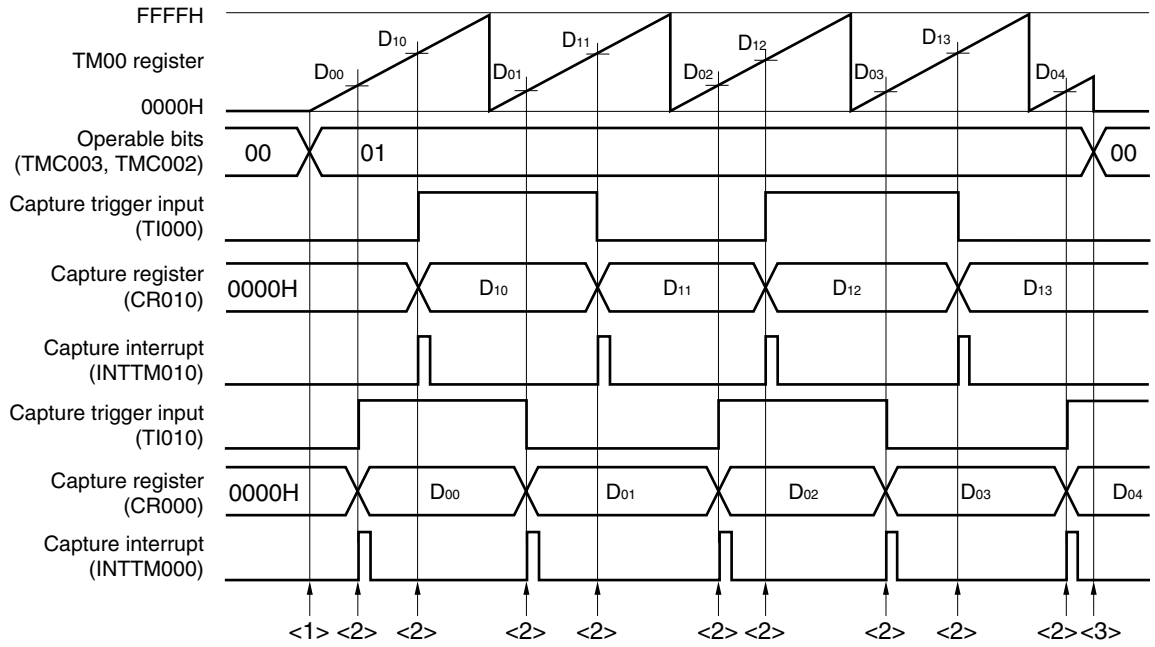
This is an application example where the pulse width of the signal input to the TI000 pin is measured.
By setting CRC00, the count value can be captured to CR000 in the phase reverse to the falling edge of the TI000 pin (i.e., rising edge) and to CR010 at the falling edge of the TI000 pin.
The high- and low-level widths of the input pulse can be calculated by the following expressions.

- High-level width = [CR010 value] – [CR000 value] × [Count clock cycle]
- Low-level width = [CR000 value] × [Count clock cycle]

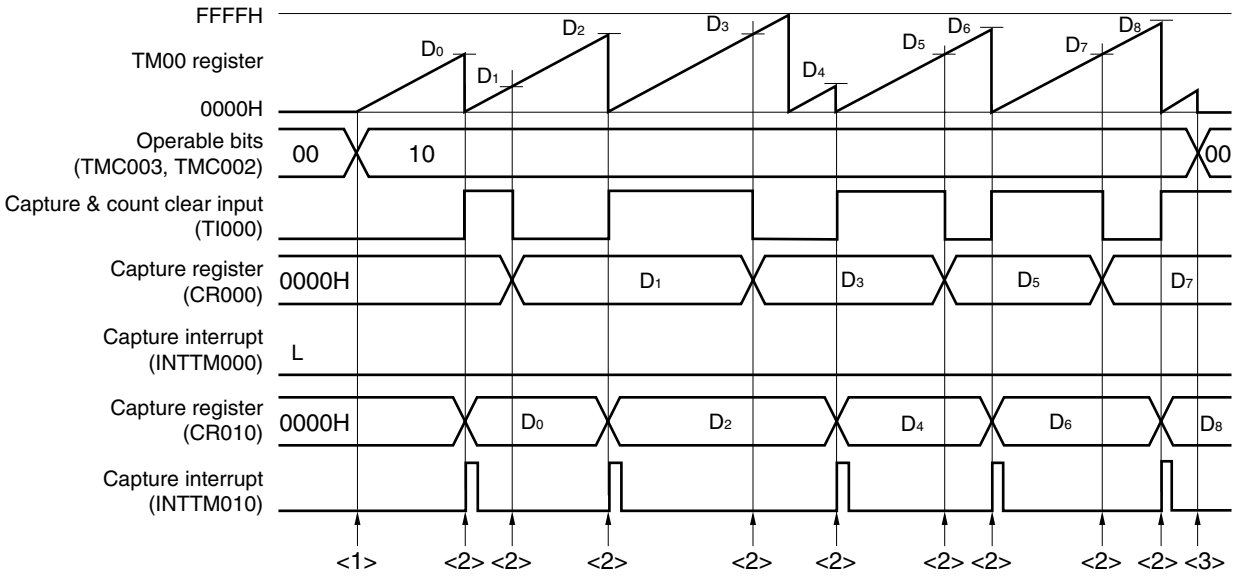
If the reverse phase of the TI000 pin is selected as a trigger to capture the count value to CR000, the INTTM000 signal is not generated. Read the values of CR000 and CR010 to measure the pulse width immediately after the INTTM010 signal is generated.
However, if the valid edge specified by bits 6 and 5 (ES110 and ES100) of prescaler mode register 00 (PRM00) is input to the TI010 pin, the count value is not captured but the INTTM000 signal is generated. To measure the pulse width of the TI000 pin, mask the INTTM000 signal when it is not used.

Figure 6-53. Example of Software Processing for Pulse Width Measurement (1/2)

(a) Example of free-running timer mode



(b) Example of clear & start mode entered by TI000 pin valid edge



7.3 Registers Controlling 8-Bit Timer/Event Counters 50 and 51

The following five registers are used to control 8-bit timer/event counters 50 and 51.

- Timer clock selection register 5n (TCL5n)
- 8-bit timer mode control register 5n (TMC5n)
- <R> Port alternate switch control register (MUXSEL) (78K0/KA2-L (25-pin products) only)
- <R> Port mode register 0 (PM0), port mode register 1 (PM1), or port mode register 3 (PM3)
- <R> Port register 0 (P0), port register 1 (P1), or port register 3 (P3)

(1) Timer clock selection register 5n (TCL5n)

This register sets the count clock of 8-bit timer/event counter 5n and the valid edge of the TI5n pin input.

TCL5n can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TCL5n to 00H.

Remark 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

Figure 7-7. Format of Timer Clock Selection Register 50 (TCL50) (78K0/KB2-L, 78K0/KC2-L Only)

Address: FF6AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TCL50	0	0	0	0	0	TCL502	TCL501	TCL500

TCL502	TCL501	TCL500	Count clock selection[Note 1]			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	TI50 pin falling edge[Note 2]			
0	0	1	TI50 pin rising edge[Note 2]			
0	1	0	f_{PRS}	2 MHz	5 MHz	10 MHz
0	1	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
1	0	0	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
1	0	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	1	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz	39.06 kHz
1	1	1	$f_{PRS}/2^{13}$	0.24 kHz	0.61 kHz	1.22 kHz

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.
- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. Do not start timer operation with the external clock from the TI50 pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. When rewriting TCL50 to other data, stop the timer operation beforehand.
2. Be sure to clear bits 3 to 7 to "0".

Remark f_{PRS}: Peripheral hardware clock frequency

Figure 7-10. Format of 8-Bit Timer Mode Control Register 51 (TMC51) (2/2)

(b) 78K0/KB2-L, 78K0/KC2-L

Address: FF43H After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC51	TCE51	TMC516	0	0	LVS51	LVR51	TMC511	TOE51

TCE51	TM51 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC516	TM51 operating mode selection
0	Mode in which clear & start occurs on a match between TM51 and CR51
1	PWM (free-running) mode

LVS51	LVR51	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO51 output: low)
1	0	Timer output F/F set (1) (default value of TO51 output: high)
1	1	Setting prohibited

TMC511	In other modes (TMC516 = 0)	In PWM mode (TMC516 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

TOE51	Timer output control
0	Output disabled (TO51 output is low level)
1	Output enabled

Note Bits 2 and 3 are write-only.

Cautions 1. The settings of LVS51 and LVR51 are valid in other than PWM mode.

2. Perform <1> to <4> below in the following order, not at the same time.

<1> Set TMC511, TMC516: Operation mode setting

<2> Set TOE51 to enable output: Timer output enable

<3> Set LVS51, LVR51 (refer to Caution 1): Timer F/F setting

<4> Set TCE51

3. When TCE51 = 1, setting the other bits of TMC51 is prohibited.

4. The actual TO51/TI51/P33/INTP4 pin output is determined depending on PM33 and P33 besides TO51 output.

Remarks 1. In PWM mode, PWM output is made inactive by clearing TCE51 to 0.

2. If LVS51 and LVR51 are read, the value is 0.

3. The values of the TMC516, LVS51, LVR51, TMC511, and TOE51 bits are reflected at the TO51 output regardless of the value of TCE51.

8.4.2 Operation as PWM output

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

The 8-bit timer compare register 0n (CMP0n) controls the cycle of timer output (TOHn). Rewriting the CMP0n register during timer operation is prohibited.

The 8-bit timer compare register 1n (CMP1n) controls the duty of timer output (TOHn). Rewriting the CMP1n register during timer operation is possible.

The operation in PWM output mode is as follows.

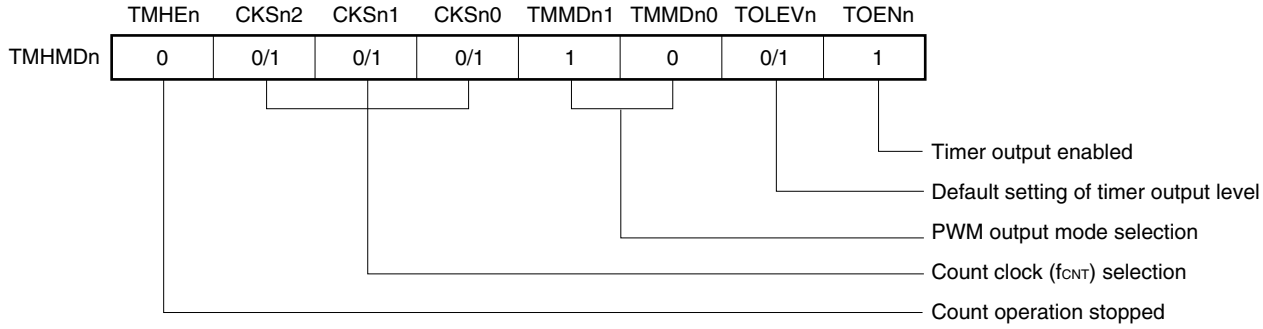
PWM output (TOHn output) outputs an active level and 8-bit timer counter Hn is cleared to 0 when 8-bit timer counter Hn and the CMP0n register match after the timer count is started. PWM output (TOHn output) outputs an inactive level when 8-bit timer counter Hn and the CMP1n register match.

Setting

<1> Set each register.

Figure 8-14. Register Setting in PWM Output Mode

(i) Setting timer H mode register n (TMHMDn)



(ii) Setting CMP0n register

- Compare value (N): Cycle setting

(iii) Setting CMP1n register

- Compare value (M): Duty setting

Remarks 1. 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

2. 00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

<2> The count operation starts when TMHEn = 1.

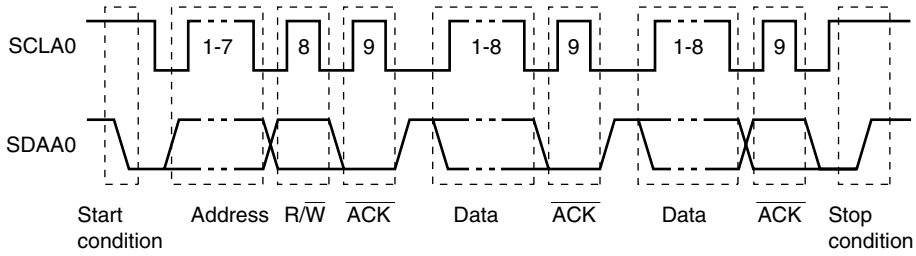
<3> The CMP0n register is the compare register that is to be compared first after counter operation is enabled. When the values of the 8-bit timer counter Hn and the CMP0n register match, the 8-bit timer counter Hn is cleared, an interrupt request signal (INTTMHn) is generated, and an active level is output. At the same time, the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP0n register to the CMP1n register.

<4> When the 8-bit timer counter Hn and the CMP1n register match, an inactive level is output and the compare register to be compared with the 8-bit timer counter Hn is changed from the CMP1n register to the CMP0n register. At this time, the 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

15.5 I^2C Bus Definitions and Control Methods

The following section describes the I^2C bus's serial data communication format and the signals used by the I^2C bus. Figure 15-15 shows the transfer timing for the "start condition", "address", "data", and "stop condition" output via the I^2C bus's serial data bus.

Figure 15-15. I^2C Bus Serial Data Transfer Timing



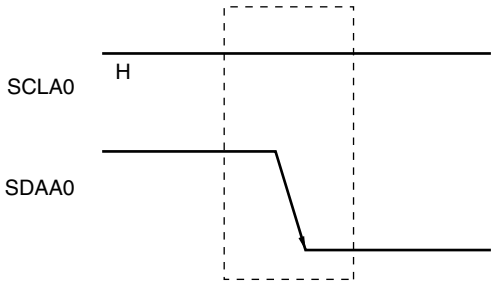
The master device generates the start condition, slave address, and stop condition.
The acknowledge ($\overline{ACK}$) can be generated by either the master or slave device (normally, it is output by the device that receives 8-bit data).

The serial clock (SCLA0) is continuously output by the master device. However, in the slave device, the SCLA0's low level period can be extended and a wait can be inserted.

15.5.1 Start conditions

A start condition is met when the SCLA0 pin is at high level and the SDAA0 pin changes from high level to low level. The start conditions for the SCLA0 pin and SDAA0 pin are signals that the master device generates to the slave device when starting a serial transfer. When the device is used as a slave, start conditions can be detected.

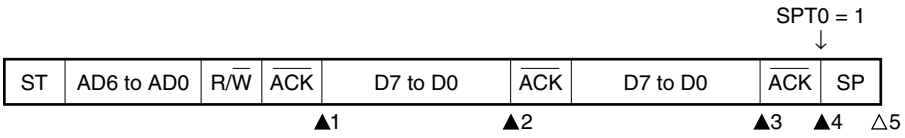
Figure 15-16. Start Conditions



A start condition is output when bit 1 (STT0) of IICA control register 0 (IICACTL0) is set (1) after a stop condition has been detected (SPD0: Bit 0 of the IICA status register 0 (IICAS0) = 1). When a start condition is detected, bit 1 (STD0) of the IICAS0 register is set (1).

(c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

(i) When WTIM0 = 0

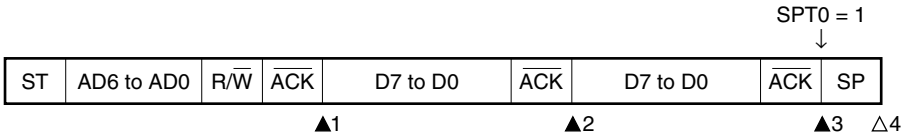


▲1: IICAS0 = 1010×110B
▲2: IICAS0 = 1010×000B
▲3: IICAS0 = 1010×000B (Sets WTIM0 to 1)[Note]
▲4: IICAS0 = 1010××00B (Sets SPT0 to 1)
△5: IICAS0 = 00000001B

Note To generate a stop condition, set WTIM0 to 1 and change the timing for generating the INTIICA0 interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1

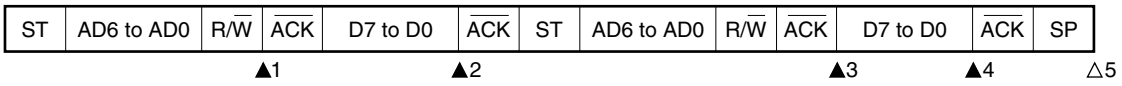


▲1: IICAS0 = 1010×110B
▲2: IICAS0 = 1010×100B
▲3: IICAS0 = 1010××00B (Sets SPT0 to 1)
△4: IICAS0 = 00001001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(b) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

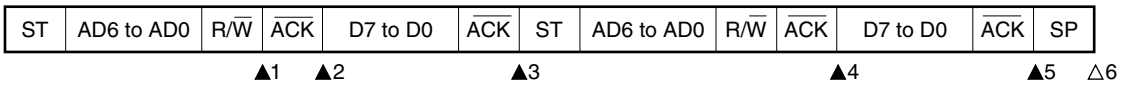
(i) When WTIM0 = 0 (after restart, matches SVA0)



▲1: IICAS0 = 0010×010B
▲2: IICAS0 = 0010×000B
▲3: IICAS0 = 0001×110B
▲4: IICAS0 = 0001×000B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

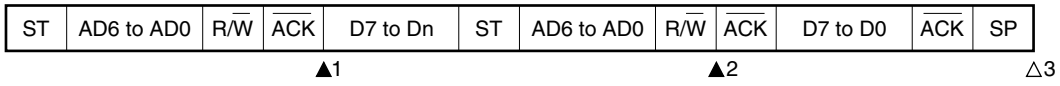
(ii) When WTIM0 = 1 (after restart, matches SVA0)



▲1: IICAS0 = 0010×010B
▲2: IICAS0 = 0010×110B
▲3: IICAS0 = 0010××00B
▲4: IICAS0 = 0001×110B
▲5: IICAS0 = 0001××00B
△6: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

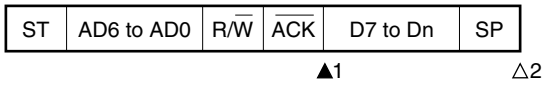
(ii) Extension code



▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 01100010B
Sets LREL0 = 1 by software
△3: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care
n = 6 to 0

(e) When loss occurs due to stop condition during data transfer



▲1: IICAS0 = 10000110B
△2: IICAS0 = 01000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care
n = 6 to 0

16.4 Operation of Serial Interfaces CSI10 and CSI11

Serial interfaces CSI10 and CSI11 can be used in the following two modes.

- Operation stop mode
- 3-wire serial I/O mode

16.4.1 Operation stop mode

Serial communication is not executed in this mode. Therefore, the power consumption can be reduced. In addition, the $\overline{SCK1n}$, SI1n, SO1n, and $\overline{SSI11}$ pins can be used as ordinary I/O port pins in this mode.

(1) Register used

The operation stop mode is set by serial operation mode register 1n (CSIM1n).

To set the operation stop mode, clear bit 7 (CSIE1n) of CSIM1n to 0.

(a) Serial operation mode register 1n (CSIM1n)

CSIM1n can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CSIM1n to 00H.

Remarks 1. 78K0/KA2-L (25, 32-pin products): n = 1
78K0/KB2-L: n = 0
78K0/KC2-L: n = 0, 1

2. The $\overline{SSI11}$ pin is available only in 78K0/KA2-L (25, 32-pin products) and 78K0/KC2-L (48-pin products).

- Serial operation mode register 10 (CSIM10)

Address: FF80H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CSIM10	CSIE10	TRMD10	0	DIR10	0	0	0	CSOT10

CSIE10	Operation control in 3-wire serial I/O mode
0	Disables operation[Note 1] and asynchronously resets the internal circuit[Note 2].

Notes 1. To use P10/$\overline{SCK10}$ and P12/SO10 as general-purpose ports, set CSIM10 in the default status (00H).

2. Bit 0 (CSOT10) of CSIM10 and serial I/O shift register 10 (SIO10) are reset.

<R> **Table 17-2. Flags Corresponding to Interrupt Request Sources (2/2)**

KY 2-L	KA 2-L		KB 2-L	KC2-L			Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
									Register		Register		Register
16 pins	20 pins	25, 32 pins	30 pins	40 pins	44 pins	48 pins							
√	√	√	√	√	√	√	INTAD	ADIF	IF1L	ADMK	MK1L	ADPR	PR1L
–	–	–	–	–	–	√	INTP6	PIF6		PMK6		PPR6	
–	–	–	–	√	√	√	INTRTCI	RTCIIF		RTCIMK		RTCIPR	
√	√	√	√	√	√	√	INTTM51[Note]	TMIF51		TMMK51		TMPR51	
–	–	–	–	√	√	√	INTKR	KRIF		KRMK		KRPR	
–	–	–	–	√	√	√	INTRTC	RTCIF		RTCMK		RTCPR	
–	–	–	–	–	–	√	INTP7	PIF7		PMK7		PPR7	
–	–	–	–	–	√	√	INTP8	PIF8		PMK8		PPR8	
√	√	√	√	√	√	√	INTIICA0	IICAIF0	IF1H	IICAMK0	MK1H	IICAPR0	PR1H
–	–	–	–	–	√	√	INTCSI11	CSIIF11		CSIMK11		CSIPR11	
–	–	–	–	√	√	√	INTP9	PIF9		PMK9		PPR9	
–	–	–	√	√	√	√	INTP10	PIF10		PMK10		PPR10	
–	–	–	√	√	√	√	INTP11	PIF11		PMK11		PPR11	

Note When 8-bit timer/event counter 51 is used in the carrier generator mode, an interrupt is generated upon the timing when the INTTM5H1 signal is generated (refer to **Figure 8-16 Transfer Timing**).

Table 20-2. Hardware Statuses After Reset Acknowledgment (3/4)

Hardware		Status After Reset Acknowledgment Note 1
Clock output controller	Clock output selection register (CKS)	00H
Watchdog timer	Enable register (WDTE)	1AH/9AH Note 2
A/D converter	10-bit A/D conversion result register (ADCR)	0000H
	8-bit A/D conversion result register L (ADCRL)	00H
	8-bit A/D conversion result register H (ADCRH)	00H
	Mode register 0 (ADM0)	00H
	Analog input channel specification register (ADS)	00H
	A/D port configuration register 0 (ADPC0)	00H
	A/D port configuration register 1 (ADPC1)	07H Note 3
Operational amplifier 0 (AMP0, PGA)	Operational amplifier 0 control register (AMP0M)	00H
Operational amplifier 1 (AMP1)	Operational amplifier 1 control register (AMP1M)	00H
Serial interface UART6	Receive buffer register 6 (RXB6)	FFH
	Transmit buffer register 6 (TXB6)	FFH
	Asynchronous serial interface operation mode register 6 (ASIM6)	01H
	Asynchronous serial interface reception error status register 6 (ASIS6)	00H
	Asynchronous serial interface transmission status register 6 (ASIF6)	00H
	Clock selection register 6 (CKSR6)	00H
	Baud rate generator control register 6 (BRGC6)	FFH
	Asynchronous serial interface control register 6 (ASICL6)	16H
	Input switch control register (ISC)	00H
Serial interfaces CSI10, CSI11	Transmit buffer registers 10, 11 (SOTB10, SOTB11)	00H
	Serial I/O shift registers 10, 11 (SIO10, SIO11)	00H
	Serial operation mode registers 10, 11 (CSIM10, CSIM11)	00H
	Serial clock selection registers 10, 11 (CSIC10, CSIC11)	00H
Serial interface IICA	Shift register (IICA)	00H
	Status register 0 (IICS0)	00H
	Flag register 0 (IICF0)	00H
	Control register 0 (IICCTL0)	00H
	Control register 1 (IICCTL1)	00H
	Low-level width setting register (IICWL)	FFH
	High-level width setting register (IICWH)	FFH
	Slave address register 0 (SVA0)	00H
Key interrupt	Key return mode register (KRM)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. The reset value of WDTE is determined by the option byte setting.

<R> **3.** For the 78K0/KA2-L (32-pin products), cleared to 00H.

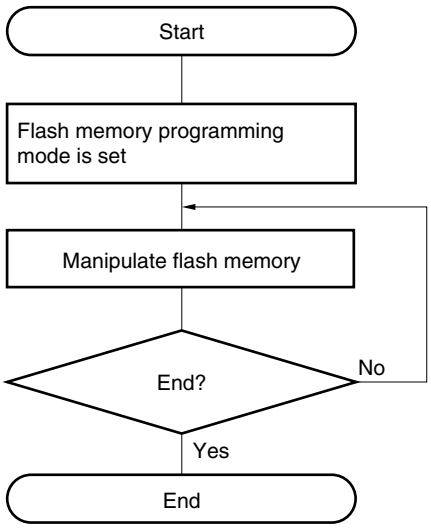
Remark The special function registers (SFRs) mounted depend on the product. Refer to **3.2.3 Special function registers (SFRs)**.

25.5 Programming Method

25.5.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

Figure 25-6. Flash Memory Manipulation Procedure



25.5.2 Flash memory programming mode

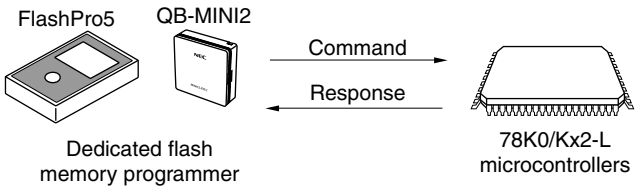
To rewrite the contents of the flash memory by using the dedicated flash memory programmer, set the 78K0/Kx2-L microcontrollers in the flash memory programming mode. The system switches to the flash memory programming mode once the dedicated flash memory programmer is connected and communication starts.

Change the mode by using a jumper when writing the flash memory on-board.

25.5.3 Communication commands

The 78K0/Kx2-L microcontrollers communicate with the dedicated flash memory programmer by using commands. The signals sent from the flash memory programmer to the 78K0/Kx2-L microcontrollers are called commands, and the signals sent from the 78K0/Kx2-L microcontrollers to the dedicated flash memory programmer are called response.

Figure 25-7. Communication Commands

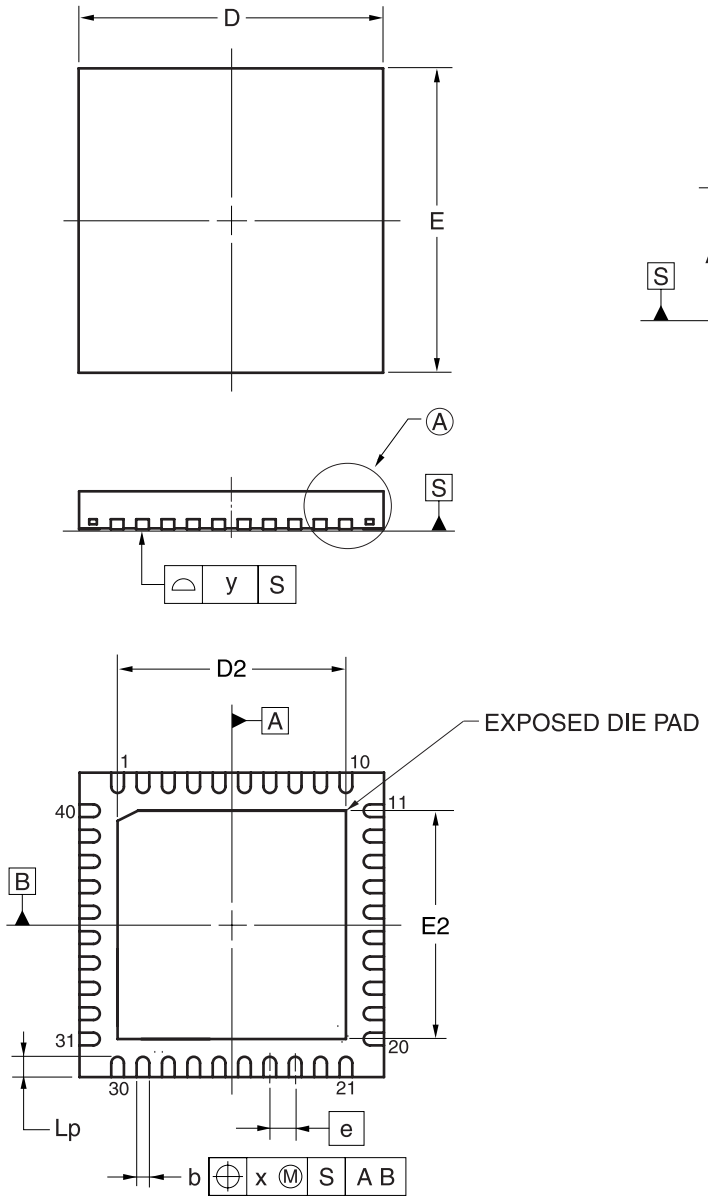


The flash memory control commands of the 78K0/Kx2-L microcontrollers are listed in the table below. All these commands are issued from the programmer and the 78K0/Kx2-L microcontrollers perform processing corresponding to the respective commands.

29.4 78K0/KC2-L

<R>• μPD78F0581K8-4B4-AX, 78F0582K8-4B4-AX, 78F0583K8-4B4-AX, 78F0586K8-4B4-AX, 78F0587K8-4B4-AX, 78F0588K8-4B4-AX

40-PIN PLASTIC WQFN(6x6)



(UNIT:mm)

ITEM	DIMENSIONS
D	6.00±0.05
E	6.00±0.05
D2	4.50±0.05
E2	4.50±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

P40K8-50-4B4-1

(3/4)

Page	Description	Classification
CHAPTER 12 A/D CONVERTER		
p.421	Change of **Table 12-8. Setting Functions of P70/ANI8 to P72/ANI10 Pins**	(d)
p.433	Change of mode name in **Table 12-9. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)**	(c)
CHAPTER 13 OPERATIONAL AMPLIFIERS		
p.435	Change of **Figure 13-1. Block Diagram of Operational Amplifier**	(c)
p.439	Change of **Figure 13-6. Format of Analog Input Channel Specification Register (ADS)**	(c)
p.444	Change of **Table 13-5. Setting Functions of P21/ANI1/AMP0OUT/PGAIN Pin**	(c)
CHAPTER 16 SERIAL INTERFACES CSI10 AND CSI11		
p.573	Change of **(4) Port mode registers 0, 1, 3, 4, 6, 12 (PM0, PM1, PM3, PM4, PM6, PM12)** in **16.3 Registers Controlling Serial Interfaces CSI10 and CSI11**	(d)
p.574	Addition of **Figure 16-9. Format of Port Mode Register 0 (PM0)**	(d)
p.574	Addition of **Figure 16-11. Format of Port Mode Register 3 (PM3)**	(d)
CHAPTER 17 INTERRUPT FUNCTIONS		
pp.592, 593	Change of **Table 17-1. Interrupt Source List**	(d)
CHAPTER 19 STANDBY FUNCTION		
p.649	Addition of **Caution** in **Table 19-3. Operating Statuses in STOP Mode**	(c)
CHAPTER 20 RESET FUNCTION		
pp.662, 663	Change of **Note** in **Table 20-2. Hardware Statuses After Reset Acknowledgment**	(b)
p.664	Change of **Table 20-3. RESF Status When Reset Request Is Generated**	(b)
CHAPTER 21 POWER-ON-CLEAR CIRCUIT		
p.668	Change of **Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2/2)**	(b)
CHAPTER 22 LOW-VOLTAGE DETECTOR		
p.673	Change of **Note 1** in **Figure 22-2. Format of Low-Voltage Detection Register (LVIM)**	(b)
p.675	Change of **Note** in **Figure 22-3. Format of Low-Voltage Detection Level Select Register (LVIS)**	(b)
p.676	Change of **Remark 1** in **22.4 (1) Used as reset (LVIMD = 1)**	(b)
p.680	Change of description in **22.4.1 (1) (b) When LVI default start function enabled is set (LVISTART = 1)**	(b)
p.680	Change of **Figure 22-6. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVISTART = 1)**	(b)
p.685	Change of description in **22.4.2 (1) (b) When LVI default start function enabled is set (LVISTART = 1)**	(b)
p.685	Change of **Figure 22-9. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 0, Option Byte: LVISTART = 1)**	(b)
CHAPTER 23 REGULATOR		
p.691	Change of **(1) Regulator mode control register (RMC)** in **23.2 Register Controlling Regulator**	(b)
CHAPTER 24 OPTION BYTE		
p.694	Change of **(4) 0083H/1083H** in **24.1 Functions of Option Bytes**	(b)
p.696	Change of description of LVISTART bit in **Figure 24-1. Format of Option Byte (2/3)**	(b)
p.697	Change of **Figure 24-1. Format of Option Byte (3/3)**	(b)
p.698	Change of description example of software in **24.2 Format of Option Byte**	(b)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents