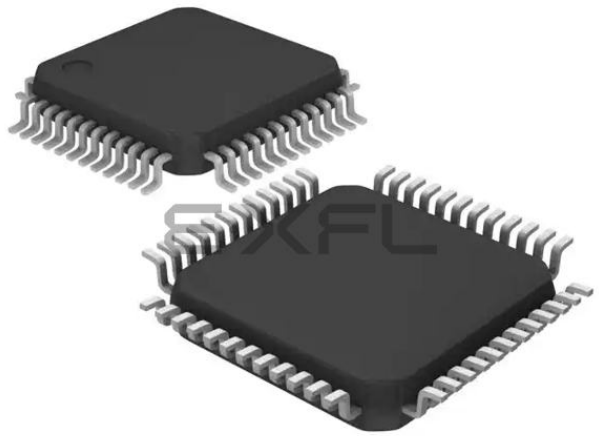


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

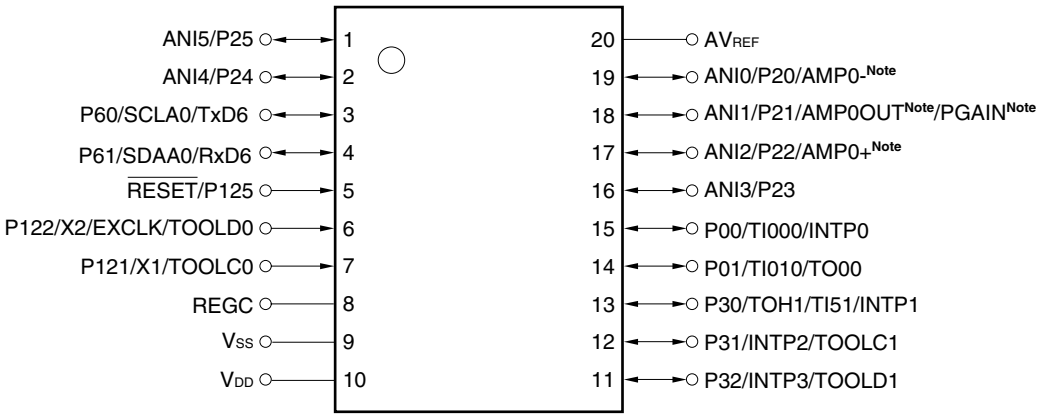
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0583ga-gam-ax

1.3.2 78K0/KA2-L

(1) 20-pin plastic SSOP (7.62 mm (300))



AMP0-Note, AMP0+Note :	Amplifier Input	P121, P122, P125 :	Port 12
AMP0OUTNote :	Amplifier Output	REGC :	Regulator Capacitance
PGAINNote :	Programmable Gain	$\overline{\text{RESET}}$:	Reset
	Amplifier Input	RxD6 :	Receive Data
ANI0 to ANI5 :	Analog Input	SCLA0 :	Serial Clock Input/Output
AVREF :	Analog Reference	SDAA0 :	Serial Data Input/Output
	Voltage	TI000, TI010, TI51 :	Timer Input
EXCLK :	External Clock Input	TO00, TOH1 :	Timer Output
	(Main System Clock)	TOOLC0, TOOLC1 :	Clock Input for Tool
INTP0 to INTP3 :	External Interrupt	TOOLD0, TOOLD1 :	Data Input/Output for Tool
	Input	TxD6 :	Transmit Data
P00, P01 :	Port 0	VDD :	Power Supply
P20 to P25 :	Port 2	VSS :	Ground
P30 to P32 :	Port 3	X1, X2 :	Crystal Oscillator
P60, P61 :	Port 6		(Main System Clock)

Note μPD78F0565, 78F0566, 78F0567 (products with operational amplifier) only

Cautions 1. VSS functions alternately as the ground potential of the A/D converter. Be sure to connect VSS to a stabilized GND (= 0 V).

2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

3. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, and ANI3/P23 to ANI5/P25 are set in the analog input mode after release of reset.

4. $\overline{\text{RESET}}$/P125 immediately after release of reset is set in the external reset input.

(g) SO11

This is a serial data output pin for serial interface CSI11.

(h) INTP8 to INTP11

These are external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

2.2.7 P70 to P75 (port 7)

P70 to P75 function as an I/O port. These pins also function as pins for A/D converter analog input and key interrupt input pins.

<R>

78K0/KY2-L (μPD78F057x)	78K0/KA2-L (μPD78F056x)		78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)	
16 Pins	20, 25 Pins	32 Pins	30 Pins	40, 44 Pins	48 Pins
–	–	P70/ANI8	–	P70/KR0	P70/KR0
–	–	P71/ANI9	–	P71/KR1	P71/KR1
–	–	P72/ANI10	–	P72/KR2	P72/KR2
–	–	–	–	P73/KR3	P73/KR3
–	–	–	–	–	P74/KR4
–	–	–	–	–	P75/KR5

The following operation modes can be specified in 1-bit units.

(1) Port mode

P70 to P75 function as an I/O port. P70 to P75 can be set to input or output port in 1-bit units using port mode register 7 (PM7). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 7 (PU7) in 78K0/KC2-L.

(2) Control mode

P70 to P75 function as pins for A/D converter analog input and key interrupt input pins.

(a) ANI8 to ANI10

These are the A/D converter analog input pins. When using this pin as analog input pin, refer to **(5) ANI0/P20 to ANI7/P27, ANI8/P10 to ANI10/P12, and ANI8/P70 to ANI10/P72** in **12.6 Cautions for A/D Converter**.

(b) KR0 to KR5

These are the key interrupt input pins

Table 3-6. Special Function Register List: 78K0/KY2-L (2/4)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF26H	PM6	1	1	1	1	1	1	PM61	PM60	R/W	√	√	–	FFH	167, 463, 504, 573
FF27H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF28H	ADM0	<ADCS>	0	FR2	FR1	FR0	LV1	LV0	<ADCE>	R/W	√	√	–	00H	405
FF29H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF2AH	POM6	0	0	0	0	0	0	POM61	POM60	R/W	√	√	–	00H	180, 464, 504
FF2BH	FPCTL	0	0	0	0	0	0	0	<FLMD PUP>	R/W	√	√	–	00H	713
FF2CH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF2DH	RSTMASK	0	0	RSTM	0	0	0	0	0	R/W	√	√	–	00H	180
FF2EH	ADPC0	0	0	0	0	ADPCS3	ADPCS2	ADPCS1	ADPCS0	R/W	√	√	–	00H	181, 413, 437
FF2FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF30H	PU0	0	0	0	0	0	0	PU01	PU00	R/W	√	√	–	00H	177
FF31H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF32H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF33H	PU3	0	0	0	0	0	0	0	PU30	R/W	√	√	–	00H	177
FF34H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF35H															
FF36H	PU6	0	0	0	0	0	0	PU61	PU60	R/W	√	√	–	00H	177
FF37H to FF3BH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF3CH	PU12	0	0	PU125	0	0	0	0	0	R/W	√	√	–	20H	177
FF3DH	RMC	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	691
FF3EH	PIM6	0	0	0	0	0	0	PIM61	PIM60	R/W	√	√	–	00H	179, 503
FF3FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF40H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF41H	CR51	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	317
FF42H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF43H	TMC51	<TCE51>	0	0	0	0	0	0	0	R/W	√	√	–	00H	320
FF44H to FF47H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF48H	EGPCTL0	0	0	0	0	0	0	EGP1	EGP0	R/W	√	√	–	00H	619
FF49H	EGNCTL0	0	0	0	0	0	0	EGN1	EGN0	R/W	√	√	–	00H	619
FF4AH to FF4EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF4FH	ISC	0	0	0	0	0	0	ISC1	ISC0	R/W	√	√	–	00H	463
FF50H	ASIM6	<POWER6>	<TXE6>	<RXE6>	PS61	PS60	CL6	SL6	ISRM6	R/W	√	√	–	01H	454

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

3.4.9 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call and return instructions are executed or the register is saved/reset upon generation of an interrupt request.

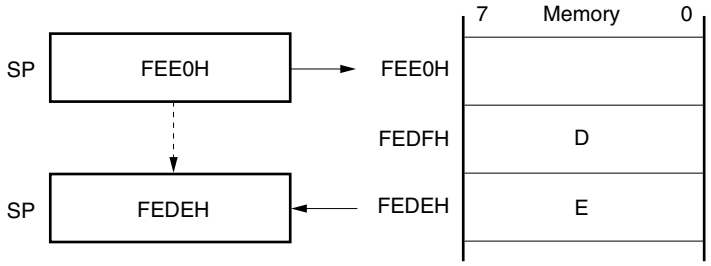
With stack addressing, only the internal high-speed RAM area can be accessed.

[Description example]

PUSH DE; when saving DE register

Operation code	1	0	1	1	0	1	0	1

[Illustration]



4.2.2 Port 1

<R>

78K0/KY2-L (μPD78F055x)	78K0/KA2-L (μPD78F056x)	78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)
16 Pins	20, 25, 32 Pins	30 Pins	40, 44, 48 Pins
–	–	P10/ANI8/AMP1-Note/$\overline{SCK10}$	P10/ANI8/AMP1-Note/$\overline{SCK10}$
–	–	P11/ANI9/AMP1OUTNote/SI10	P11/ANI9/AMP1OUTNote/SI10
–	–	P12/ANI10/AMP1+Note/SO10	P12/ANI10/AMP1+Note/SO10
–	–	P13/TxD6	P13/TxD6
–	–	P14/RxD6	P14/RxD6
–	–	P15/TOH0	P15/TOH0
–	–	P16/TOH1/INTP5	P16/TOH1/INTP5
–	–	P17/TI50/TO50	P17/TI50/TO50

Note Products with operational amplifier only

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P17 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

This port can also be used for A/D converter analog input, operational amplifier I/O, external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

When using P10/ANI8/AMP1-, P11/ANI9/AMP1OUT, or P12/ANI10/AMP1+, set the registers according to the pin function to be used (refer to **Tables 4-8** and **4-9**).

Table 4-8. Setting Functions of P10/ANI8/AMP1-, P12/ANI10/AMP1+ Pins

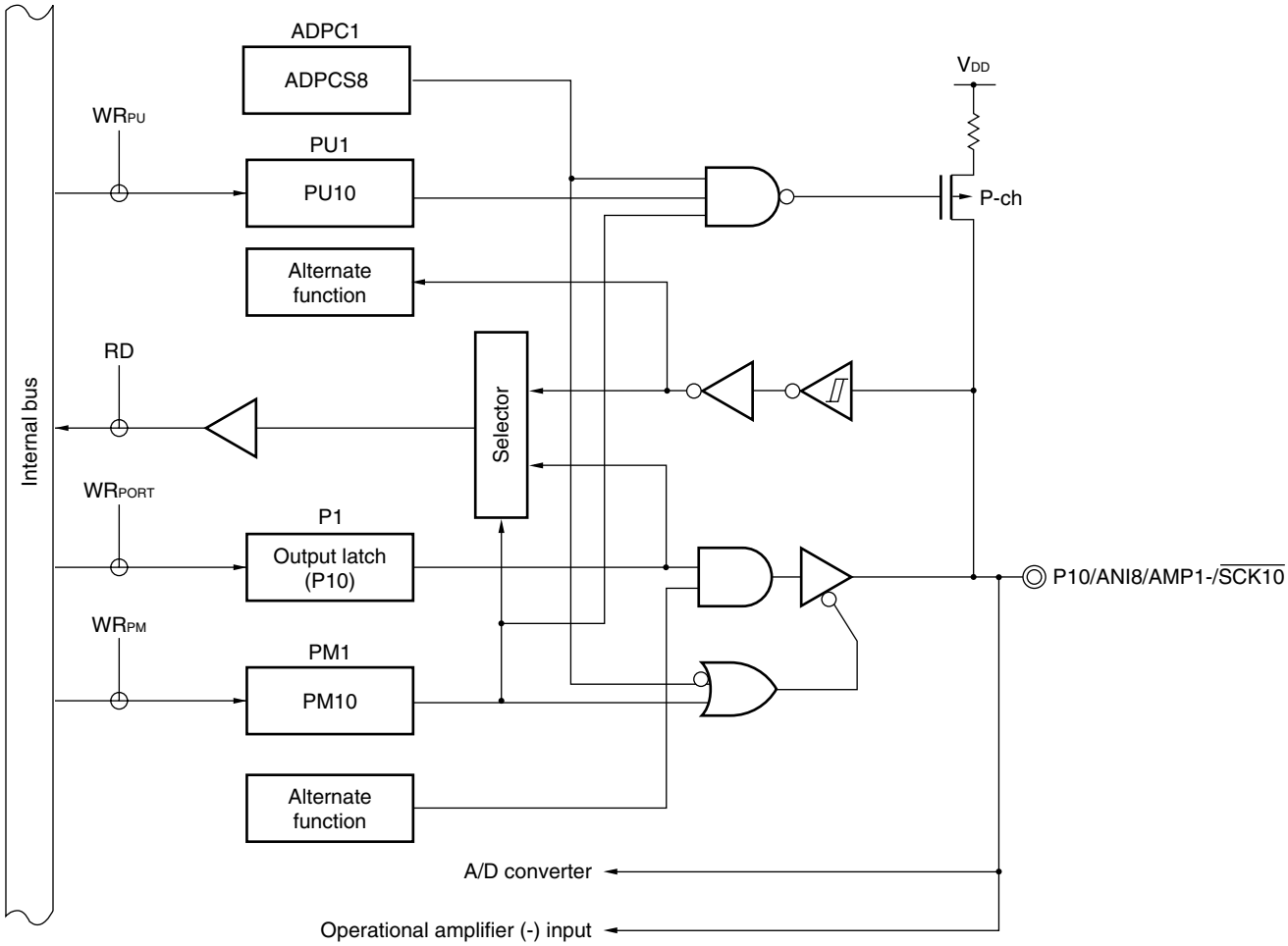
ADPC1 Register	PM1 Register	OPAMP1E bit	ADS Register (n = 8, 10)	P10/ANI8/AMP1-, P12/ANI10/AMP1+ Pins
Digital I/O selection	Input mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital input
	Output mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital output
Analog input selection	Input mode	0	Selects ANIn.	Analog input (to be converted into digital signals)
			Does not select ANIn.	Analog input (not to be converted into digital signals)
		1	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Operational amplifier 1 input
	Output mode	–	–	Setting prohibited

Remark ADPC1: A/D port configuration register 1
PM1: Port mode register 1
OPAMP1E: Bit 7 of operational amplifier 1 control register (AMP1M)
ADS: Analog input channel specification register

<R>

Figure 4-4. Block Diagram of P10 (2/2)

(2) Products with operational amplifier of 78K0/KB2-L and 78K0/KC2-L

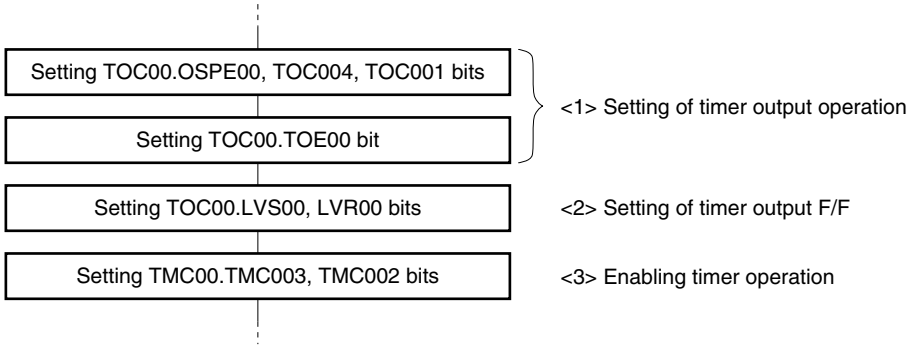


P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
ADPC1: A/D port configuration register 1
RD: Read signal
WR××: Write signal

(2) Setting LVS00 and LVR00

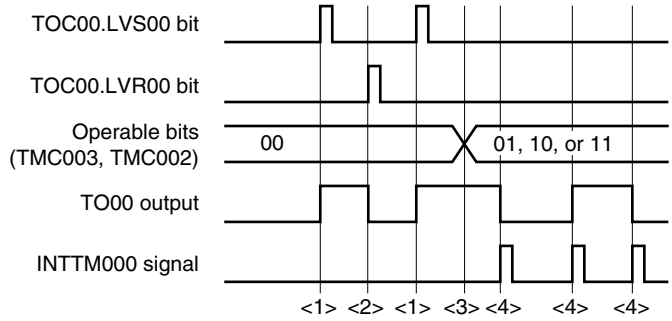
Set LVS00 and LVR00 using the following procedure.

Figure 6-54. Example of Flow for Setting LVS00 and LVR00 Bits



Caution Be sure to set LVS00 and LVR00 following steps <1>, <2>, and <3> above.
Step <2> can be performed after <1> and before <3>.

Figure 6-55. Timing Example of LVR00 and LVS00



<1> The TO00 output goes high when LVS00 and LVR00 = 10.

<2> The TO00 output goes low when LVS00 and LVR00 = 01 (the pin output remains unchanged from the high level even if LVS00 and LVR00 are cleared to 00).

<3> The timer starts operating when TMC003 and TMC002 are set to 01, 10, or 11. Because LVS00 and LVR00 were set to 10 before the operation was started, the TO00 output starts from the high level. After the timer starts operating, setting LVS00 and LVR00 is prohibited until TMC003 and TMC002 = 00 (disabling the timer operation).

<4> The TO00 output level is inverted each time an interrupt signal (INTTM000) is generated.

Figure 10-1. Block Diagram of Real-Time Counter

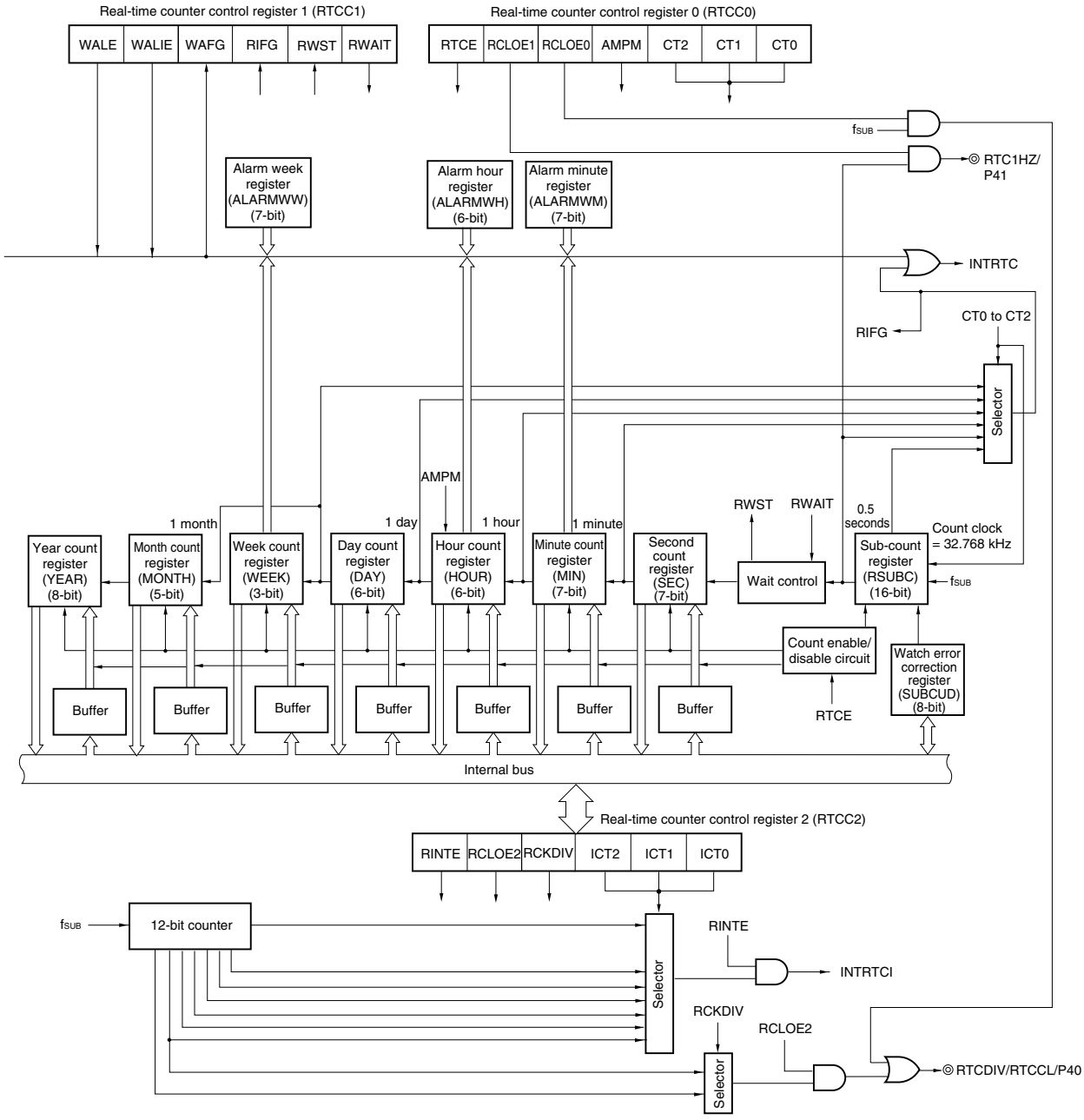


Figure 14-12. Format of Port Mode Register 1 (PM1)

Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

PM1n	P1n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 1 (PM1) of the 78K0/KB2-L and 78K0/KC2-L.

Figure 14-13. Format of Port Mode Register 6 (PM6)

Address: FF26H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM6	1	1	1	1	1	1	PM61	PM60

PM6n	P6n pin I/O mode selection (n = 0, 1)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 6 (PM6) of the 78K0/KY2-L and 78K0/KA2-L.

(9) Port output mode register 6 (POM6)

This register sets the output mode of P60 and P61 in 1-bit units.

In the 78K0/KY2-L and 78K0/KA2-L, clear POM60 to 0 when using the P60/TxD6/SCLA0 pin as the data output of serial interface UART6.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 14-14. Format of Port Output Mode Register 6 (POM6)

Address: FF2AH After reset: 00H R/W

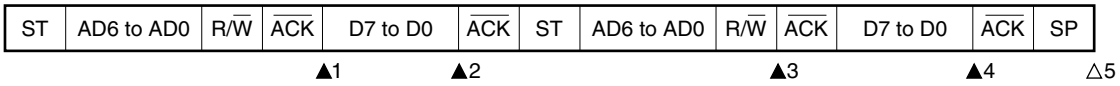
Symbol	7	6	5	4	3	2	1	0
POM6	0	0	0	0	0	0	POM61	POM60

POM6n	P6n pin output mode selection (n = 0 and 1)
0	Normal output (CMOS output) mode
1	N-ch open drain output (V_{DD} tolerance) mode

Remark The figure shown above presents the format of port output mode register 6 (POM6) of the 78K0/KY2-L and 78K0/KA2-L.

(c) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

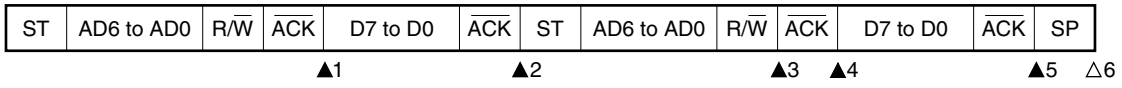
(i) When WTIM0 = 0 (after restart, does not match address (= extension code))



▲1: IICAS0 = 0001×110B
▲2: IICAS0 = 0001×000B
▲3: IICAS0 = 0010×010B
▲4: IICAS0 = 0010×000B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, does not match address (= extension code))

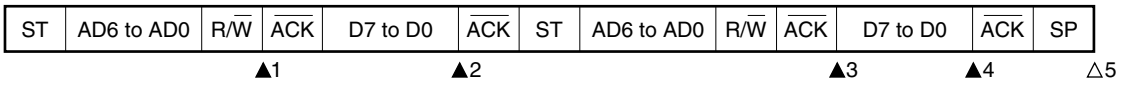


▲1: IICAS0 = 0001×110B
▲2: IICAS0 = 0001××00B
▲3: IICAS0 = 0010×010B
▲4: IICAS0 = 0010×110B
▲5: IICAS0 = 0010××00B
△6: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(b) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

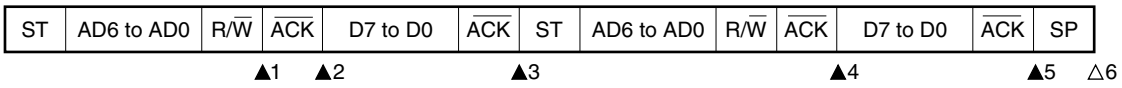
(i) When WTIM0 = 0 (after restart, matches SVA0)



▲1: IICAS0 = 0010×010B
▲2: IICAS0 = 0010×000B
▲3: IICAS0 = 0001×110B
▲4: IICAS0 = 0001×000B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, matches SVA0)

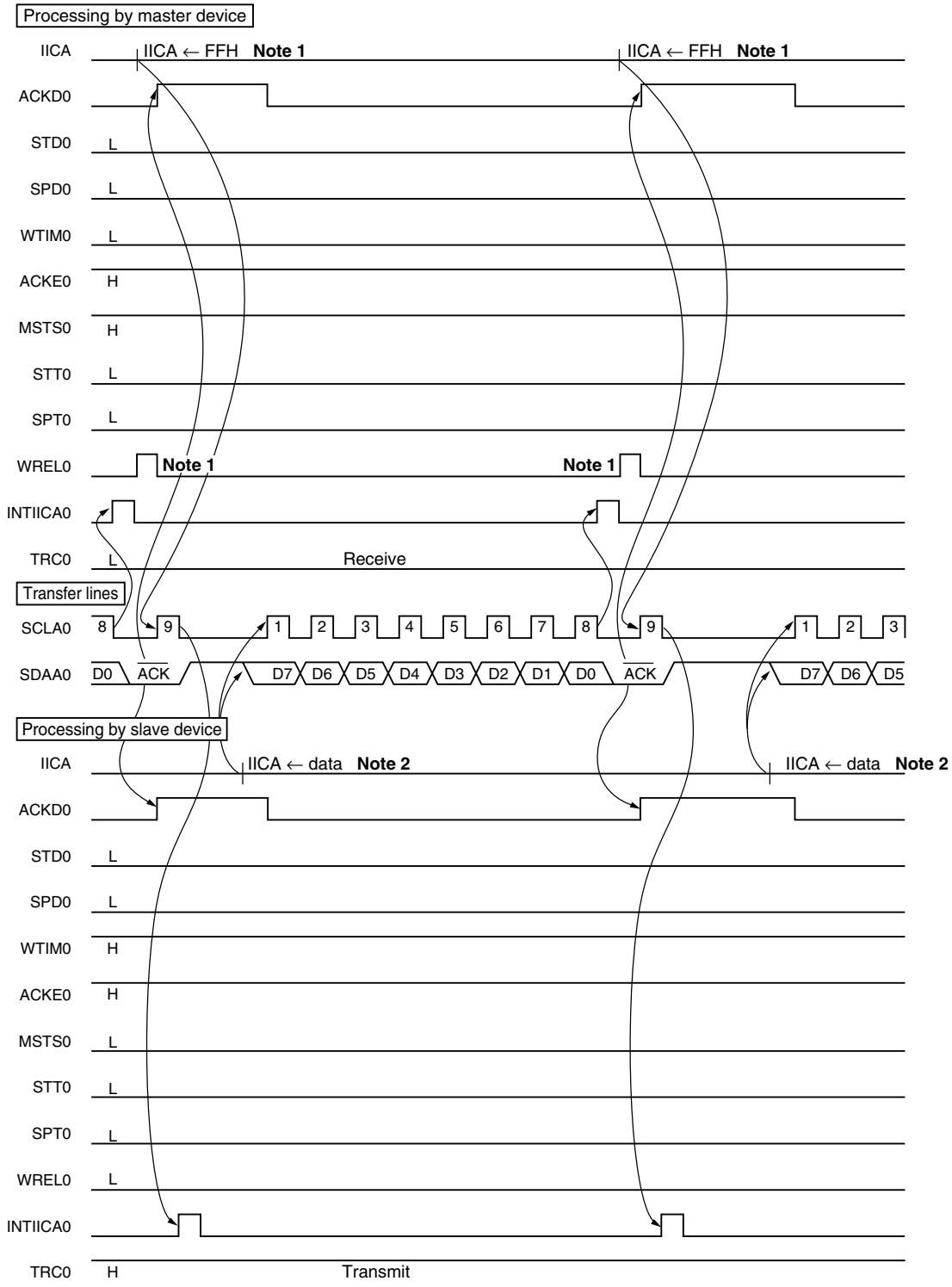


▲1: IICAS0 = 0010×010B
▲2: IICAS0 = 0010×110B
▲3: IICAS0 = 0010××00B
▲4: IICAS0 = 0001×110B
▲5: IICAS0 = 0001××00B
△6: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Figure 15-34. Example of Slave to Master Communication
(When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/3)

(2) Data



Notes 1. To cancel master wait, write “FFH” to IICA or set WREL0.

2. Write data to IICA, not setting WREL0, in order to cancel a wait state during slave transmission.

(4) Port mode registers 0, 1, 3, 4, 6, 12 (PM0, PM1, PM3, PM4, PM6, PM12)

These registers set input/output of ports 0, 1, 3, 4, 6, and 12 in 1-bit units.

<R> • 78K0/KA2-L (25, 32-pin products)

When using P35/SCK11 as the clock output pin of the serial interface, clear PM35 to 0, and set the output latches of P35 to 1.

When using P37/SO11 as the data output pin of the serial interface, clear PM37 and the output latches of P37 to 0.

When using P35/SCK10 as the clock input pins of the serial interface, P36/SI11 as the data input pins of the serial interface, and P02/SSI11/INTP5 as the chip select input pin of the serial interface, set PM35, PM36, and PM02 to 1. At this time, the output latches of P35, P36, and P02 may be 0 or 1.

• 78K0/KB2-L

When using P10/SCK10 as the clock output pin of the serial interface, clear PM10 to 0, and set the output latches of P10 to 1.

When using P12/SO10 as the data output pin of the serial interface, clear PM12 and the output latches of P12 to 0.

When using P10/SCK10 as the clock input pin of the serial interface and P11/SI10 as the data input pin of the serial interface, set PM10 and PM11 to 1. At this time, the output latches of P10 and P11 may be 0 or 1.

• 78K0/KC2-L (when CSISEL = 0)

When using P10/SCK10 and P60/SCK11/SCLA0 as the clock output pins of the serial interface, clear PM10 and PM60 to 0, and set the output latches of P10 and P60 to 1.

When using P12/SO10 and P62/SO11 as the data output pins of the serial interface, clear PM12 and PM62 and the output latches of P12 and P62 to 0.

When using P10/SCK10 and P60/SCK11/SCLA0 as the clock input pins of the serial interface, P11/SI10 and P61/SI11/SDAA0 as the data input pins of the serial interface, and P42/SSI11/PCL/INTP6 as the chip select input pin of the serial interface, set PM10, PM60, PM11, PM61, and PM42 to 1. At this time, the output latches of P10, P60, P11, P61, and P42 may be 0 or 1.

• 78K0/KC2-L (when CSISEL = 1)

When using P10/SCK10 and P40/SCK11/RTCCL/RTCDIV as the clock output pins of the serial interface, clear PM10 and PM40 to 0, and set the output latches of P10 and P40 to 1.

When using P12/SO10 and P120/SO11/INTP0/EXLVI as the data output pins of the serial interface, clear PM12 and PM120 and the output latches of P12 and P120 to 0.

When using P10/SCK10 and P40/SCK11/RTCCL/RTCDIV as the clock input pins of the serial interface, P11/SI10 and P41/SI11/RTC1HZ as the data input pins of the serial interface, and P42/SSI11/PCL/INTP6 as the chip select input pin of the serial interface, set PM10, PM40, PM11, PM41, and PM42 to 1. At this time, the output latches of P10, P40, P11, P41, and P42 may be 0 or 1.

Remark The SSI11 pin is available only in 78K0/KA2-L (25, 32-pin products) and 78K0/KC2-L(48-pin products).

Table 17-3. Ports Corresponding to EGPn and EGNn (2/3)

(e) 78K0/KB2-L

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P120	INTP0
EGP1	EGN1	P30	INTP1
EGP2	EGN2	P31	INTP2
EGP3	EGN3	P32	INTP3
EGP4	EGN4	P33	INTP4
EGP5	EGN5	P16	INTP5
EGP10	EGN10	P61	INTP10
EGP11	EGN11	P60	INTP11

<R> **(f) 78K0/KC2-L (40-pin products)**

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P120	INTP0
EGP1	EGN1	P30	INTP1
EGP2	EGN2	P31	INTP2
EGP3	EGN3	P32	INTP3
EGP4	EGN4	P33	INTP4
EGP5	EGN5	P16	INTP5
EGP9	EGN9	P62	INTP9
EGP10	EGN10	P61	INTP10
EGP11	EGN11	P60	INTP11

Caution Select the port mode by clearing EGPn and EGNn to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0 to 5, 10, 11: 78K0/KB2-L
n = 0 to 5, 9 to 11: 78K0/KC2-L (40-pin products)

Figure 19-2. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection	
				fx = 10 MHz
0	0	1	2^{11}/fx	204.8 μs
0	1	0	2^{13}/fx	819.2 μs
0	1	1	2^{14}/fx	1.64 ms
1	0	0	2^{15}/fx	3.27 ms
1	0	1	2^{16}/fx	6.55 ms
Other than above			Setting prohibited	

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

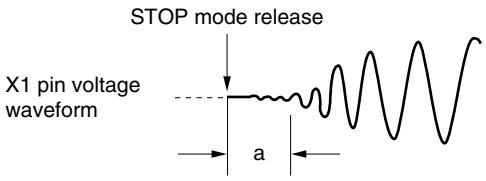
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

19.2 Standby Function Operation

19.2.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock, internal high-speed oscillation clock, or subsystem clock[Note]. The operating statuses in the HALT mode are shown below.

Note 78K0/KC2-L only

Table 25-9. Processing Time for Each Command When PG-FP5 Is Used (Reference) (3/3)

(2) 78K0/KB2-L, 78K0/KC2-L (2/2)

(b) Products with internal ROMs of the 16 KB: μPD78F0572, 78F0577, 78F0582, 78F0587

Command of PG-FP5	Port: UART-Internal-OSC (Internal high-speed oscillation clock (f_{IH}: 8 MHz (typ.)), Speed: 500,000 bps
Signature	0.5 s (typ.)
Blankcheck	1 s (typ.)
Erase	1 s (typ.)
Program	2.5 s (typ.)
Verify	1.5 s (typ.)
E.P.V	2.5 s (typ.)
Checksum	1 s (typ.)
Security	1 s (typ.)

(c) Products with internal ROMs of the 32 KB: μPD78F0573, 78F0578, 78F0583, 78F0588

Command of PG-FP5	Port: UART-Internal-OSC (Internal high-speed oscillation clock (f_{IH}: 8 MHz (typ.)), Speed: 500,000 bps
Signature	0.5 s (typ.)
Blankcheck	1 s (typ.)
Erase	1 s (typ.)
Program	4.5 s (typ.)
Verify	3 s (typ.)
E.P.V	4.5 s (typ.)
Checksum	1 s (typ.)
Security	1 s (typ.)

Caution When executing boot swapping, do not use the E.P.V. command with the dedicated flash memory programmer.

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First Operand \ Second Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruction					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

<R> **(2) Non-port functions**

Port		78K0/KY2-L	78K0/KA2-L			78K0/KB2-L	78K0/KC2-L		
		16 Pins	20 Pins	25 Pins	32 Pins	30 Pins	40 Pins	44 Pins	48 Pins
Power supply, ground		V_{DD}, V_{SS}, AV_{REF}				V_{DD}, V_{SS}, AV_{REF}, AV_{SS}			
Regulator		REGC							
Reset		$\overline{\text{RESET}}$							
Clock oscillation		X1, X2, EXCLK					X1, X2, EXCLK, XT1, XT2, EXCLKS		
Interrupt		INTP0, INTP1	INTP0 to INTP3	INTP0, INTP2 to INTP5		INTP0 to INTP5, INTP10, INTP11	INTP0 to INTP5, INTP9 to INTP11	INTP0 to INTP5, INTP8 to INTP11	INTP0 to INTP11
Key interrupt		–					KR0 to KR3		KR0 to KR5
Timer	TM00	TI000, TI010, TO00		TI000	(TI000) TI010, TO00	TI000, TI010, TO00			
	TM5x	TI51		(TI51)	–	TI50, TO50, TI51, TO51			
	TMHx	TOH1		(TOH1)		TOH0, TOH1			
	RTC	–						RTC1HZ, RTCCL, RTCDIV	
Serial interface	UART6	RxD6, TxD6							
	IICA	SCLA0, SDAA0							
	CSI10	–				$\overline{\text{SCK10}}$, SI10, SO10			
	CSI11	–		$\overline{\text{SCK11}}$, SI11, SO11, $\overline{\text{SSI11}}$		–	$\overline{\text{SCK11}}$, SI11, SO11		$\overline{\text{SCK11}}$, SI11, SO11, $\overline{\text{SSI11}}$
A/D converter		ANI0 to ANI3	ANI0 to ANI5	ANI0 to ANI6	ANI0 to ANI10	ANI0 to ANI3, ANI8 to ANI10	ANI0 to ANI6, ANI8 to ANI10	ANI0 to ANI10	
Operational amplifier[Note]		AMP0+, AMP0-, AMP0OUT, PGAIN				AMP0+, AMP0-, AMP0OUT, PGAIN, AMP1+, AMP1-, AMP1OUT			
Clock output		–							PCL
Low-voltage detector (LVI)		–				EXLVI			
On-chip debug function		TOOLC0, TOOLD0	TOOLC0, TOOLC1, TOOLD0, TOOLD1						

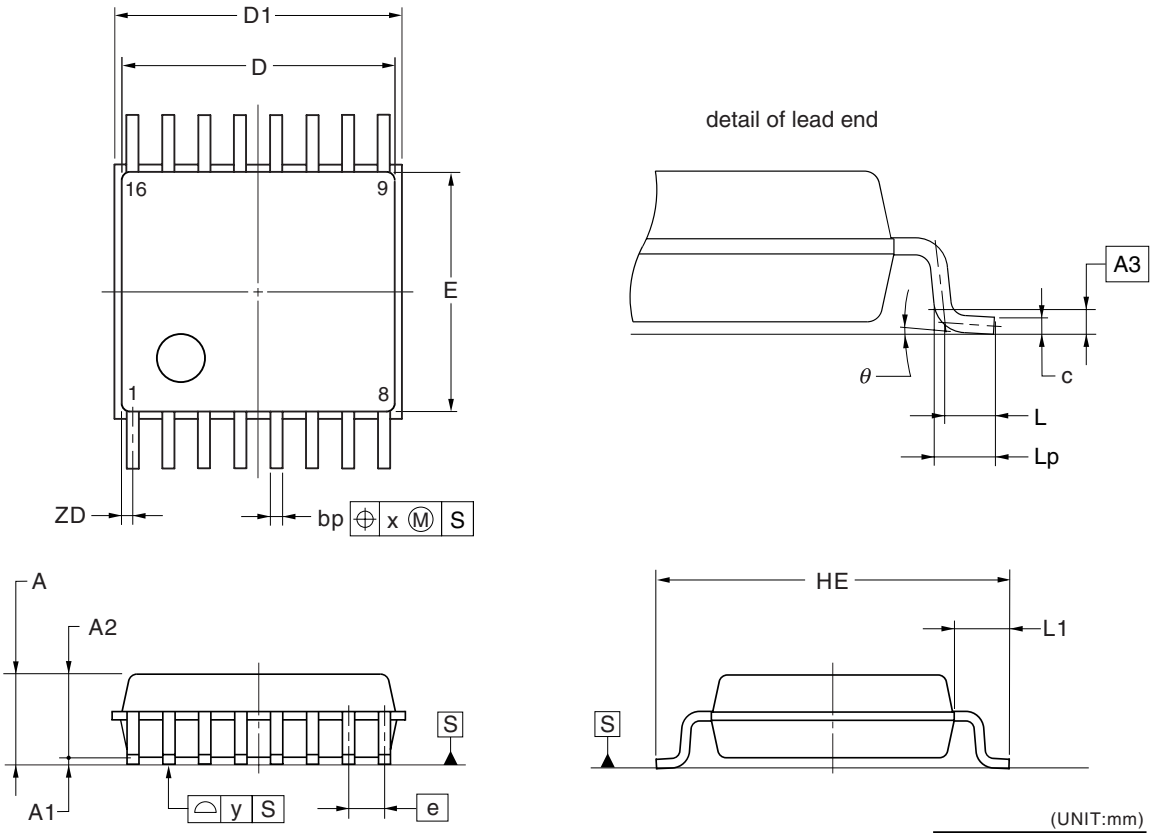
Note Products with operational amplifier only.

CHAPTER 29 PACKAGE DRAWINGS

29.1 78K0/KY2-L

- μPD78F0550MA-FAA-AX, 78F0551MA-FAA-AX, 78F0552MA-FAA-AX, 78F0555MA-FAA-AX, 78F0556MA-FAA-AX, 78F0557MA-FAA-AX

16-PIN PLASTIC SSOP (4.4x5.0)



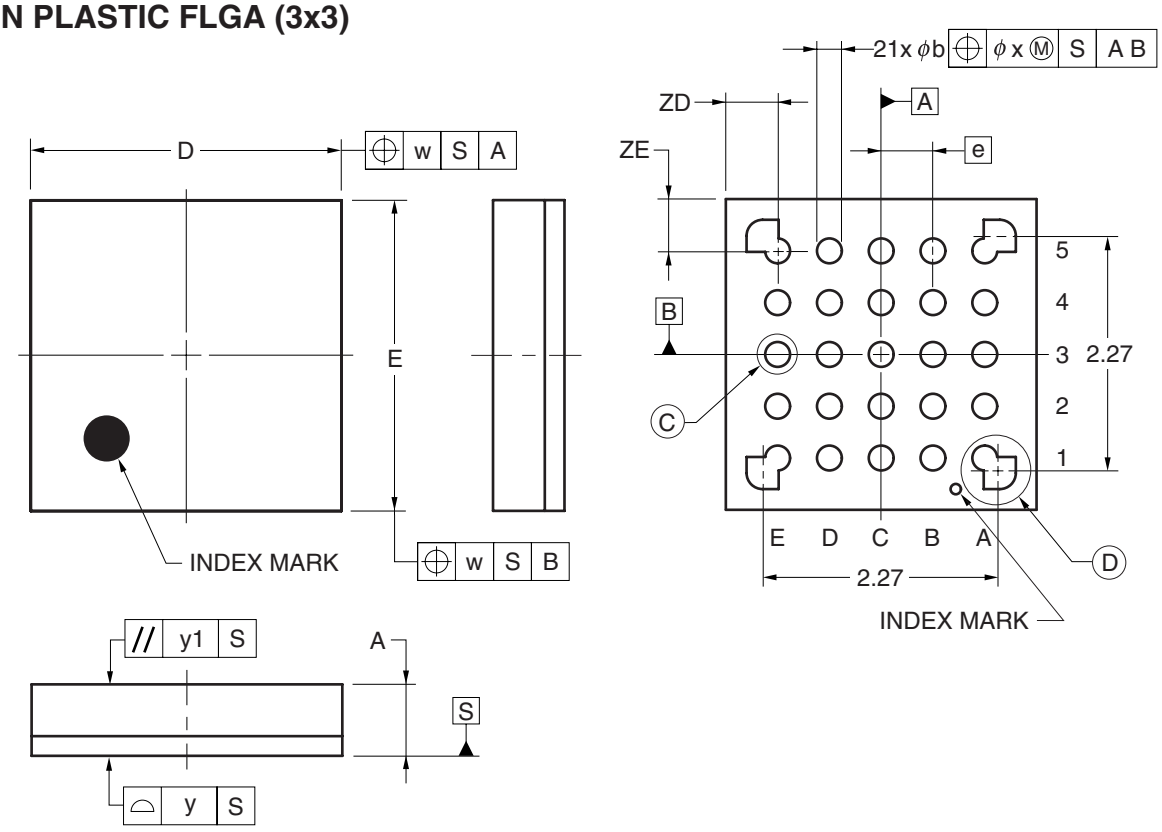
(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.15
D1	5.20±0.15
E	4.40±0.20
HE	6.40±0.20
A	1.725 MAX.
A1	0.125±0.05
A2	1.50
A3	0.25
e	0.65
bp	$0.22^{+0.08}_{-0.07}$
c	$0.15^{+0.03}_{-0.04}$
L	0.50
Lp	0.60±0.10
L1	1.00±0.20
x	0.13
y	0.10
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
ZD	0.325

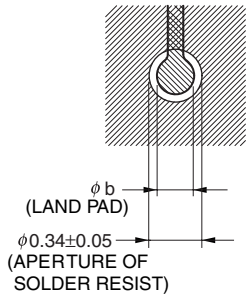
P16MA-65-FAA

<R> • μPD78F0560FC-2N2-A, 78F0561FC-2N2-A, 78F0562FC-2N2-A, 78F0565FC-2N2-A, 78F0566FC-2N2-A, 78F0567FC-2N2-A

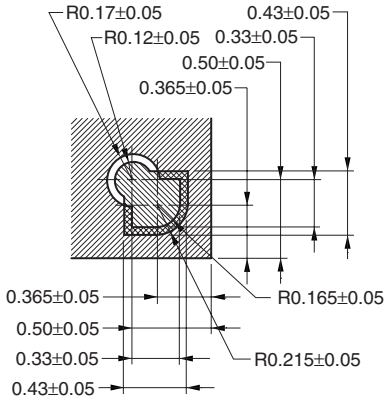
25-PIN PLASTIC FLGA (3x3)



DETAIL OF Ⓒ PART



DETAIL OF Ⓓ PART



(UNIT:mm)

ITEM	DIMENSIONS
D	3.00±0.10
E	3.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

P25FC-50-2N2