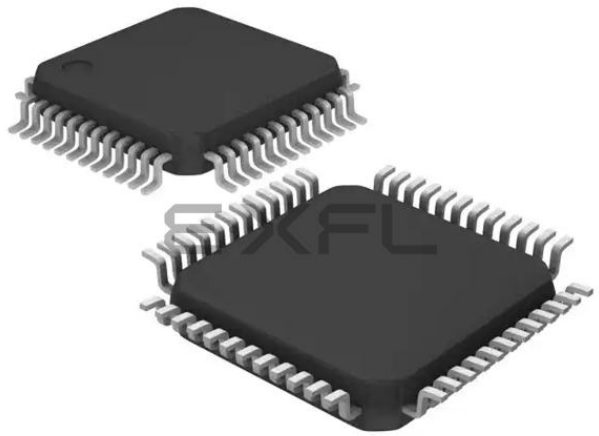
Renesas Electronics America Inc - UPD78F0586GA-GAM-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0586ga-gam-ax

○ Timer

- 16-bit timer/event counter … PPG output, capture input, external event counter input
- 8-bit timer H … PWM output
- 8-bit timer/event counter 5 … PWM output, external event counter input
- Watchdog timer … Operable with low-speed internal oscillation clock
- Real-time counter … Available to count up in year, month, week, day, hour, minute, and second units

Item / Products	16-bit timer/event counter	8-bit timer	Watchdog timer	Real-time counter
78K0/KY2-L (16 pins)	1 ch	Timer H: 1 ch Timer 5: 1 ch	1 ch	–
78K0/KA2-L (20 pins)				
<R> 78K0/KA2-L (25 pins)				
<R> 78K0/KA2-L (32 pins)				
78K0/KB2-L (30 pins)		Timer H: 2 ch Timer 5: 2 ch		
<R> 78K0/KC2-L (40 pins)				1 ch
78K0/KC2-L (44 pins)				
78K0/KC2-L (48 pins)				

○ Serial interface

- UART … Asynchronous 2-wire serial interface
- IICA … Clock synchronous 2-wire serial interface, multimaster supported, standby can be released upon address match in slave mode
- CSI … Clock synchronous 3-wire serial interface

Item / Products	UART	IIC	CSI
78K0/KY2-L (16 pins)	1 ch	1 ch	–
78K0/KA2-L (20 pins)			
<R> 78K0/KA2-L (25 pins)			1 ch (CSI11[Note])
<R> 78K0/KA2-L (32 pins)			
78K0/KB2-L (30 pins)			1 ch (CSI10)
<R> 78K0/KC2-L (40 pins)			2 ch (CSI10, CSI11)
78K0/KC2-L (44 pins)			
78K0/KC2-L (48 pins)			2 ch (CSI10, CSI11[Note])

Note Can control by an enabled signal, when using CSI11 in the slave mode.

○ 10-bit resolution A/D conversion

- 78K0/KY2-L: 4 ch
- <R> 78K0/KA2-L (20 pins): 6 ch, 78K0/KA2-L (25 pins): 7 ch
- <R> 78K0/KA2-L (32 pins): 11 ch
- 78K0/KB2-L: 7 ch
- <R> 78K0/KC2-L (40 pins): 10 ch, 78K0/KC2-L (44 pins, 48 pins): 11 ch

○ Operational amplifier (products with operational amplifier only)

- 78K0/KY2-L, 78K0/KA2-L: 1 ch
- 78K0/KB2-L, 78K0/KC2-L: 2 ch

(g) SO11

This is a serial data output pin for serial interface CSI11.

(h) INTP8 to INTP11

These are external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

2.2.7 P70 to P75 (port 7)

P70 to P75 function as an I/O port. These pins also function as pins for A/D converter analog input and key interrupt input pins.

<R>

78K0/KY2-L (μPD78F057x)	78K0/KA2-L (μPD78F056x)		78K0/KB2-L (μPD78F057x)	78K0/KC2-L (μPD78F058x)	
16 Pins	20, 25 Pins	32 Pins	30 Pins	40, 44 Pins	48 Pins
–	–	P70/ANI8	–	P70/KR0	P70/KR0
–	–	P71/ANI9	–	P71/KR1	P71/KR1
–	–	P72/ANI10	–	P72/KR2	P72/KR2
–	–	–	–	P73/KR3	P73/KR3
–	–	–	–	–	P74/KR4
–	–	–	–	–	P75/KR5

The following operation modes can be specified in 1-bit units.

(1) Port mode

P70 to P75 function as an I/O port. P70 to P75 can be set to input or output port in 1-bit units using port mode register 7 (PM7). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 7 (PU7) in 78K0/KC2-L.

(2) Control mode

P70 to P75 function as pins for A/D converter analog input and key interrupt input pins.

(a) ANI8 to ANI10

These are the A/D converter analog input pins. When using this pin as analog input pin, refer to **(5) ANI0/P20 to ANI7/P27, ANI8/P10 to ANI10/P12, and ANI8/P70 to ANI10/P72** in **12.6 Cautions for A/D Converter**.

(b) KR0 to KR5

These are the key interrupt input pins

Table 3-6. Special Function Register List: 78K0/KY2-L (4/4)

Address	Symbol		Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
			7	6	5	4	3	2	1	0		1	8	16		
FFA7H	IICACTL0		<IICE0>	<LREL0>	<WREL0>	<SPIE0>	<WTIM0>	<ACKE0>	<STT0>	<SPT0>	R/W	√	√	–	00H	492
FFA8H	IICACTL1		<WUP>	0	<CLD0>	<DAD0>	<SMC0>	<DFC0>	0	0	R/W	√	√	–	00H	501
FFA9H	IICAF0		<STCF>	<IICBSY>	0	0	0	0	<STCEN>	<IICRSV>	R/W	√	√	–	00H	499
FFAAH	IICAS0		<MSTS0>	<ALD0>	<EXC0>	<COI0>	<TRC0>	<ACKD0>	<STD0>	<SPD0>	R	√	√	–	00H	497
FFABH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFACH	RESF		0	0	0	WDTRF	0	0	0	LVIRF	R	–	√	–	00H[Note1]	664
FFADH	IICWL		–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	503
FFAEH	IICWH		–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	503
FFAFH to FFB9H	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFBAH	TMC00		0	0	0	0	TMC003	TMC002	TMC001	<OVF00>	R/W	√	√	–	00H	248
FFBBH	PRM00		ES110	ES100	ES010	ES000	0	0	PRM001	PRM000	R/W	√	√	–	00H	253
FFBCH	CRC00		0	0	0	0	0	CRC002	CRC001	CRC000	R/W	√	√	–	00H	249
FFBDH	TOC00		0	<OSPT00>	<OSPE00>	TOC004	<LVS00>	<LVR00>	TOC001	<TOE00>	R/W	√	√	–	00H	251
FFBEH	LVIM		<LVION>	0	0	0	0	0	<LVIMD>	<LVIF>	R/W	√	√	–	00H[Note2]	672
FFBFH	LVIS		0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0	R/W	√	√	–	00H[Note3]	675
FFC0H to FFDFH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFE0H	IF0	IF0L	<SREIF6>	0	0	0	0	<PIF1>	<PIF0>	<LVIIF>	R/W	√	√	√	00H	598
FFE1H		IF0H	<TMIF010>	<TMIF000>	0	0	<TMIFH1>	0	<STIF6>	<SRIF6>	R/W	√	√		00H	598
FFE2H	IF1	IF1L	0	0	0	0	<TMIF51>	0	0	<ADIF>	R/W	√	√	√	00H	598
FFE3H		IF1H	0	0	0	0	0	0	0	<IICAIF0>	R/W	√	√		00H	598
FFE4H	MK0	MK0L	<SREMK6>	1	1	1	1	<PMK1>	<PMK0>	<LVIMK>	R/W	√	√	√	FFH	606
FFE5H		MK0H	<TMMK010>	<TMMK000>	1	1	<TMMKH1>	1	<STMK6>	<SRMK6>	R/W	√	√		FFH	606
FFE6H	MK1	MK1L	1	1	1	1	<TMMK51>	1	1	<ADMK>	R/W	√	√	√	FFH	606
FFE7H		MK1H	1	1	1	1	1	1	1	<IICAMK0>	R/W	√	√		FFH	606
FFE8H	PR0	PR0L	<SREPR6>	1	1	1	1	<PPR1>	<PPR0>	<LVIPR>	R/W	√	√	√	FFH	613
FFE9H		PR0H	<TMPR010>	<TMPR000>	1	1	<TMPRH1>	1	<STPR6>	<SRPR6>	R/W	√	√		FFH	613
FFEAH	PR1	PR1L	1	1	1	1	<TMPR51>	1	1	<ADPR>	R/W	√	√	√	FFH	613
FFEBH		PR1H	1	1	1	1	1	1	1	<IICAPR0>	R/W	√	√		FFH	613
FFECH to FFEFH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFF0H	IMS		RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	R/W	–	√	–	CFH[Note4]	699
FFF1H to FFFAH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFFBH	PCC		0	0	0	0	0	PCC2	PCC1	PCC0	R/W	√	√	–	01H	204

Notes 1. The reset value of RESF varies depending on the reset source.

2. The reset values of LVIM vary depending on the reset source and setting of option byte.

3. The reset values of LVIS vary depending on the reset source.

4. Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated in Table 3-1 after release of reset.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

Table 3-7. Special Function Register List: 78K0/KA2-L (20-pin products) (3/4)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF51H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF52H															
FF53H	ASIS6	0	0	0	0	0	PE6	FE6	OVE6	R	–	√	–	00H	457
FF54H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF55H	ASIF6	0	0	0	0	0	0	TXBF6	TXSF6	R	–	√	–	00H	458
FF56H	CKSR6	0	0	0	0	TPS63	TPS62	TPS61	TPS60	R/W	–	√	–	00H	458
FF57H	BRGC6	MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60	R/W	–	√	–	FFH	460
FF58H	ASICL6	<SBRF6>	<SBRT6>	SBTT6	SBL62	SBL61	SBL60	DIR6	TXDLV6	R/W	√	√	–	16H	461
FF59H to FF5FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF60H	AMP0M[Note1]	<OPAMP0E>	<PGAEN>	0	0	0	0	AMP0VG1	AMP0VG0	R/W	√	√	–	00H	436
FF61H to FF6BH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF6CH	TMHMD1	<TMHE1>	CKS12	CKS11	CKS10	TMMD11	TMMD10	<TOLEV1>	<TOEN1>	R/W	√	√	–	00H	339
FF6DH	TMCYC1	0	0	0	0	0	RMC1	NRZB1	<NRZ1>	R/W	√	√	–	00H	343
FF6EH to FF8BH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF8CH	TCL51	0	0	0	0	0	TCL512	TCL511	TCL510	R/W	√	√	–	00H	318
FF8DH to FF98H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF99H	WDTE	–	–	–	–	–	–	–	–	R/W	–	√	–	1AH/9AH[Note2]	365
FF9AH to FF9EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF9FH	OSCCTL	<EXCLK>	<OSCSEL>	0	0	0	0	0	0	R/W	√	√	–	00H	202
FFA0H	RCM	<RSTS>	0	0	0	0	0	<LSRSTOP>	<RSTOP>	R/W	√	√	–	80H[Note3]	207
FFA1H	MCM	0	0	0	0	0	<XSEL>	<MCS>	<MCM0>	R/W	√	√	–	00H	209
FFA2H	MOC	<MSTOP>	0	0	0	0	0	0	0	R/W	√	√	–	80H	208
FFA3H	OSTC	0	0	0	MOST11	MOST13	MOST14	MOST15	MOST16	R	√	√	–	00H	210, 640
FFA4H	OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	R/W	–	√	–	05H	211, 641
FFA5H	IICA	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	490
FFA6H	SVA0	–	–	–	–	–	–	–	0	R/W	–	√	–	00H	490

Notes 1. This register is incorporated only in products with operational amplifier.

2. The reset value of WDTE is determined by setting of option byte.

3. The value of this register is 00H immediately after a reset release but automatically changes to 80H after oscillation accuracy stabilization of high-speed internal oscillator has been waited.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

3.3 Instruction Address Addressing

An instruction address is determined by contents of the program counter (PC) and is normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to PC and branched by the following addressing (for details of instructions, refer to the **78K/0 Series Instructions User's Manual (U12326E)**).

3.3.1 Relative addressing

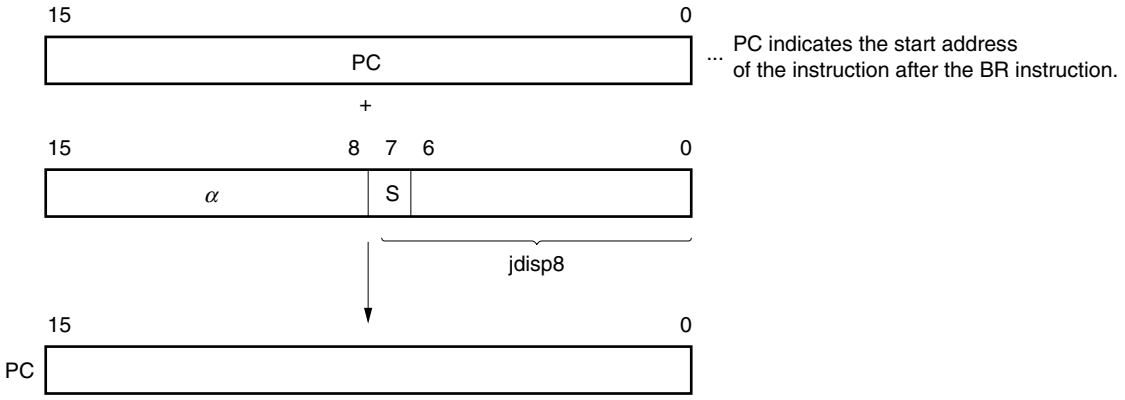
[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (−128 to +127) and bit 7 becomes a sign bit.

In other words, relative addressing consists of relative branching from the start address of the following instruction to the −128 to +127 range.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

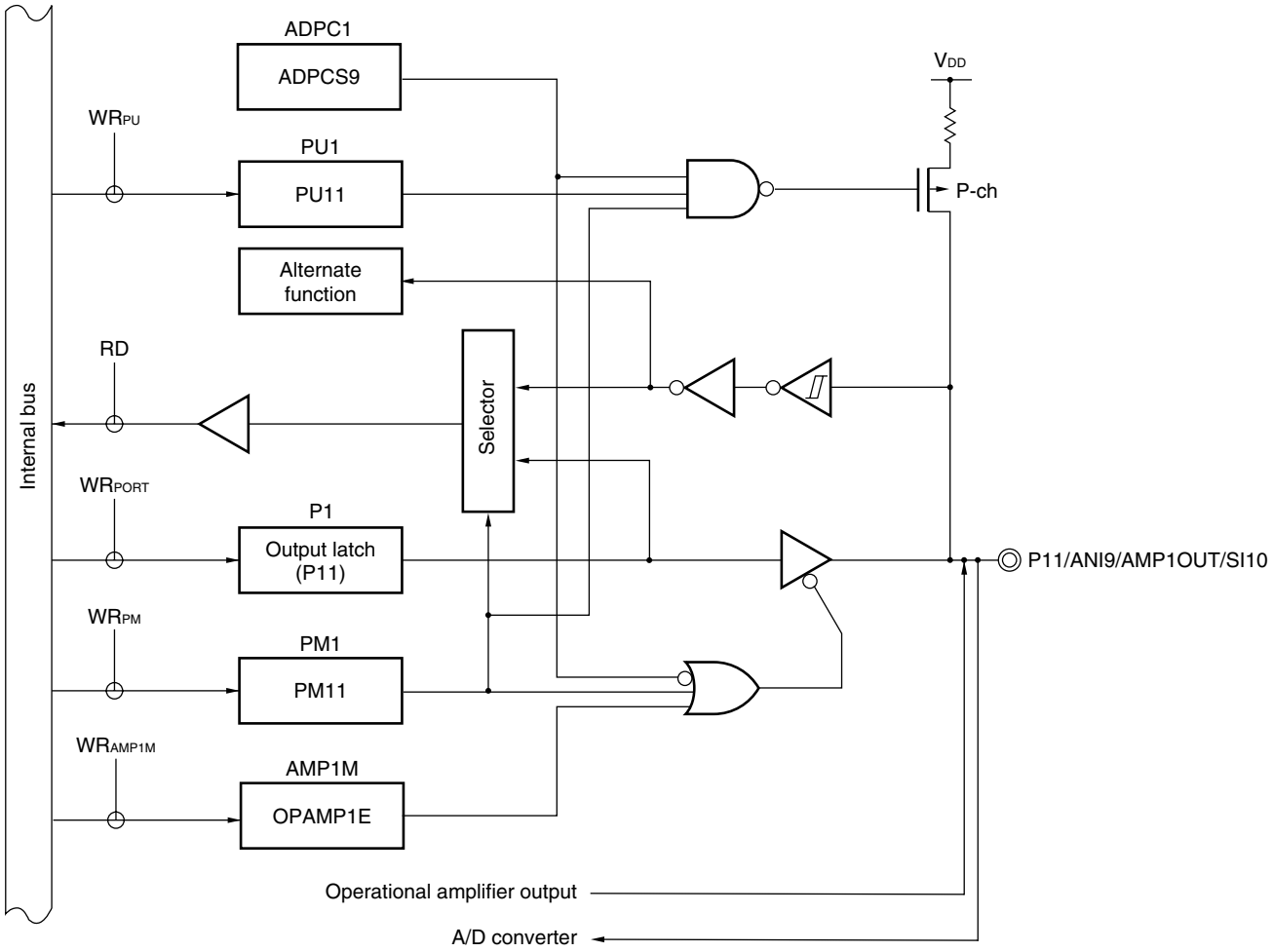
[Illustration]



When S = 0, all bits of α are 0.
When S = 1, all bits of α are 1.

<R> **Figure 4-5. Block Diagram of P11 (2/2)**

(2) Products with operational amplifier of 78K0/KB2-L and 78K0/KC2-L



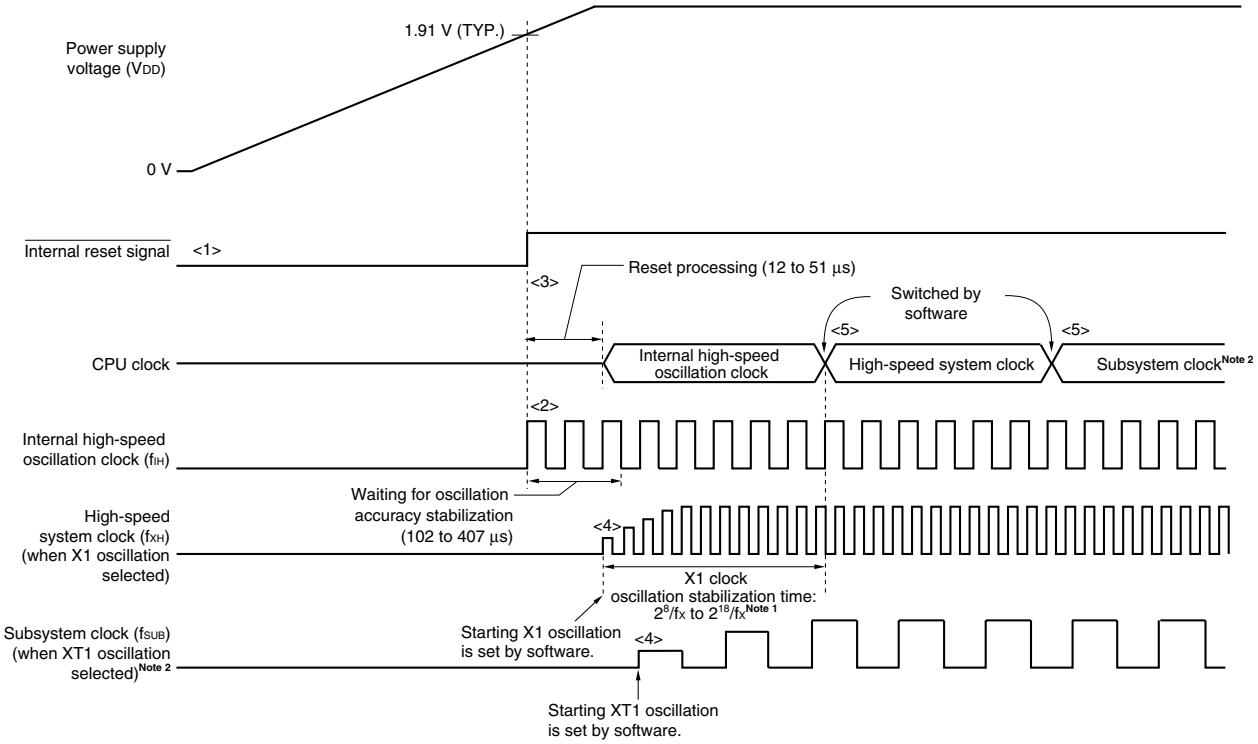
P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
ADPC1: A/D port configuration register 1
RD: Read signal
WR××: Write signal

Cautions 1. If the voltage rises with a slope of less than 0.5 V/ms (MIN.) from power application until the voltage reaches 1.8 V, input a low level to the $\overline{\text{RESET}}$ pin from power application until the voltage reaches 1.8 V, or set the LVI default start function enabled by using the option byte (LVISTART = 1) (refer to Figure 5-17). When a low level has been input to the $\overline{\text{RESET}}$ pin until the voltage reaches 1.8 V, the CPU operates with the same timing as <2> and thereafter in Figure 5-16, after the reset has been released by the $\overline{\text{RESET}}$ pin.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK and EXCLKS pins is used.

Remark While the microcontroller is operating, a clock that is not used as the CPU clock can be stopped via software settings. The internal high-speed oscillation clock and high-speed system clock can be stopped by executing the STOP instruction (refer to **(4)** in **5.6.1 Example of controlling high-speed system clock**, **(3)** in **5.6.2 Example of controlling internal high-speed oscillation clock**, and **(4)** in **5.6.3 Example of controlling subsystem clock**).

Figure 5-17. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Enabled Is Set (Option Byte: LVISTART = 1))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 1.91 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

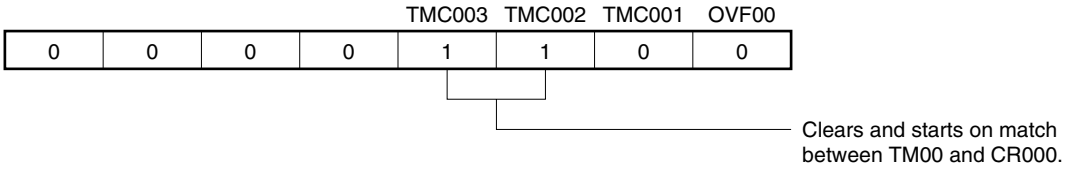
<3> After the reset is released and reset processing is performed, the CPU starts operation on the internal high-speed oscillation clock.

<4> Set the start of oscillation of the X1 or XT1 clock via software (refer to **(1)** in **5.6.1 Example of controlling high-speed system clock** and **(1)** in **5.6.3 Example of controlling subsystem clock**).

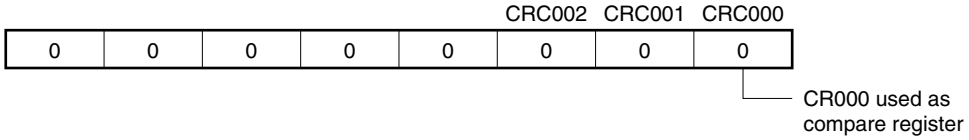
<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (refer to **(3)** in **5.6.1 Example of controlling high-speed system clock** and **(3)** in **5.6.3 Example of controlling subsystem clock**).

Figure 6-21. Example of Register Settings in External Event Counter Mode (1/2)

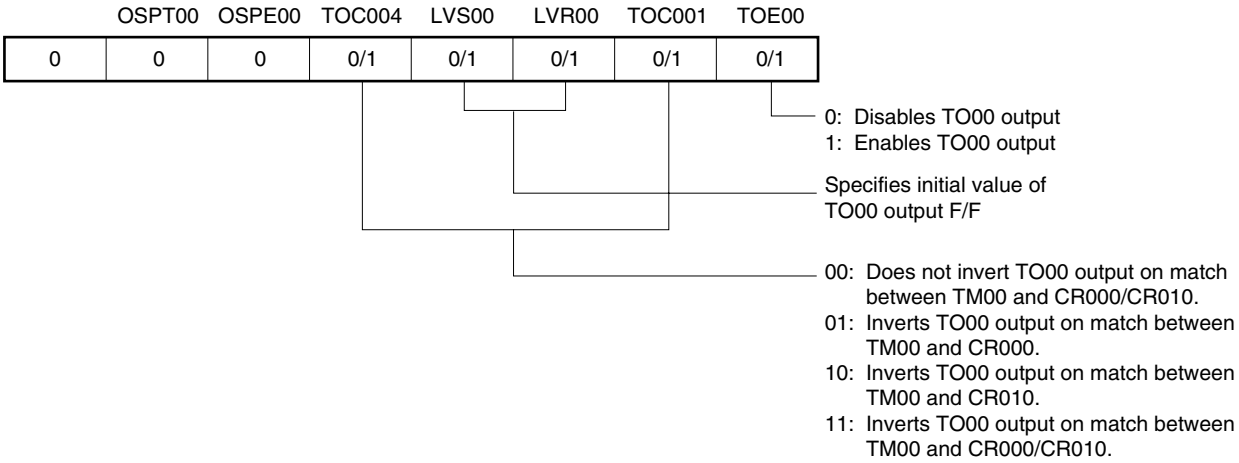
(a) 16-bit timer mode control register 00 (TMC00)



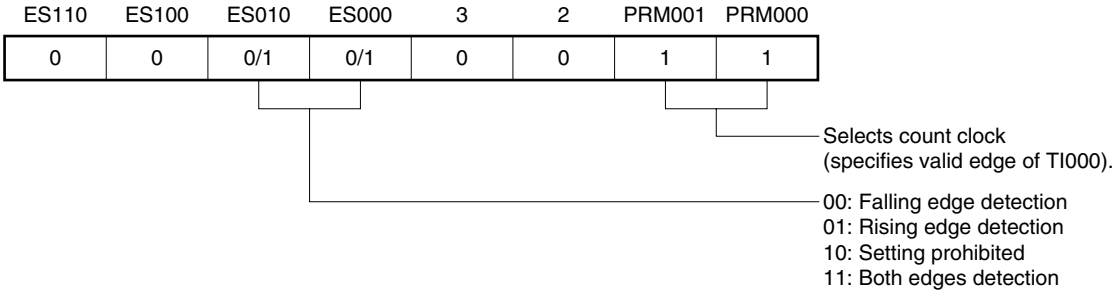
(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)



(9) Capture operation

(a) When valid edge of TI000 is specified as count clock

When the valid edge of TI000 is specified as the count clock, the capture register for which TI000 is specified as a trigger does not operate correctly.

(b) Pulse width to accurately capture value by signals input to TI010 and TI000 pins

To accurately capture the count value, the pulse input to the TI000 and TI010 pins as a capture trigger must be wider than two count clocks selected by PRM00 (refer to **Figure 6-7**).

(c) Generation of interrupt signal

The capture operation is performed at the falling edge of the count clock but the interrupt signals (INTTM000 and INTTM010) are generated at the rising edge of the next count clock (refer to **Figure 6-7**).

(d) Note when CRC001 (bit 1 of capture/compare control register 00 (CRC00)) is set to 1

When the count value of the TM00 register is captured to the CR000 register in the phase reverse to the signal input to the TI000 pin, the interrupt signal (INTTM000) is not generated after the count value is captured. If the valid edge is detected on the TI010 pin during this operation, the capture operation is not performed but the INTTM000 signal is generated as an external interrupt signal. Mask the INTTM000 signal when the external interrupt is not used.

(10) Edge detection

(a) Specifying valid edge after reset

If the operation of the 16-bit timer/event counter 00 is enabled after reset and while the TI000 or TI010 pin is at high level and when the rising edge or both the edges are specified as the valid edge of the TI000 or TI010 pin, then the high level of the TI000 or TI010 pin is detected as the rising edge. Note this when the TI000 or TI010 pin is pulled up. However, the rising edge is not detected when the operation is once stopped and then enabled again.

(b) Sampling clock for eliminating noise

The sampling clock for eliminating noise differs depending on whether the valid edge of TI000 is used as the count clock or capture trigger. In the former case, the sampling clock is fixed to f_{PRS}. In the latter, the count clock selected by PRM00 is used for sampling.

When the signal input to the TI000 pin is sampled and the valid level is detected two times in a row, the valid edge is detected. Therefore, noise having a short pulse width can be eliminated (refer to **Figure 6-7**).

(11) Timer operation

The signal input to the TI000/TI010 pin is not acknowledged while the timer is stopped, regardless of the operation mode of the CPU.

Remark f_{PRS}: Peripheral hardware clock frequency

7.2 Configuration of 8-Bit Timer/Event Counters 50 and 51

8-bit timer/event counters 50 and 51 include the following hardware.

Table 7-1. Configuration of 8-Bit Timer/Event Counters 50 and 51

(1) 78K0/KY2-L, 78K0/KA2-L (20-pin products)

Item	Configuration
Timer register	8-bit timer counter 51 (TM51)
Timer input	TI51
Register	8-bit timer compare register 51 (CR51)
Control registers	Timer clock selection register 51 (TCL51) 8-bit timer mode control register 51 (TMC51) Port mode register 3 (PM3) Port register 3 (P3)

<R> (2) 78K0/KA2-L (25-pin and 32-pin products)

Item	Configuration
Timer register	8-bit timer counter 51 (TM51)
Timer input	TI51 Note
Register	8-bit timer compare register 51 (CR51)
Control registers	Timer clock selection register 51 (TCL51) 8-bit timer mode control register 51 (TMC51) Port alternate switch control register (MUXSEL) Note Port mode register 0 (PM0) or port mode register 3 (PM3) Note Port register 0 (P0) or port register 3 (P3) Note

Note 78K0/KA2-L (25-pin products) only

(3) 78K0/KB2-L, 78K0/KC2-L

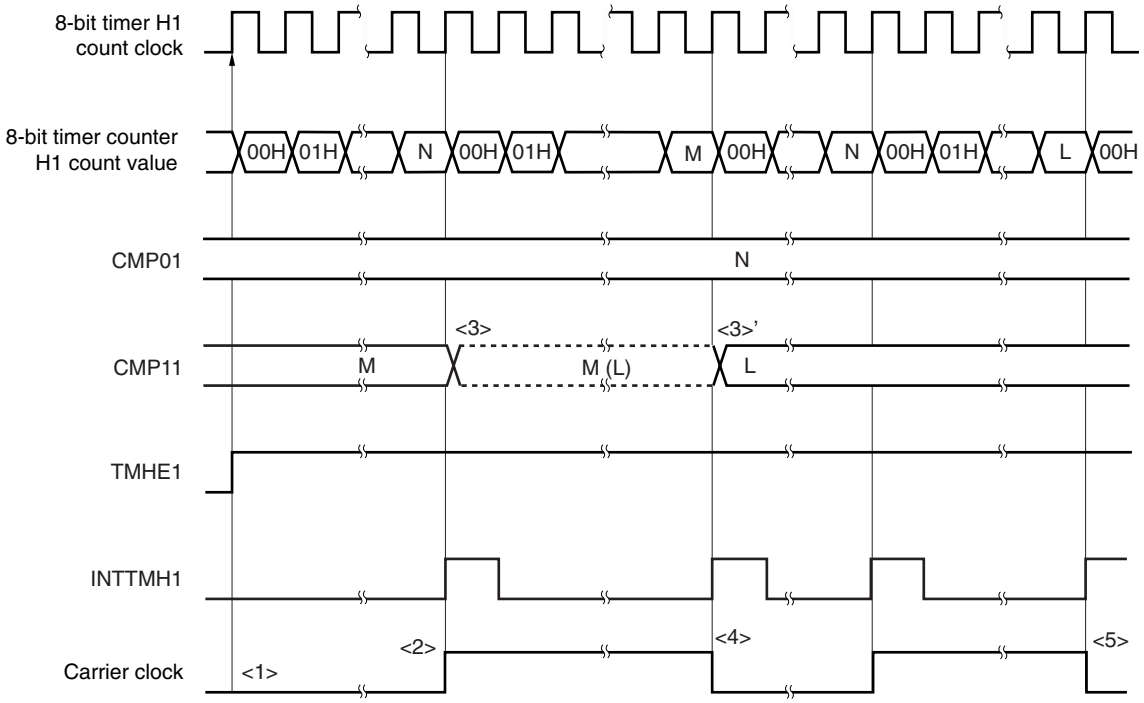
Item	Configuration
Timer register	8-bit timer counter 5n (TM5n)
Register	8-bit timer compare register 5n (CR5n)
Timer input	TI5n
Timer output	TO5n
Control registers	Timer clock selection register 5n (TCL5n) 8-bit timer mode control register 5n (TMC5n) Port mode register 1 (PM1) or port mode register 3 (PM3) Port register 1 (P1) or port register 3 (P3)

Remark n = 0, 1

Figures 7-1 to 7-4 show the block diagrams of 8-bit timer/event counters 50 and 51.

Figure 8-18. Carrier Generator Mode Operation Timing (3/3)

(c) Operation when CMP11 is changed



<1> When TMHE1 = 1 is set, the 8-bit timer H1 starts a count operation. At that time, the carrier clock remains default.

<2> When the count value of the 8-bit timer counter H1 matches the value of the CMP01 register, the INTTMH1 signal is output, the carrier signal is inverted, and the timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter H1 is changed from the CMP01 register to the CMP11 register.

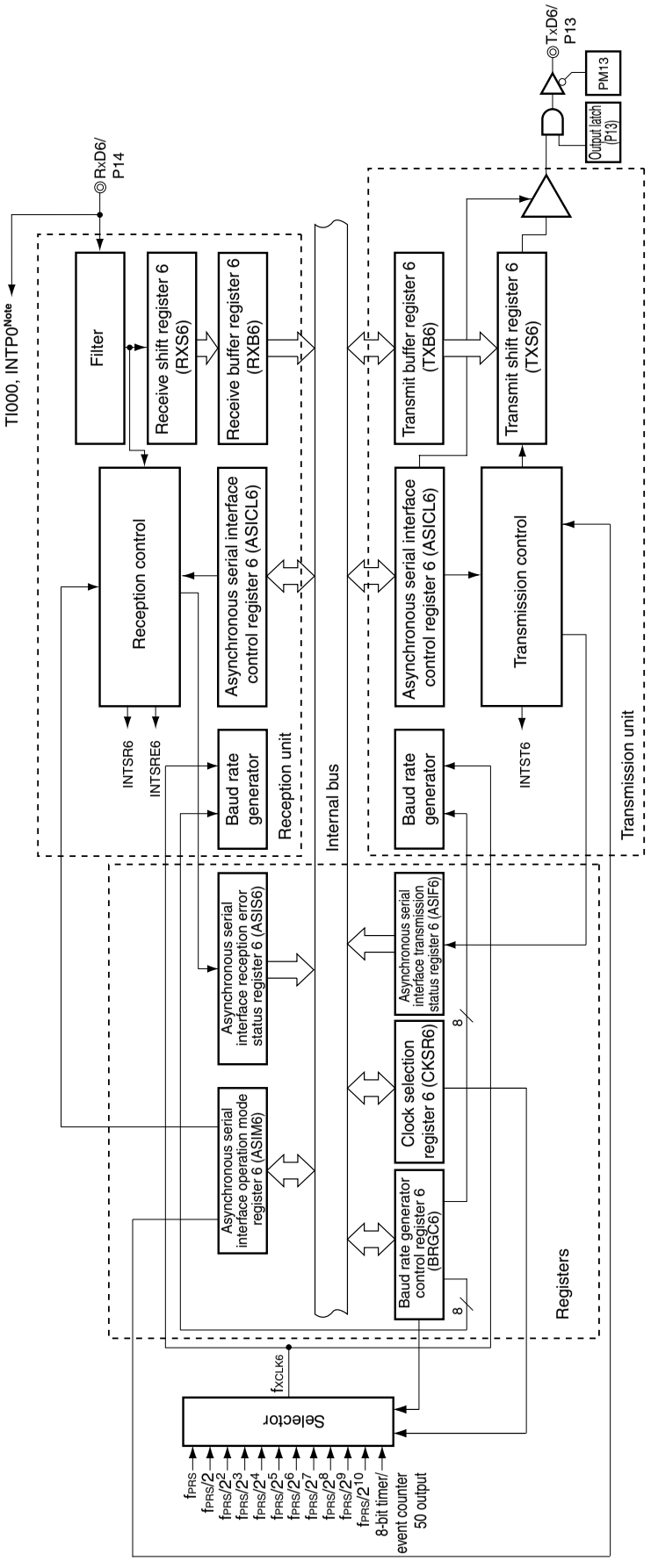
<3> The CMP11 register is asynchronous to the count clock, and its value can be changed while the 8-bit timer H1 is operating. The new value (L) to which the value of the register is to be changed is latched. When the count value of the 8-bit timer counter H1 matches the value (M) of the CMP11 register before the change, the CMP11 register is changed (<3>').

However, it takes three count clocks or more since the value of the CMP11 register has been changed until the value is transferred to the register. Even if a match signal is generated before the duration of three count clocks elapses, the new value is not transferred to the register.

<4> When the count value of 8-bit timer counter H1 matches the value (M) of the CMP11 register before the change, the INTTMH1 signal is output, the carrier signal is inverted, and the timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter H1 is changed from the CMP11 register to the CMP01 register.

<5> The timing at which the count value of the 8-bit timer counter H1 and the CMP11 register value match again is indicated by the value after the change (L).

Figure 14-4. Block Diagram of Serial Interface UART6



Note Selectable with input switch control register (ISC).

Remark 78K0/KY2-L, 78K0/KA2-L: RxD6/SDAA0/P61, TxD6/SCLA0/P60
78K0/KB2-L, 78K0/KC2-L: RxD6/P14, TxD6/P13

(1) Receive buffer register 6 (RXB6)

14.4.3 Dedicated baud rate generator

The dedicated baud rate generator consists of a source clock selector and an 8-bit programmable counter, and generates a serial clock for transmission/reception of UART6.

Separate 8-bit counters are provided for transmission and reception.

(1) Configuration of baud rate generator

- Base clock
  The clock selected by bits 3 to 0 (TPS63 to TPS60) of clock selection register 6 (CKSR6) is supplied to each module when bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is 1. This clock is called the base clock and its frequency is called f_{XCLK6}. The base clock is fixed to low level when POWER6 = 0.

- Transmission counter
  This counter stops operation, cleared to 0, when bit 7 (POWER6) or bit 6 (TXE6) of asynchronous serial interface operation mode register 6 (ASIM6) is 0.
  It starts counting when POWER6 = 1 and TXE6 = 1.
  The counter is cleared to 0 when the first data transmitted is written to transmit buffer register 6 (TXB6).
  If data are continuously transmitted, the counter is cleared to 0 again when one frame of data has been completely transmitted. If there is no data to be transmitted next, the counter is not cleared to 0 and continues counting until POWER6 or TXE6 is cleared to 0.

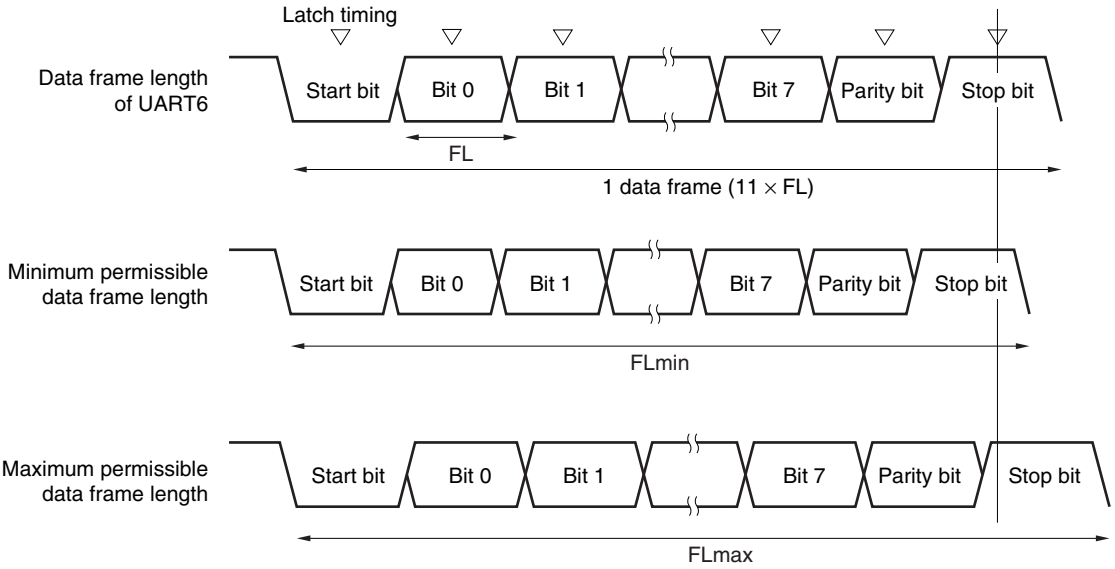
- Reception counter
  This counter stops operation, cleared to 0, when bit 7 (POWER6) or bit 5 (RXE6) of asynchronous serial interface operation mode register 6 (ASIM6) is 0.
  It starts counting when the start bit has been detected.
  The counter stops operation after one frame has been received, until the next start bit is detected.

(4) Permissible baud rate range during reception

The permissible error from the baud rate at the transmission destination during reception is shown below.

Caution Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.

Figure 14-27. Permissible Baud Rate Range During Reception



As shown in Figure 14-27, the latch timing of the receive data is determined by the counter set by baud rate generator control register 6 (BRGC6) after the start bit has been detected. If the last data (stop bit) meets this latch timing, the data can be correctly received.

Assuming that 11-bit data is received, the theoretical values can be calculated as follows.

$FL = (Brate)^{-1}$

Brate: Baud rate of UART6
k: Set value of BRGC6
FL: 1-bit data length
Margin of latch timing: 2 clocks

Figure 15-6. Format of IICA Status Register 0 (IICAS0) (3/3)

ACKD0	Detection of acknowledge ($\overline{ACK}$)
0	Acknowledge was not detected.
1	Acknowledge was detected.

Condition for clearing (ACKD0 = 0)	Condition for setting (ACKD0 = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by LREL0 = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• After the SDAA0 line is set to low level at the rising edge of SCLA0's ninth clock

STD0	Detection of start condition
0	Start condition was not detected.
1	Start condition was detected. This indicates that the address transfer period is in effect.

Condition for clearing (STD0 = 0)	Condition for setting (STD0 = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by LREL0 = 1 (exit from communications) • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is detected

SPD0	Detection of stop condition
0	Stop condition was not detected.
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

Condition for clearing (SPD0 = 0)	Condition for setting (SPD0 = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When the IICE0 bit changes from 1 to 0 (operation stop) • Reset	• When a stop condition is detected

Remark LREL0: Bit 6 of IICA control register 0 (IICACTL0)
IICE0: Bit 7 of IICA control register 0 (IICACTL0)

(3) IICA flag register 0 (IICAF0)

This register sets the operation mode of I^2C and indicates the status of the I^2C bus.

This register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the STT0 clear flag (STCF) and I^2C bus status flag (IICBSY) are read-only.

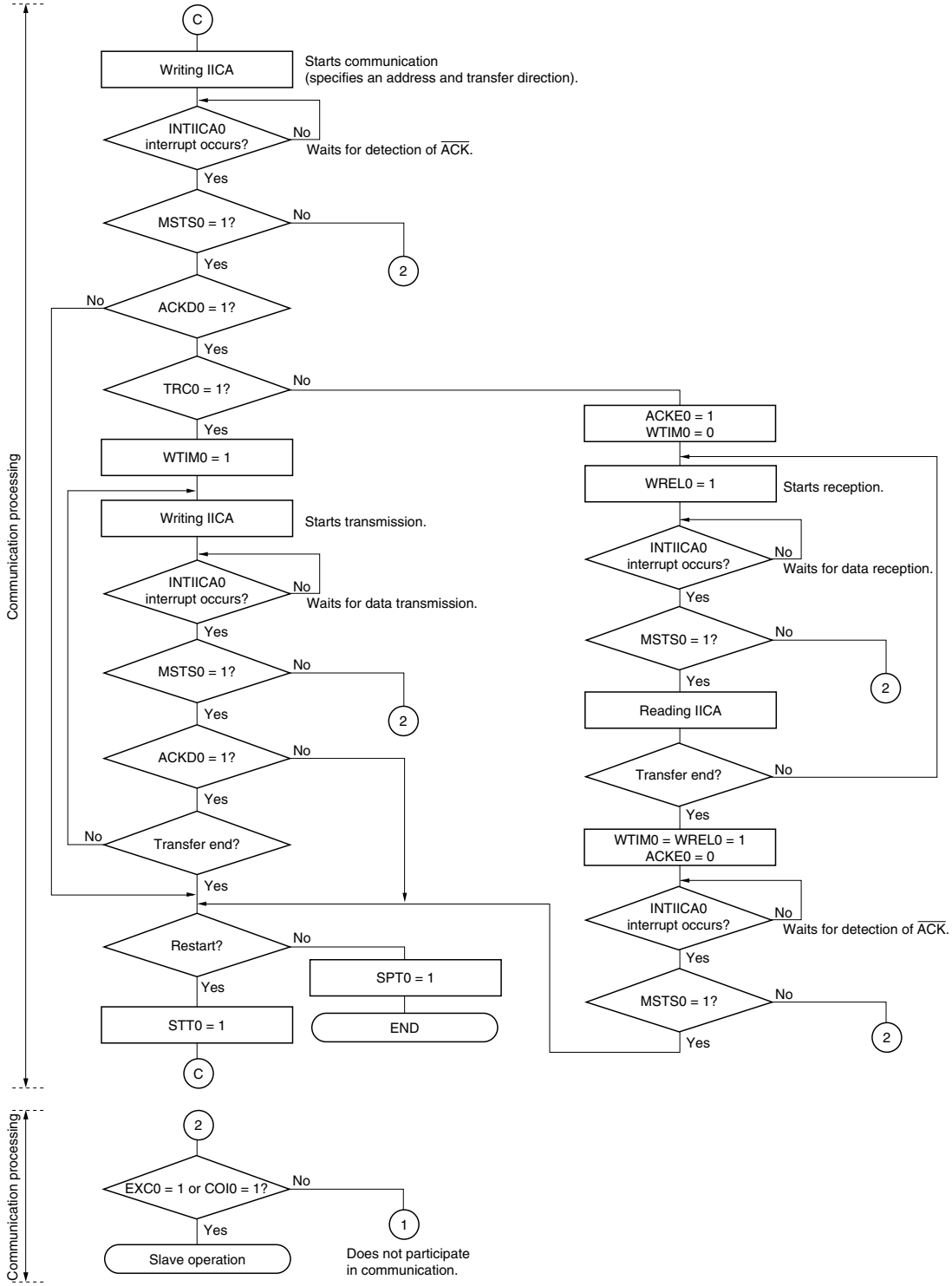
The IICRSV bit can be used to enable/disable the communication reservation function.

The STCEN bit can be used to set the initial value of the IICBSY bit.

The IICRSV and STCEN bits can be written only when the operation of I^2C is disabled (bit 7 (IICE0) of the IICA control register 0 (IICACTL0) = 0). When operation is enabled, the IICAF0 register can be read.

Reset signal generation clears this register to 00H.

Figure 15-30. Master Operation in Multi-Master System (3/3)



Remarks 1. Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

2. To use the device as a master in a multi-master system, read the MSTS0 bit each time interrupt INTIICA0 has occurred to check the arbitration result.

3. To use the device as a slave in a multi-master system, check the status by using the IICAS0 and IICAF0 registers each time interrupt INTIICA0 has occurred, and determine the processing to be performed next.

(3) Slave operation

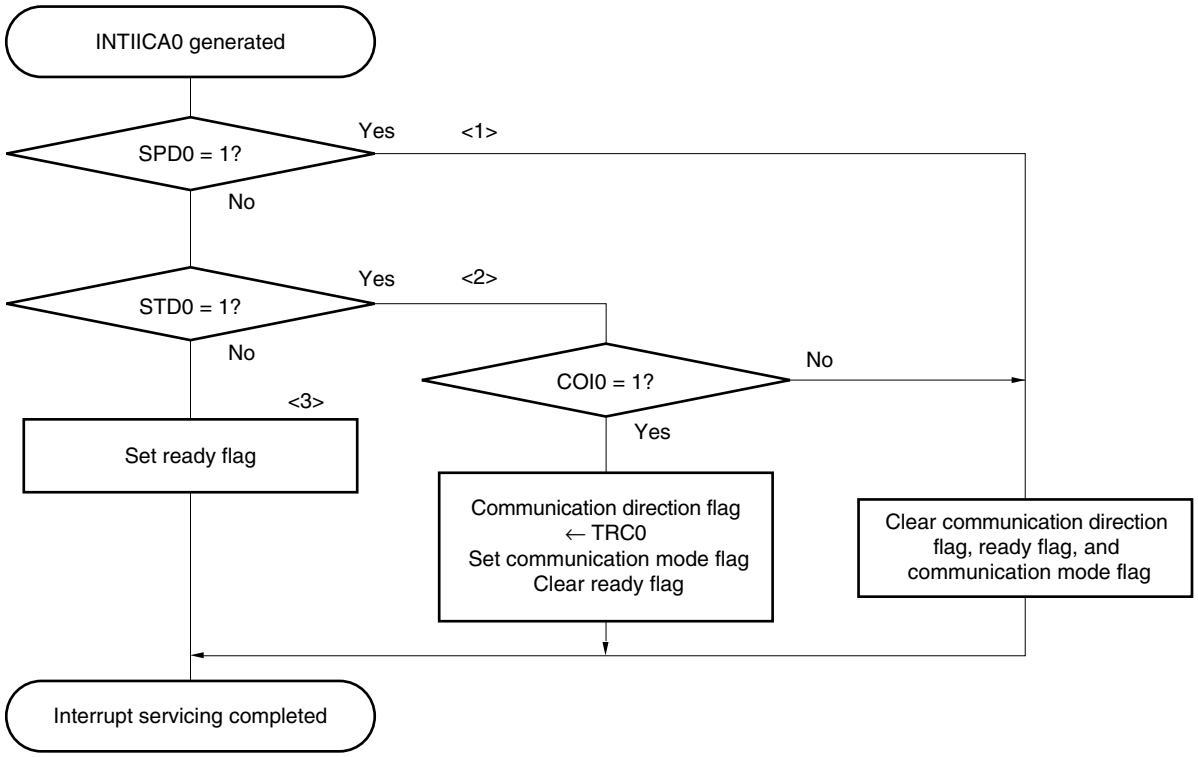
The processing procedure of the slave operation is as follows.

An example of the processing procedure of the slave with the INTIICA0 interrupt is explained below (processing is performed assuming that no extension code is used). The INTIICA0 interrupt checks the status, and the following operations are performed.

<1> Communication is stopped if the stop condition is issued.
<2> If the start condition is issued, the address is checked and communication is completed if the address does not match. If the address matches, the communication mode is set, wait is cancelled, and processing returns from the interrupt (the ready flag is cleared).
<3> For data transmit/receive, only the ready flag is set. Processing returns from the interrupt with the I^2C bus remaining in the wait state.

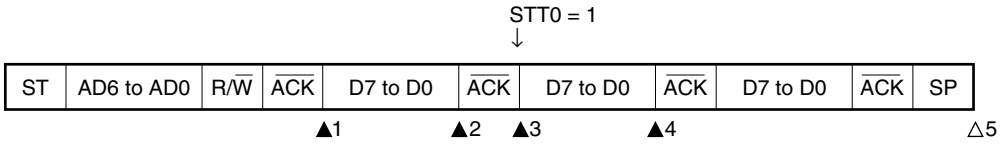
Remark <1> to <3> above correspond to <1> to <3> in Figure 15-32 Slave Operation Flowchart (2).

Figure 15-32. Slave Operation Flowchart (2)



(f) When arbitration loss occurs due to low-level data when attempting to generate a restart condition

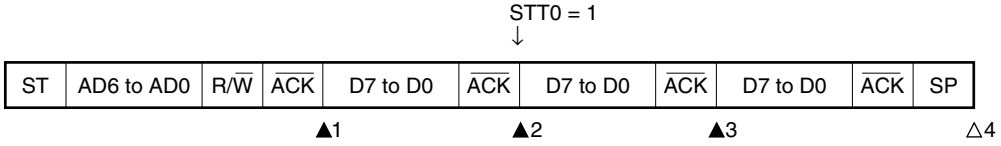
(i) When WTIM0 = 0



▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 1000×000B (Sets WTIM0 to 1)
▲3: IICAS0 = 1000×100B (Clears WTIM0 to 0)
▲4: IICAS0 = 01000000B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1



▲1: IICAS0 = 1000×110B
▲2: IICAS0 = 1000×100B (Sets STT0 to 1)
▲3: IICAS0 = 01000100B
△4: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

22.4.1 When used as reset

(1) When detecting level of supply voltage (V_{DD})

(a) When LVI default start function stopped is set (LVISTART = 0)

- When starting operation

<1> Mask the LVI interrupt (LVIMK = 1).

<2> Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (detects level of supply voltage (V_{DD})) (default value).

<3> Set the LVI detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).

<4> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).

<5> Use software to wait for an operation stabilization time (10 μs (MAX.)).

<6> Wait until it is checked that (supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI})) by bit 0 (LVIF) of LVIM.

<7> Set bit 1 (LVIMD) of LVIM to 1 (generates reset when the level is detected).

Figure 22-5 shows the timing of the internal reset signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <7> above.

Cautions 1. Be sure to execute <1>. When LVIMK = 0, an interrupt may occur immediately after the processing in <4>.

2. If supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI}) when LVIMD is set to 1, an internal reset signal is not generated.

- When stopping operation

Either of the following procedures must be executed.

• When using 8-bit memory manipulation instruction:

Write 00H to LVIM.

• When using 1-bit memory manipulation instruction:

Clear LVIMD to 0 and then LVION to 0.

CHAPTER 25 FLASH MEMORY

The 78K0/Kx2-L microcontrollers incorporates the flash memory to which a program can be written, erased, and overwritten while mounted on the board.

25.1 Internal Memory Size Switching Register

Select the internal memory capacity using the internal memory size switching register (IMS).
IMS is set by an 8-bit memory manipulation instruction.
Reset signal generation sets IMS to CFH.

Caution Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated Table 25-1 after release of reset.

Figure 25-1. Format of Internal Memory Size Switching Register (IMS)

Address: FFF0H After reset: CFH R/W

Symbol	7	6	5	4	3	2	1	0
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
0	0	0	768 bytes
0	1	0	512 bytes
0	1	1	384 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
0	0	0	1	4 KB
0	0	1	0	8 KB
0	1	0	0	16 KB
1	0	0	0	32 KB
1	1	1	1	(Default value)
Other than above				Setting prohibited