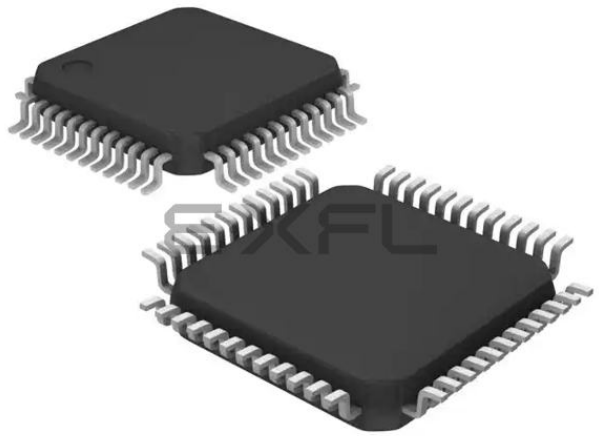

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Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
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Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

<R>**Related Documents** The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
78K0/Kx2-L User's Manual	This manual
78K0/Kx2-L Application Note Setting for Low Power Consumption Operation	U19612E
78K/0 Series User's Manual Instructions	U12326E
78K0 Microcontrollers User's Manual Self Programming Library Type 01	U18274E
78K0 Microcontrollers Self Programming Library Type 01 Ver. 3.10 Operating Precautions (Notification Document)	ZUD-CD-09-0122
78K0 Microcontrollers User's Manual EEPROM™ Emulation Library Type 01	U18275E
78K0 Microcontrollers EEPROM Emulation Library Type 01 Ver.2.10 Operating Precautions (Notification Document)	ZUD-CD-09-0165

Documents Related to Development Tools (Hardware) (User's Manual)

Document Name		Document No.
QB-MINI2 On-Chip Debug Emulator with Programming Function		U18371E
QB-Programmer Programming GUI	Operation	U18527E

Documents Related to Flash Memory Programming (User's Manual)

Document Name	Document No.
PG-FP5 Flash Memory Programmer	U18865E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

There are two types of pin I/O buffer power supplies: AV_{REF} and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27[Note]
V_{DD}	Pins other than P20 to P27[Note]

Note 78K0/KY2-L: P20 to P23
78K0/KA2-L (20 pins): P20 to P25
<R> 78K0/KA2-L (25 pins): P20 to P26
<R> 78K0/KA2-L (32 pins): P20 to P27, P70 to P72
78K0/KB2-L: P20 to P23
<R> 78K0/KC2-L (40 pins): P20 to P26
78K0/KC2-L (44 pins, 48 pins): P20 to P27

Table 3-6. Special Function Register List: 78K0/KY2-L (2/4)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF26H	PM6	1	1	1	1	1	1	PM61	PM60	R/W	√	√	–	FFH	167, 463, 504, 573
FF27H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF28H	ADM0	<ADCS>	0	FR2	FR1	FR0	LV1	LV0	<ADCE>	R/W	√	√	–	00H	405
FF29H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF2AH	POM6	0	0	0	0	0	0	POM61	POM60	R/W	√	√	–	00H	180, 464, 504
FF2BH	FPCTL	0	0	0	0	0	0	0	<FLMD PUP>	R/W	√	√	–	00H	713
FF2CH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF2DH	RSTMASK	0	0	RSTM	0	0	0	0	0	R/W	√	√	–	00H	180
FF2EH	ADPC0	0	0	0	0	ADPCS3	ADPCS2	ADPCS1	ADPCS0	R/W	√	√	–	00H	181, 413, 437
FF2FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF30H	PU0	0	0	0	0	0	0	PU01	PU00	R/W	√	√	–	00H	177
FF31H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF32H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF33H	PU3	0	0	0	0	0	0	0	PU30	R/W	√	√	–	00H	177
FF34H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF35H															
FF36H	PU6	0	0	0	0	0	0	PU61	PU60	R/W	√	√	–	00H	177
FF37H to FF3BH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF3CH	PU12	0	0	PU125	0	0	0	0	0	R/W	√	√	–	20H	177
FF3DH	RMC	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	691
FF3EH	PIM6	0	0	0	0	0	0	PIM61	PIM60	R/W	√	√	–	00H	179, 503
FF3FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF40H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF41H	CR51	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	317
FF42H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF43H	TMC51	<TCE51>	0	0	0	0	0	0	0	R/W	√	√	–	00H	320
FF44H to FF47H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF48H	EGPCTL0	0	0	0	0	0	0	EGP1	EGP0	R/W	√	√	–	00H	619
FF49H	EGNCTL0	0	0	0	0	0	0	EGN1	EGN0	R/W	√	√	–	00H	619
FF4AH to FF4EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF4FH	ISC	0	0	0	0	0	0	ISC1	ISC0	R/W	√	√	–	00H	463
FF50H	ASIM6	<POWER6>	<TXE6>	<RXE6>	PS61	PS60	CL6	SL6	ISRM6	R/W	√	√	–	01H	454

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

Table 3-7. Special Function Register List: 78K0/KA2-L (20-pin products) (4/4)

Address	Symbol		Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
			7	6	5	4	3	2	1	0		1	8	16		
FFA7H	IICACTL0		<IICE0>	<LREL0>	<WREL0>	<SPIE0>	<WTIM0>	<ACKE0>	<STT0>	<SPT0>	R/W	√	√	–	00H	492
FFA8H	IICACTL1		<WUP>	0	<CLD0>	<DAD0>	<SMC0>	<DFC0>	0	0	R/W	√	√	–	00H	501
FFA9H	IICAF0		<STCF>	<IICBSY>	0	0	0	0	<STCEN>	<IICRSV>	R/W	√	√	–	00H	499
FFAAH	IICAS0		<MSTS0>	<ALD0>	<EXC0>	<COI0>	<TRC0>	<ACKD0>	<STD0>	<SPD0>	R	√	√	–	00H	497
FFABH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFACH	RESF		0	0	0	WDTRF	0	0	0	LVIRF	R	–	√	–	00H[Note1]	664
FFADH	IICWL		–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	503
FFAEH	IICWH		–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	503
FFAFH to FFB9H	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFBAH	TMC00		0	0	0	0	TMC003	TMC002	TMC001	<OVF00>	R/W	√	√	–	00H	248
FFBBH	PRM00		ES110	ES100	ES010	ES000	0	0	PRM001	PRM000	R/W	√	√	–	00H	253
FFBCH	CRC00		0	0	0	0	0	CRC002	CRC001	CRC000	R/W	√	√	–	00H	249
FFBDH	TOC00		0	<OSPT00>	<OSPE00>	TOC004	<LVS00>	<LVR00>	TOC001	<TOE00>	R/W	√	√	–	00H	251
FFBEH	LVIM		<LVION>	0	0	0	0	0	<LVIMD>	<LVIF>	R/W	√	√	–	00H[Note2]	672
FFBFH	LVIS		0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0	R/W	√	√	–	00H[Note3]	675
FFC0H to FFDFH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFE0H	IF0	IF0L	<SREIF6>	0	0	<PIF3>	<PIF2>	<PIF1>	<PIF0>	<LVIIF>	R/W	√	√	√	00H	598
FFE1H		IF0H	<TMIF010>	<TMIF000>	0	0	<TMIFH1>	0	<STIF6>	<SRIF6>	R/W	√	√		00H	598
FFE2H	IF1	IF1L	0	0	0	0	<TMIF51>	0	0	<ADIF>	R/W	√	√	√	00H	598
FFE3H		IF1H	0	0	0	0	0	0	0	<IICAIF0>	R/W	√	√		00H	598
FFE4H	MK0	MK0L	<SREMK6>	1	1	<PMK3>	<PMK2>	<PMK1>	<PMK0>	<LVIMK>	R/W	√	√	√	FFH	606
FFE5H		MK0H	<TMMK010>	<TMMK000>	1	1	<TMMKH1>	1	<STMK6>	<SRMK6>	R/W	√	√		FFH	606
FFE6H	MK1	MK1L	1	1	1	1	<TMMK51>	1	1	<ADMK>	R/W	√	√	√	FFH	606
FFE7H		MK1H	1	1	1	1	1	1	1	<IICAMK0>	R/W	√	√		FFH	606
FFE8H	PR0	PR0L	<SREMK6>	1	1	<PPR3>	<PPR2>	<PPR1>	<PPR0>	<LVIPR>	R/W	√	√	√	FFH	613
FFE9H		PR0H	<TMPR010>	<TMPR000>	1	1	<TMPRH1>	1	<STPR6>	<SRPR6>	R/W	√	√		FFH	613
FFEAH	PR1	PR1L	1	1	1	1	<TMPR51>	1	1	<ADPR>	R/W	√	√	√	FFH	613
FFEBH		PR1H	1	1	1	1	1	1	1	<IICAPR0>	R/W	√	√		FFH	613
FFECH to FFEFH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFF0H	IMS		RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	R/W	–	√	–	CFH[Note4]	699
FFF1H to FFFAH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFFBH	PCC		0	0	0	0	0	PCC2	PCC1	PCC0	R/W	√	√	–	01H	204

Notes 1. The reset value of RESF varies depending on the reset source.

2. The reset values of LVIM vary depending on the reset source and setting of option byte.

3. The reset values of LVIS vary depending on the reset source.

4. Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated in Table 3-1 after release of reset.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

<R> **Table 3-8. Special Function Register List: 78K0/KA2-L (25-pin and 32-pin products) (5/5)**

Address	Symbol		Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
			7	6	5	4	3	2	1	0		1	8	16		
FFC0H to FFDFH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFE0H	IF0	IF0L	<SREIF6>	<PIF5>	<PIF4>	<PIF3>	<PIF2>	0	<PIF0>	<LVIIF>	R/W	√	√	√	00H	598
FFE1H		IF0H	<TMIF010>	<TMIF000>	0	0	<TMIFH1>	<CSIIF10>	<STIF6>	<SRIF6>	R/W	√	√		00H	598
FFE2H	IF1	IF1L	0	0	0	0	<TMIF51>	0	0	<ADIF>	R/W	√	√	√	00H	598
FFE3H		IF1H	0	0	0	0	0	0	0	<IICAIF0>	R/W	√	√		00H	598
FFE4H	MK0	MK0L	<SREMK6>	<PMK5>	<PMK4>	<PMK3>	<PMK2>	1	<PMK0>	<LVIMK>	R/W	√	√	√	FFH	606
FFE5H		MK0H	<TMMK010>	<TMMK000>	1	1	<TMMKH1>	<CSIMK10	<STMK6>	<SRMK6>	R/W	√	√		FFH	606
FFE6H	MK1	MK1L	1	1	1	1	<TMMK51>	1	1	<ADMK>	R/W	√	√	√	FFH	606
FFE7H		MK1H	1	1	1	1	1	1	1	<IICAMK0>	R/W	√	√		FFH	606
FFE8H	PR0	PR0L	<SREMK6>	<PPR5>	<PPR4>	<PPR3>	<PPR2>	1	<PPR0>	<LVIPR>	R/W	√	√	√	FFH	613
FFE9H		PR0H	<TMPR010>	<TMPR000>	1	1	<TMPRH1>	<CSIPR10>	<STPR6>	<SRPR6>	R/W	√	√		FFH	613
FFEAH	PR1	PR1L	1	1	1	1	<TMPR51>	1	1	<ADPR>	R/W	√	√	√	FFH	613
FFEBH		PR1H	1	1	1	1	1	1	1	<IICAPR0>	R/W	√	√		FFH	613
FFECH to FFEFH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFF0H	IMS		RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	R/W	–	√	–	CFH[Note]	699
FFF1H to FFFAH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFFBH	PCC		0	0	0	0	0	PCC2	PCC1	PCC0	R/W	√	√	–	01H	204

Note Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated in Table 3-1 after release of reset.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

(3) Internal low-speed oscillation clock (clock for watchdog timer)

- **Internal low-speed oscillator**

  This circuit oscillates a clock of f_{IL} = 30 kHz (TYP.). After a reset release, the internal low-speed oscillation clock always starts operating.

  Oscillation can be stopped by using the internal oscillation mode register (RCM) when “internal low-speed oscillator can be stopped by software” is set by option byte.

  The internal low-speed oscillation clock cannot be used as the CPU clock. The following hardware operates with the internal low-speed oscillation clock.

  - Watchdog timer
  - 8-bit timer H1 (when f_{IL}, $f_{IL}/2^6$, or $f_{IL}/2^{15}$ is selected)

Remark f_{IL}: Internal low-speed oscillation clock frequency

5.2 Configuration of Clock Generator

The clock generator includes the following hardware.

Table 5-1. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode select register (OSCCTL) Processor clock control register (PCC) Internal oscillation mode register (RCM) Main OSC control register (MOC) Main clock mode register (MCM) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS)
Oscillators	X1 oscillator XT1 oscillator[Note] Internal high-speed oscillator Internal low-speed oscillator

Note 78K0/KC2-L only

(5) Main OSC control register (MOC)

This register selects the operation mode of the high-speed system clock.

This register is used to stop the X1 oscillator or to disable an external clock input from the EXCLK pin when the CPU operates with a clock other than the high-speed system clock.

MOC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 80H.

Figure 5-8. Format of Main OSC Control Register (MOC)

Address: FFA2H After reset: 80H R/W

Symbol	<7>	6	5	4	3	2	1	0
MOC	MSTOP	0	0	0	0	0	0	0

MSTOP	Control of high-speed system clock operation	
	X1 oscillation mode	External clock input mode
0	X1 oscillator operating	External clock from EXCLK pin is enabled
1	X1 oscillator stopped	External clock from EXCLK pin is disabled

Cautions 1. Clear MSTOP to 0 while the regulator mode control register (RMC) is 00H.

2. When setting MSTOP to 1, be sure to confirm that the CPU operates with a clock other than the high-speed system clock. Specifically, set under either of the following conditions.

<1> 78K0/KY2-L, 78K0/KA2-L, and 78K0/KB2-L

- **When MCS = 0 (when CPU operates with the internal high-speed oscillation clock)**

<2> 78K0/KC2-L

- **When MCS = 0 (when CPU operates with the internal high-speed oscillation clock)**
- **When CLS = 1 (when CPU operates with the subsystem clock)**

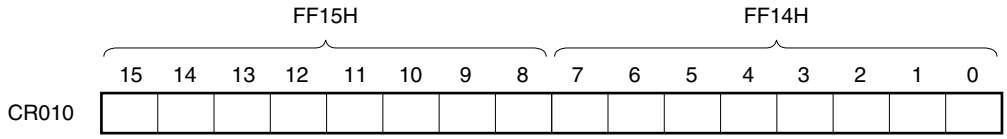
In addition, stop peripheral hardware that is operating on the high-speed system clock before setting MSTOP to 1.

3. Do not clear MSTOP to 0 while bit 6 (OSCSEL) of the clock operation mode select register (OSCCTL) is 0 (input port mode).

4. The peripheral hardware cannot operate when the peripheral hardware clock is stopped. To resume the operation of the peripheral hardware after the peripheral hardware clock has been stopped, initialize the peripheral hardware.

Figure 6-4. Format of 16-Bit Timer Capture/Compare Register 010 (CR010)

Address: FF14H, FF15H After reset: 0000H R/W



(i) When CR010 is used as a compare register

The value set in CR010 is constantly compared with the TM00 count value, and an interrupt request signal (INTTM010) is generated if they match.

Caution CR010 does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

(ii) When CR010 is used as a capture register

The count value of TM00 is captured to CR010 when a capture trigger is input.

It is possible to select the valid edge of the TI000 pin as the capture trigger. The TI000 pin valid edge is set by PRM00.

(iii) Setting range when CR000 or CR010 is used as a compare register

When CR000 or CR010 is used as a compare register, set it as shown below.

Operation	CR000 Register Setting Range	CR010 Register Setting Range
Operation as interval timer	0000H < N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH Normally, this setting is not used. Mask the match interrupt signal (INTTM010).
Operation as square-wave output		
Operation as external event counter		
Operation in the clear & start mode entered by TI000 pin valid edge input	0000H[Note] ≤ N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH
Operation as free-running timer		
Operation as PPG output	M < N ≤ FFFFH	0000H[Note] ≤ M < N
Operation as one-shot pulse output	0000H[Note] ≤ N ≤ FFFFH (N ≠ M)	0000H[Note] ≤ M ≤ FFFFH (M ≠ N)

Note When 0000H is set, a match interrupt immediately after the timer operation does not occur and timer output is not changed, and the first match timing is as follows. A match interrupt occurs at the timing when the timer counter (TM00 register) is changed from 0000H to 0001H.

- When the timer counter is cleared due to overflow
- When the timer counter is cleared due to TI000 pin valid edge (when clear & start mode is entered by TI000 pin valid edge input)
- When the timer counter is cleared due to compare match (when clear & start mode is entered by match between TM00 and CR000 (CR000 = other than 0000H, CR010 = 0000H))

(1) PWM output basic operation

Setting

<1> Set each register.

- Clear the port output latch (P17 or P33)[Note] and port mode register (PM17 or PM33)[Note] to 0.
- TCL5n: Select the count clock.
- CR5n: Compare value
- TMC5n: Stop the count operation, select PWM mode.
  The timer output F/F is not changed.

TMC5n1	Active Level Selection
0	Active-high
1	Active-low

Timer output enabled
(TMC5n = 01000001B or 01000011B)

<2> The count operation starts when TCE5n = 1.
Clear TCE5n to 0 to stop the count operation.

Note 8-bit timer/event counter 50: P17, PM17
8-bit timer/event counter 51: P33, PM33

PWM output operation

<1> PWM output (TO5n output) outputs an inactive level until an overflow occurs.

<2> When an overflow occurs, the active level is output. The active level is output until CR5n matches the count value of 8-bit timer counter 5n (TM5n).

<3> After the CR5n matches the count value, the inactive level is output until an overflow occurs again.

<4> Operations <2> and <3> are repeated until the count operation stops.

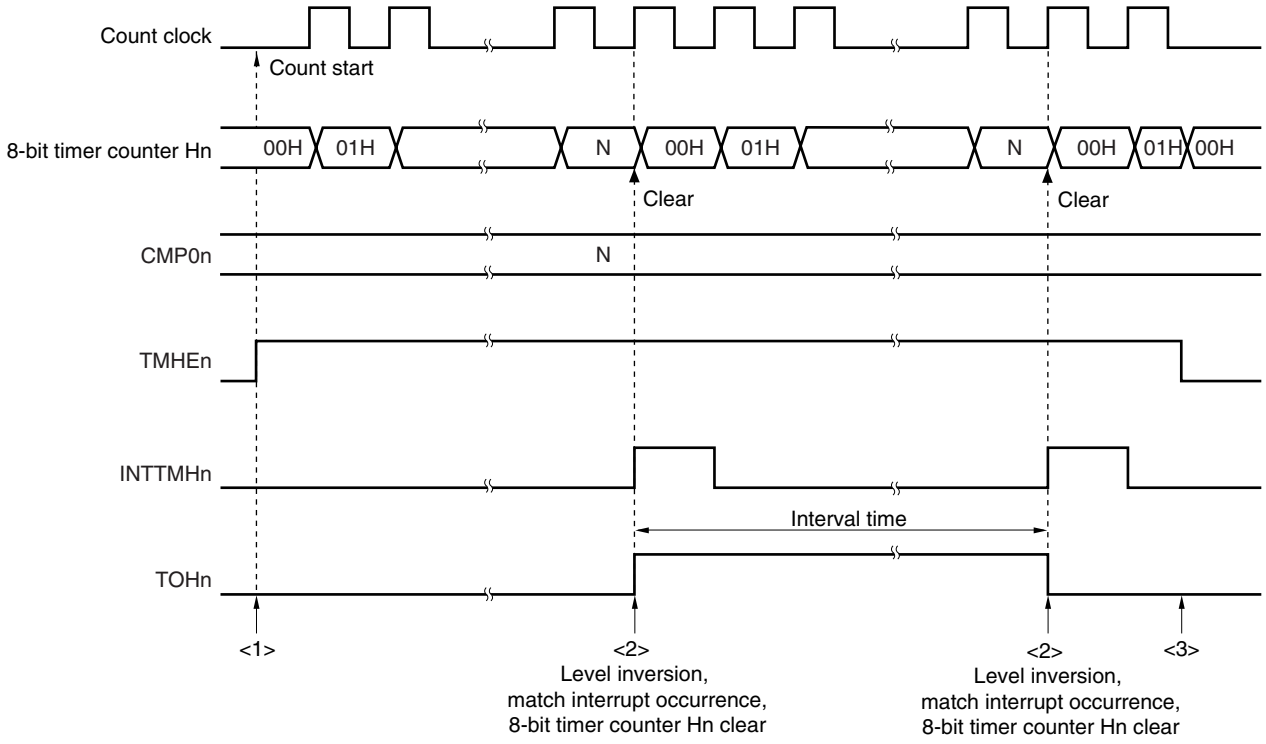
<5> When the count operation is stopped with TCE5n = 0, PWM output becomes inactive.
For details of timing, refer to **Figures 7-18** and **7-19**.
The cycle, active-level width, and duty are as follows.

- Cycle = 2^8t
- Active-level width = Nt
- Duty = N/2^8
  (N = 00H to FFH)

Remark 78K0/KB2-L, 78K0/KC2-L: n = 0, 1

Figure 8-13. Timing of Interval Timer/Square-Wave Output Operation (1/2)

(a) Basic operation (Operation When 01H ≤ CMP0n ≤ FEH)



<1> The count operation is enabled by setting the TMHEn bit to 1. The count clock starts counting no more than 1 clock after the operation is enabled.

<2> When the value of the 8-bit timer counter Hn matches the value of the CMP0n register, the value of the timer counter is cleared, and the level of the TOHn output is inverted. In addition, the INTTMHn signal is output at the rising edge of the count clock.

<3> If the TMHEn bit is cleared to 0 while timer H is operating, the INTTMHn signal and TOHn output are set to the default level. If they are already at the default level before the TMHEn bit is cleared to 0, then that level is maintained.

Remarks 1. 01H ≤ N ≤ FEH

2. 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

Figure 10-27. Operation when (DEV, F6, F5, F4, F3, F2, F1, F0) = (0, 0, 1, 0, 1, 1, 0, 0)

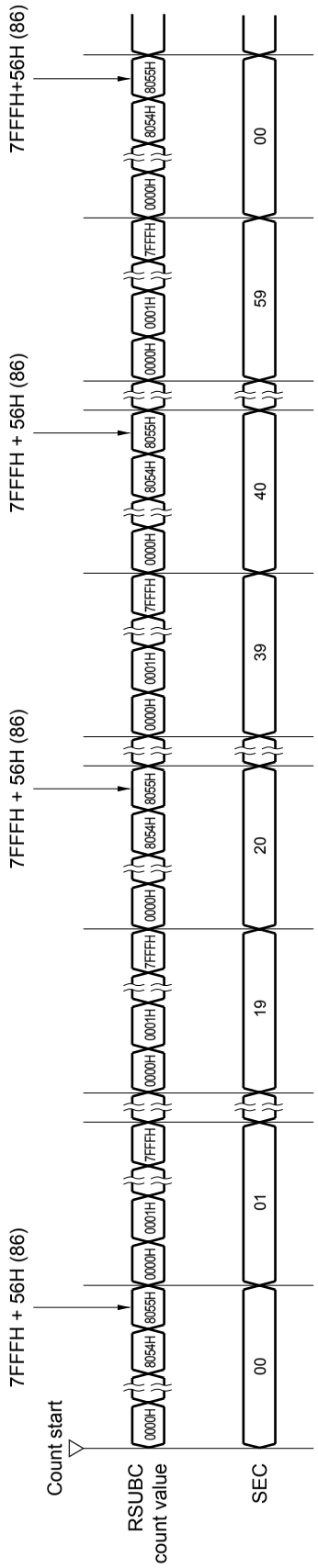
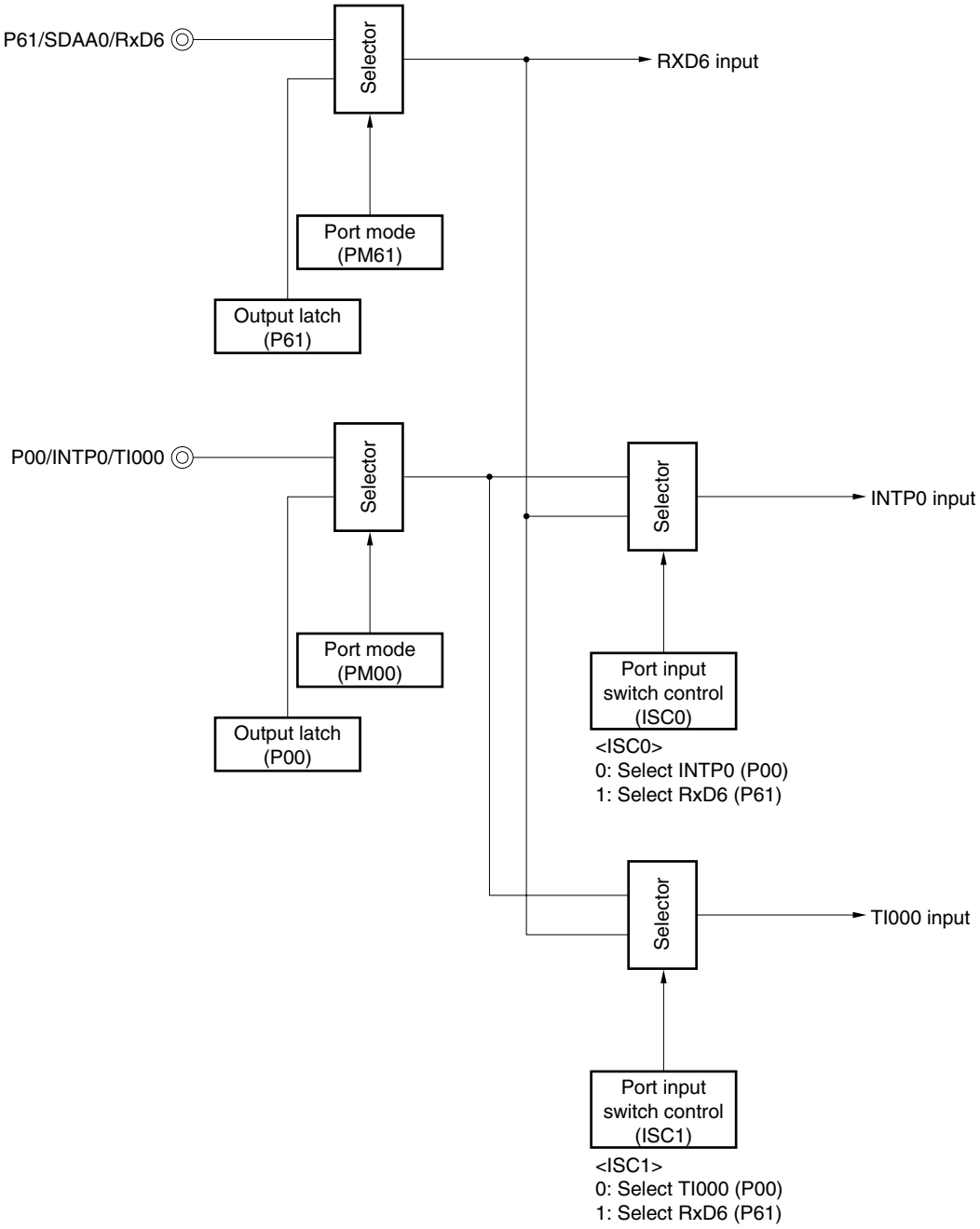


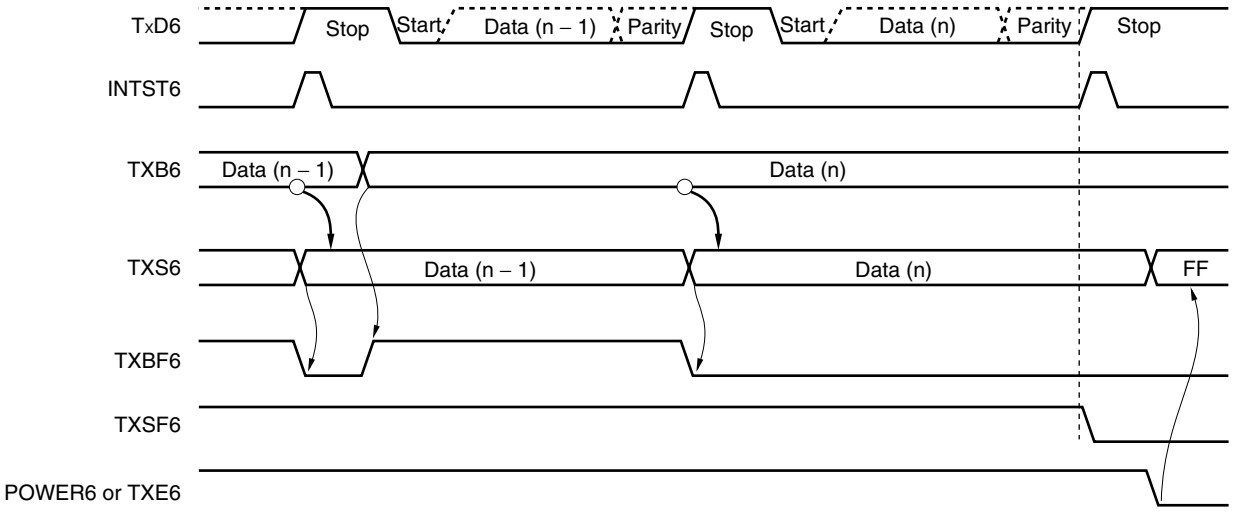
Figure 14-3. Port Configuration for LIN Reception Operation (1/2)

(1) 78K0/KY2-L and 78K0/KA2-L



Remark ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (refer to **Figure 14-11**)

Figure 14-20. Timing of Ending Continuous Transmission



Remark TxD6: TxD6 pin (output)
INTST6: Interrupt request signal
TXB6: Transmit buffer register 6
TXS6: Transmit shift register 6
ASIF6: Asynchronous serial interface transmission status register 6
TXBF6: Bit 1 of ASIF6
TXSF6: Bit 0 of ASIF6
POWER6: Bit 7 of asynchronous serial interface operation mode register (ASIM6)
TXE6: Bit 6 of asynchronous serial interface operation mode register (ASIM6)

15.5.13 Wakeup function

The I^2C bus slave function is a function that generates an interrupt request signal (INTIICA0) when a local address and extension code have been received.

This function makes processing more efficient by preventing unnecessary INTIICA0 signal from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has generated a start condition) to a slave device.

However, when a stop condition is detected, bit 4 (SPIE0) of the IICA control register 0 (IICACTL0) is set regardless of the wakeup function, and this determines whether interrupt requests are enabled or disabled.

To use the wakeup function in the STOP mode, set WUP to 1. Addresses can be received regardless of the operation clock. An interrupt request signal (INTIICA0) is also generated when a local address and extension code have been received. Operation returns to normal operation by using an instruction to clear (0) the WUP bit after this interrupt has been generated.

Figure 15-23 shows the flow for setting WUP = 1 and Figure 15-24 shows the flow for setting WUP = 0 upon an address match.

Figure 15-23. Flow When Setting WUP = 1

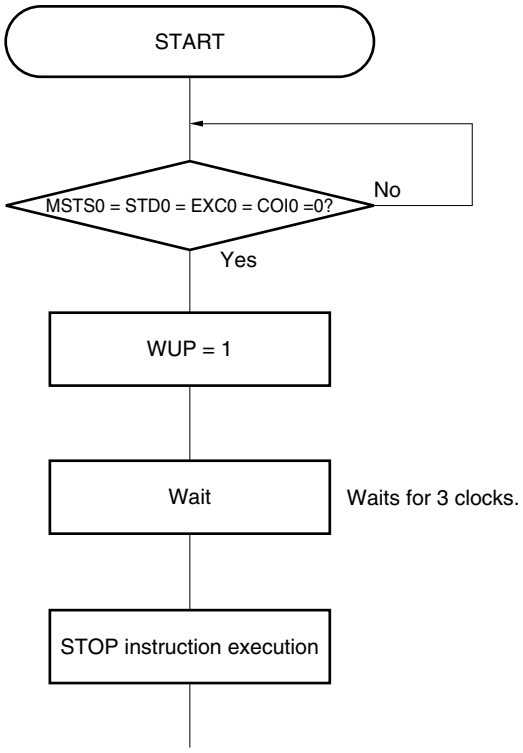
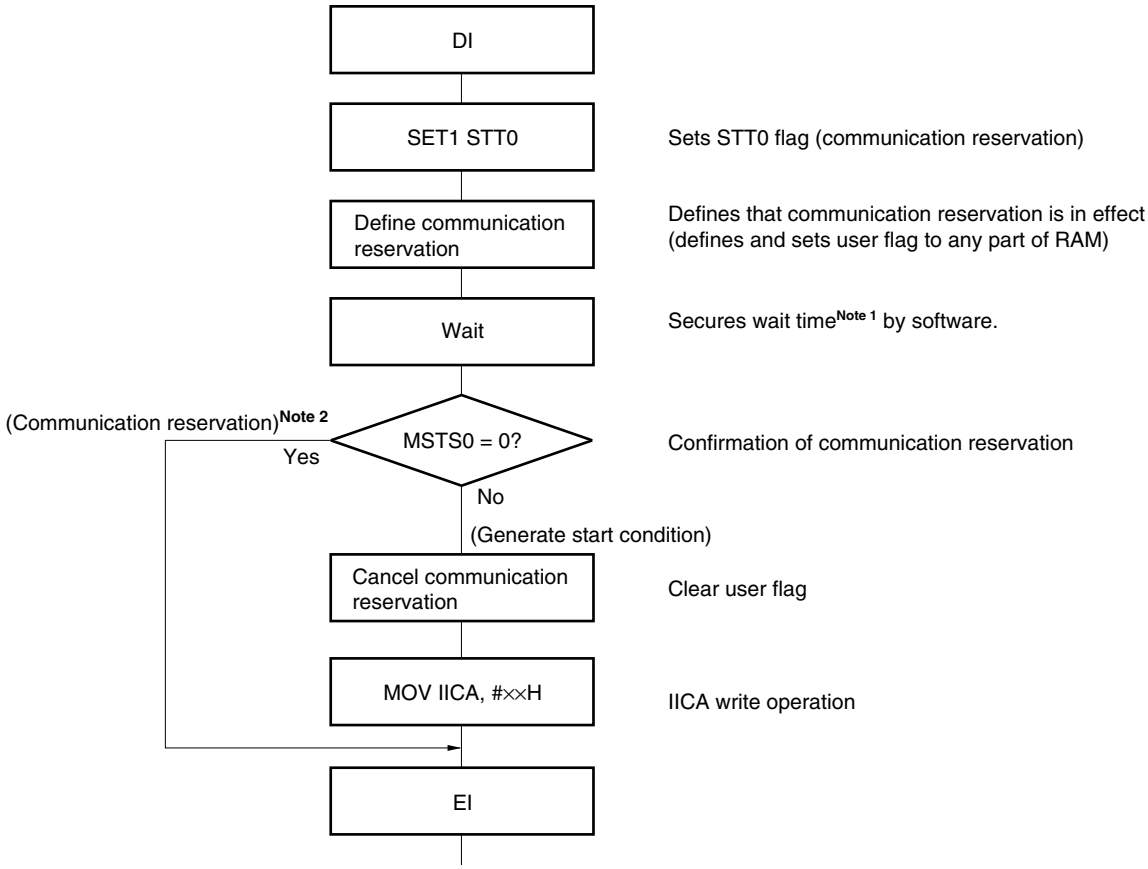


Figure 15-28. Communication Reservation Protocol



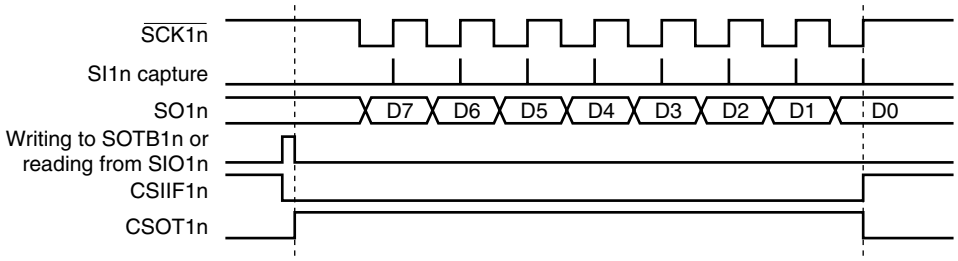
Notes 1. The wait time is calculated as follows.
(IICWL setting value + IICWH setting value + 4) + $t_F \times 2 \times f_{PRS}$ [clocks]

2. The communication reservation operation executes a write to the IICA shift register (IICA) when a stop condition interrupt request occurs.

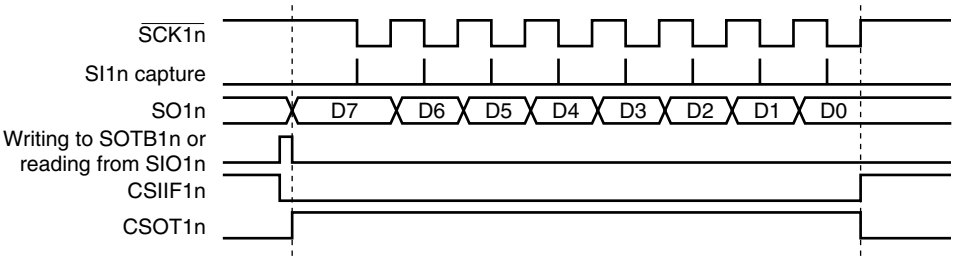
Remark STT0: Bit 1 of IICA control register 0 (IICACTL0)
MSTS0: Bit 7 of IICA status register 0 (IICAS0)
IICA: IICA shift register
IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDAA0 and SCLA0 signal falling times
(refer to **CHAPTER 28 ELECTRICAL SPECIFICATIONS**)
f_{PRS}: Peripheral hardware clock frequency

Figure 16-16. Timing of Clock/Data Phase

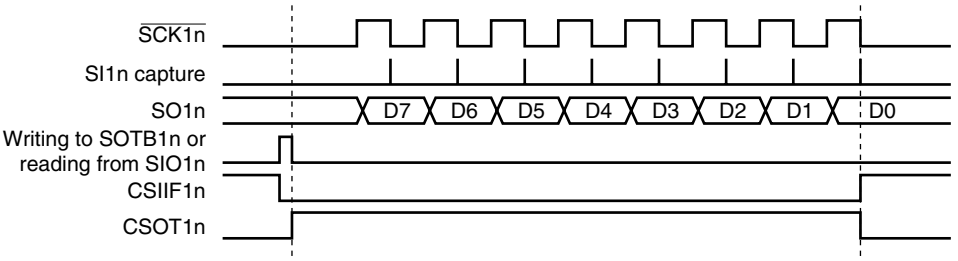
(a) Type 1: CKP1n = 0, DAP1n = 0, DIR1n = 0



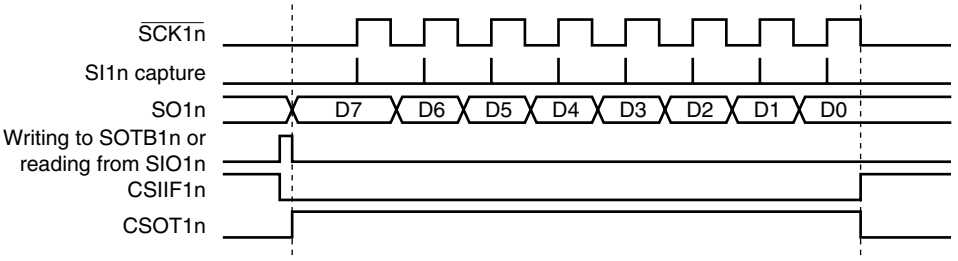
(b) Type 2: CKP1n = 0, DAP1n = 1, DIR1n = 0



(c) Type 3: CKP1n = 1, DAP1n = 0, DIR1n = 0



(d) Type 4: CKP1n = 1, DAP1n = 1, DIR1n = 0



Remarks 1. 78K0/KA2-L (25, 32-pin products): n = 1
78K0/KB2-L: n = 0
78K0/KC2-L: n = 0, 1

2. The above figure illustrates a communication operation where data is transmitted with the MSB first.

Table 17-3. Ports Corresponding to EGPn and EGNn (3/3)

(g) 78K0/KC2-L (44-pin products)

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P120	INTP0
EGP1	EGN1	P30	INTP1
EGP2	EGN2	P31	INTP2
EGP3	EGN3	P32	INTP3
EGP4	EGN4	P33	INTP4
EGP5	EGN5	P16	INTP5
EGP8	EGN8	P63	INTP8
EGP9	EGN9	P62	INTP9
EGP10	EGN10	P61	INTP10
EGP11	EGN11	P60	INTP11

(h) 78K0/KC2-L (48-pin products)

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P120	INTP0
EGP1	EGN1	P30	INTP1
EGP2	EGN2	P31	INTP2
EGP3	EGN3	P32	INTP3
EGP4	EGN4	P33	INTP4
EGP5	EGN5	P16	INTP5
EGP6	EGN6	P42	INTP6
EGP7	EGN7	P02	INTP7
EGP8	EGN8	P63	INTP8
EGP9	EGN9	P62	INTP9
EGP10	EGN10	P61	INTP10
EGP11	EGN11	P60	INTP11

Caution Select the port mode by clearing EGPn and EGNn to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0 to 5, 8 to 11: 78K0/KC2-L (44-pin products)
n = 0 to 11: 78K0/KC2-L (48-pin products)

Figure 24-1. Format of Option Byte (1/3)

Address: 0080H/1080H[Note]

7	6	5	4	3	2	1	0
0	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	LSROSC

WINDOW1	WINDOW0	Watchdog timer window open period
0	0	25%
0	1	50%
1	0	75%
1	1	100%

WDTON	Operation control of watchdog timer counter/illegal access detection
0	Counter operation disabled (counting stopped after reset), illegal access detection operation disabled
1	Counter operation enabled (counting started after reset), illegal access detection operation enabled

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time
0	0	0	$2^7/f_{IL}$ (3.88 ms)
0	0	1	$2^8/f_{IL}$ (7.76 ms)
0	1	0	$2^9/f_{IL}$ (15.52 ms)
0	1	1	$2^{10}/f_{IL}$ (31.03 ms)
1	0	0	$2^{12}/f_{IL}$ (124.12 ms)
1	0	1	$2^{14}/f_{IL}$ (496.48 ms)
1	1	0	$2^{15}/f_{IL}$ (992.97 ms)
1	1	1	$2^{17}/f_{IL}$ (3.97 s)

LSROSC	Internal low-speed oscillator operation
0	Can be stopped by software (stopped when 1 is written to bit 1 (LSRSTOP) of RCM register)
1	Cannot be stopped (not stopped even if 1 is written to LSRSTOP bit)

Note Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.

Cautions 1. The combination of WDCS2 = WDCS1 = WDCS0 = 0 and WINDOW1 = WINDOW0 = 0 is prohibited.

2. The watchdog timer continues its operation during self-programming and EEPROM emulation of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

3. If LSROSC = 0 (oscillation can be stopped by software), the count clock is not supplied to the watchdog timer in the HALT and STOP modes, regardless of the setting of bit 0 (LSRSTOP) of the internal oscillation mode register (RCM).

When 8-bit timer H1 operates with the internal low-speed oscillation clock, the count clock is supplied to 8-bit timer H1 even in the HALT/STOP mode.

4. Be sure to clear bit 7 to 0.

Remarks 1. f_{IL}: Internal low-speed oscillation clock frequency

2. ( ): f_{IL} = 33 kHz (MAX.)

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (78K0/KY2-L, 78K0/KA2-L (20 pins), 78K0/KB2-L, 78K0/KC2-L) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	AV_{REF}		−0.5 to V_{DD} + 0.3 Note 1	V
	AV_{SS}		−0.5 to +0.3	V
REGC pin input voltage Note 2	V_{IREGC}		−0.5 to +3.6 and −0.5 to V_{DD} +0.3	V
Input voltage	V_{I1}	P00 to P02, P10 to P17, P30 to P33, P40 to P42, P60 to P63, P70 to P75, P120 to P125, X1, X2, XT1, XT2, $\overline{\text{RESET}}$	−0.3 to V_{DD} + 0.3 Note 1	V
	V_{I2}	P20 to P27	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V
Output voltage	V_{O1}	P00 to P02, P10 to P17, P30 to P33, P40 to P42, P60 to P63, P70 to P75, P120	−0.3 to V_{DD} + 0.3 Note 1	V
	V_{O2}	P20 to P27	−0.3 to AV_{REF} + 0.3 Note 1	V
Analog input voltage	V_{AN1}	ANI0 to ANI7, AMP0+, AMP0-	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V
	V_{AN2}	ANI8 to ANI10, AMP1+, AMP1-	−0.3 to V_{DD} + 0.3 Note 1	V

Notes 1. Must be 6.5 V or lower.

2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.