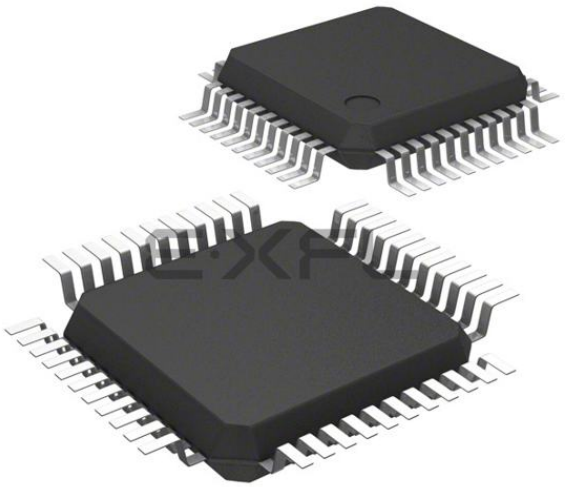

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0587gb-gaf-ax

<R> **Table 3-8. Special Function Register List: 78K0/KA2-L (25-pin and 32-pin products) (1/5)**

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF00H	P0	0	0	0	0	0	P02	P01 Note 2	P00 Note 1	R/W	√	√	–	00H	172
FF01H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF02H	P2	P27 Note 2	P26	P25	P24	P23	P22	P21	P20	R/W	√	√	–	00H	172
FF03H	P3	P37	P36	P35	P34	P33	P32	P31	0	R/W	√	√	–	00H	172
FF04H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF05H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF06H	P6	0	0	0	0	0	0	P61	P60	R/W	√	√	–	00H	172
FF07H	P7 Note 2	0	0	0	0	0	P72 Note 2	P71 Note 2	P70 Note 2	R/W	√	√	–	00H	172
FF08H	AD ADCRL	–	–	–	–	–	–	–	–	R	–	√	–	00H	411
FF09H	CR	0	0	0	0	0	0	–	–	R	–	–	√	0000H	410
FF0AH	RXB6	–	–	–	–	–	–	–	–	R	–	√	–	FFH	452
FF0BH	TXB6	–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	453
FF0CH	P12	0	0	P125	0	0	P122	P121	0	R	√	√	–	00H	172
FF0DH	ADCRH	–	–	–	–	–	–	–	–	R	–	√	–	00H	411
FF0EH	ADS	0	<ADOAS> Note 3	0	0	<ADS3> Note 3	<ADS2>	<ADS1>	<ADS0>	R/W	√	√	–	00H	412, 439
FF0FH	SIO11	–	–	–	–	–	–	–	–	R	–	√	–	00H	566
FF10H	TM00	–	–	–	–	–	–	–	–	R	–	–	√	0000H	243
FF11H		–	–	–	–	–	–	–	–						
FF12H	CR000	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	244
FF13H		–	–	–	–	–	–	–	–						
FF14H	CR010	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	244
FF15H		–	–	–	–	–	–	–	–						
FF16H to FF19H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF1AH	CMP01	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	338
FF1BH	CMP11	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	338
FF1CH to FF1EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF1FH	TM51	–	–	–	–	–	–	–	–	R	–	√	–	00H	317
FF20H	PM0	1	1	1	1	1	PM02	PM01 Note 2	PM00 Note 1	R/W	√	√	–	FFH	167, 256
FF21H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF22H	PM2	PM27 Note 2	PM26	PM25	PM24	PM23	PM22	PM21	PM20	R/W	√	√	–	FFH	167, 415, 440

Notes 1. 25-pin products only

2. 32-pin products only

3. This bit is incorporated only in products with operational amplifier.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

CHAPTER 4 PORT FUNCTIONS

4.1 Port Functions

There are two types of pin I/O buffer power supplies: AV_{REF} and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 4-1. Pin I/O Buffer Power Supplies

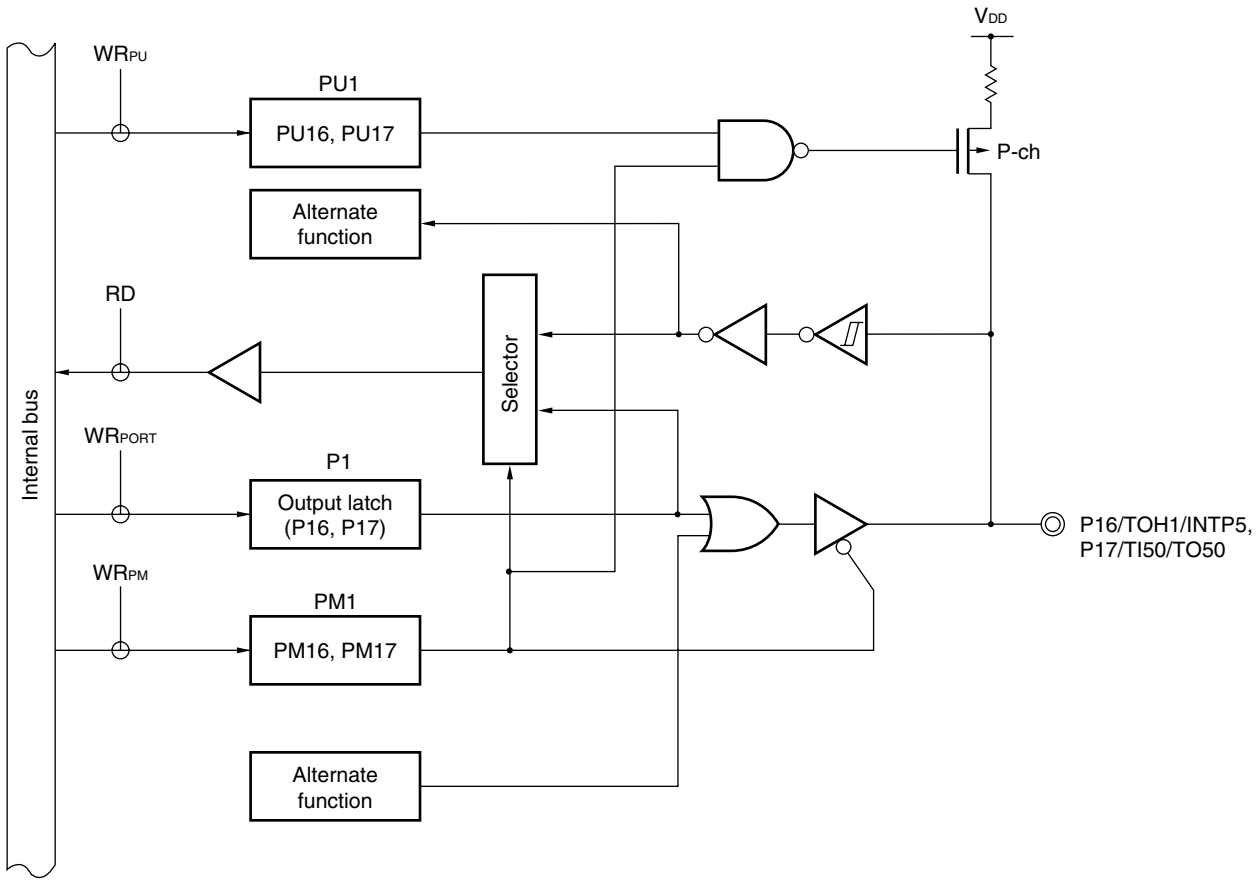
Power Supply	Corresponding Pins
AV_{REF}	P20 to P27[Note]
V_{DD}	Pins other than P20 to P27[Note]

Note 78K0/KY2-L: P20 to P23
78K0/KA2-L (20 pins): P20 to P25
<R> 78K0/KA2-L (25 pins): P20 to P26
<R> 78K0/KA2-L (32 pins): P20 to P27, P70 to P72
78K0/KB2-L: P20 to P23
<R> 78K0/KC2-L (40 pins): P20 to P26
78K0/KC2-L (44 pins, 48 pins): P20 to P27

78K0/Kx2-L microcontrollers are provided with digital I/O ports, which enable variety of control operations. The functions of each port are shown in Tables 4-2 to 4-6.

In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, refer to **CHAPTER 2 PIN FUNCTIONS**.

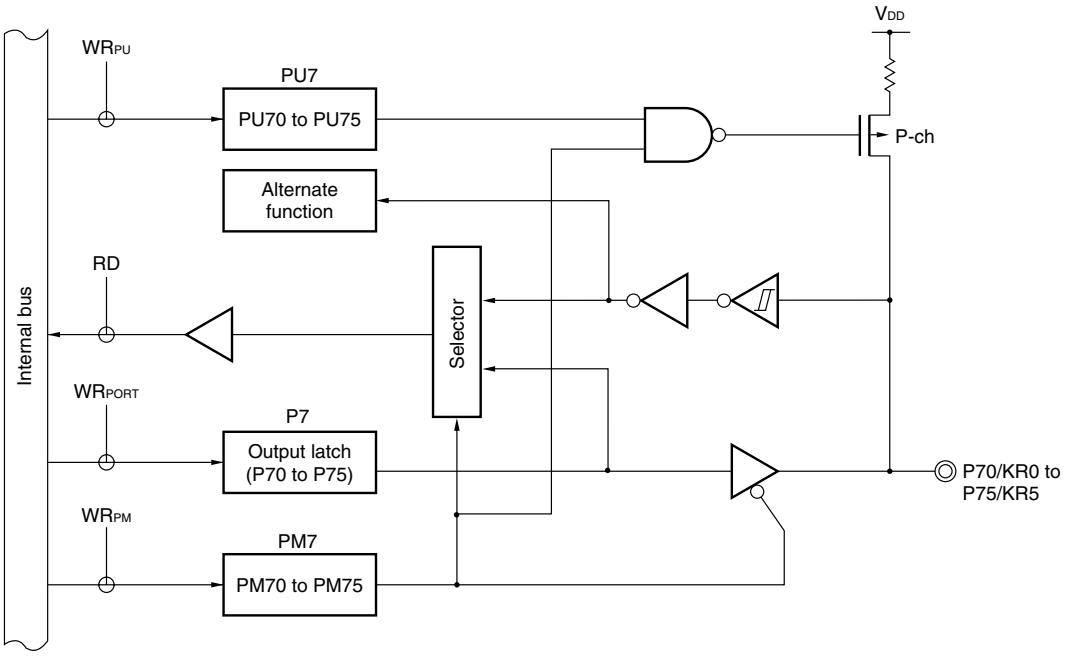
Figure 4-10. Block Diagram of P16 and P17



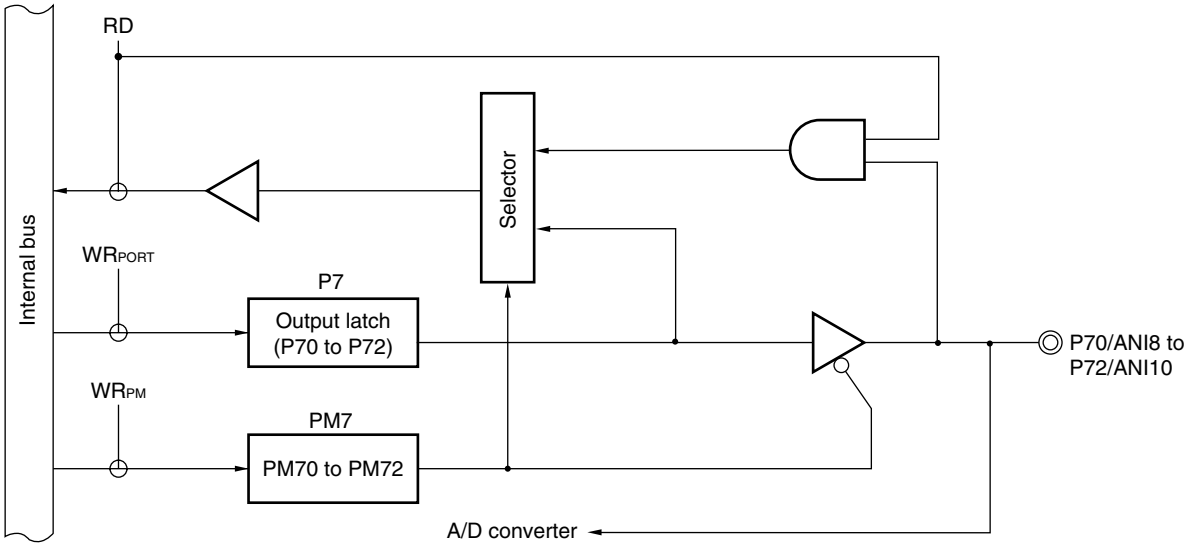
P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 4-26. Block Diagram of P70 to P75

(1) 78K0/KC2-L



<R> **(2) 78K0/KA2-L (32-pin products)**



P7: Port register 7
PU7: Pull-up resistor option register 7
PM7: Port mode register 7
RD: Read signal
WR××: Write signal

(1) Example of setting procedure when oscillating the X1 clock

<1> Setting P121/X1 and P122/X2/EXCLK pins and selecting X1 clock or external clock (OSCCTL register)
When EXCLK is cleared to 0 and OSCSEL is set to 1, the mode is switched from port mode to X1 oscillation mode.

EXCLK	OSCSEL	Operation Mode of High-Speed System Clock Pin	P121/X1 Pin	P122/X2/EXCLK Pin
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	

<2> Controlling oscillation of X1 clock (MOC register)
If MSTOP is cleared to 0, the X1 oscillator starts oscillating.

<3> Waiting for the stabilization of the oscillation of X1 clock
Check the OSTC register and wait for the necessary time.
During the wait time, other software processing can be executed with the internal high-speed oscillation clock.

Cautions 1. Do not change the value of EXCLK and OSCSEL while the X1 clock is operating.
2. Set the X1 clock after the supply voltage has reached the operable voltage of the clock to be used (refer to CHAPTER 28 ELECTRICAL SPECIFICATIONS).

(2) Example of setting procedure when using the external main system clock

<1> Setting P121/X1 and P122/X2/EXCLK pins and selecting operation mode (OSCCTL register)
When EXCLK and OSCSEL are set to 1, the mode is switched from port mode to external clock input mode.

EXCLK	OSCSEL	Operation Mode of High-Speed System Clock Pin	P121/X1 Pin	P122/X2/EXCLK Pin
1	1	External clock input mode	Input port	External clock input

<2> Controlling external main system clock input (MOC register)
When MSTOP is cleared to 0, the input of the external main system clock is enabled.

Cautions 1. Do not change the value of EXCLK and OSCSEL while the external main system clock is operating.
2. Set the external main system clock after the supply voltage has reached the operable voltage of the clock to be used (refer to CHAPTER 28 ELECTRICAL SPECIFICATIONS).

(3) Example of setting procedure when using high-speed system clock as CPU clock and peripheral hardware clock

<1> Setting high-speed system clock oscillation[Note]
(Refer to **5.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

Note The setting of <1> is not necessary when high-speed system clock is already operating.

5.6.7 Condition before changing CPU clock and processing after changing CPU clock

Condition before changing the CPU clock and processing after changing the CPU clock are shown below.

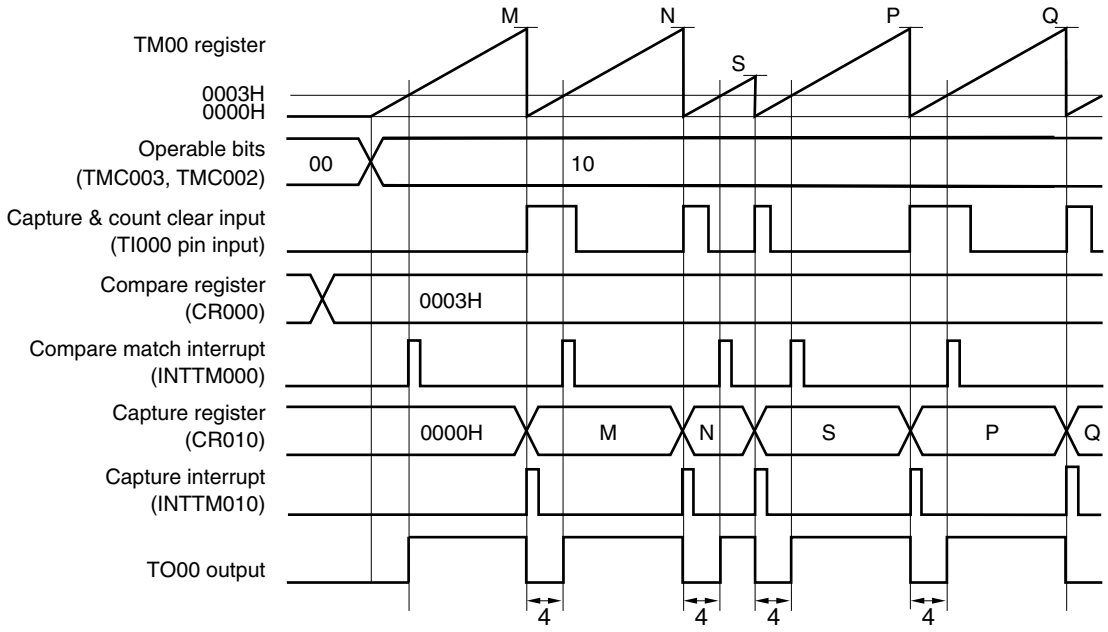
Table 5-7. Changing CPU Clock

	CPU Clock		Condition Before Change	Processing After Change
	Before Change	After Change		
KY2-L, KA2-L, KB2-L, KC2-L	Internal high-speed oscillation clock	X1 clock	Stabilization of X1 oscillation • MSTOP = 0, OSCSEL = 1, EXCLK = 0 • After elapse of oscillation stabilization time	Internal high-speed oscillator can be stopped (RSTOP = 1).
		External main system clock	Enabling input of external clock from EXCLK pin • MSTOP = 0, OSCSEL = 1, EXCLK = 1	Internal high-speed oscillator can be stopped (RSTOP = 1).
	X1 clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator • RSTOP = 0	X1 oscillation can be stopped (MSTOP = 1).
	External main system clock			External main system clock input can be disabled (MSTOP = 1).
KC2-L	Internal high-speed oscillation clock	XT1 clock	Stabilization of XT1 oscillation • XTSTART = 0, EXCLKS = 0, OSCSELS = 1, or XTSTART = 1 • After elapse of oscillation stabilization time	Operating current can be reduced by stopping internal high-speed oscillator (RSTOP = 1).
	X1 clock			X1 oscillation can be stopped (MSTOP = 1).
	External main system clock			External main system clock input can be disabled (MSTOP = 1).
	Internal high-speed oscillation clock	External subsystem clock	Enabling input of external clock from EXCLKS pin • XTSTART = 0, EXCLKS = 1, OSCSELS = 1	Operating current can be reduced by stopping internal high-speed oscillator (RSTOP = 1).
	X1 clock			X1 oscillation can be stopped (MSTOP = 1).
	External main system clock			External main system clock input can be disabled (MSTOP = 1).
	XT1 clock, external subsystem clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator and selection of internal high-speed oscillation clock as main system clock • RSTOP = 0, MCS = 0	XT1 oscillation can be stopped or external subsystem clock input can be disabled (OSCSELS = 0).
		X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • MSTOP = 0, OSCSEL = 1, EXCLK = 0 • After elapse of oscillation stabilization time • MCS = 1	XT1 oscillation can be stopped or external subsystem clock input can be disabled (OSCSELS = 0).
		External main system clock	Enabling input of external clock from EXCLK pin and selection of high-speed system clock as main system clock • MSTOP = 0, OSCSEL = 1, EXCLK = 1 • MCS = 1	XT1 oscillation can be stopped or external subsystem clock input can be disabled (OSCSELS = 0).

Remark Only 78K0/KC2-L is provided with a subsystem clock.

Figure 6-26. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (2/2)

(b) TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 0AH, CR000 = 0003H

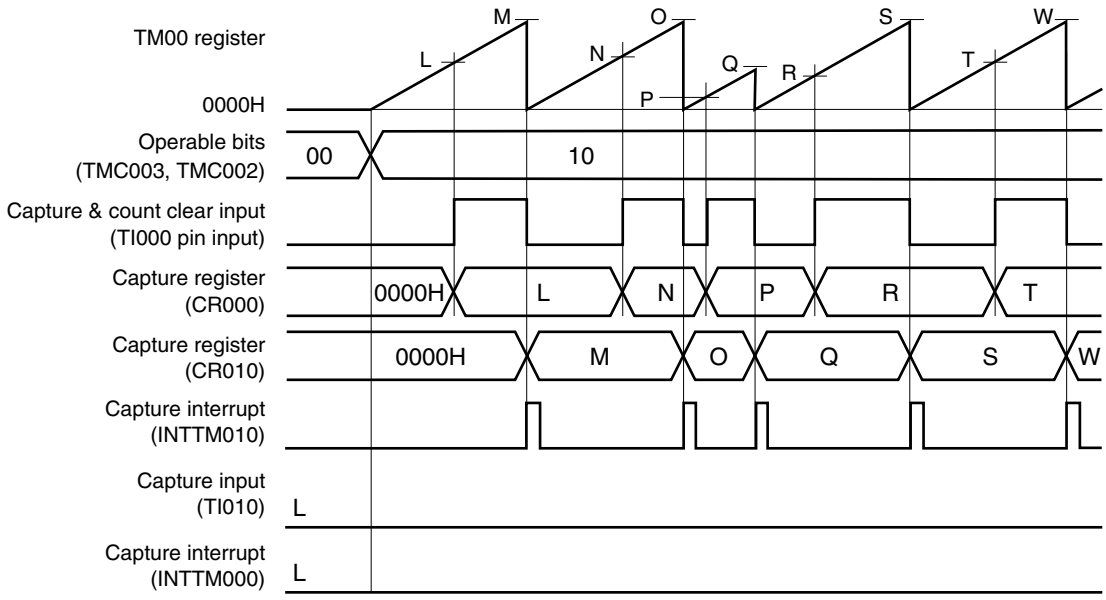


This is an application example where the width set to CR000 (4 clocks in this example) is to be output from the TO00 pin when the count value has been captured & cleared.

The count value is captured to CR010, a capture interrupt signal (INTTM010) is generated, TM00 is cleared (to 0000H), and the TO00 output level is inverted when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0003H (four clocks have been counted), a compare match interrupt signal (INTTM000) is generated and the TO00 output level is inverted.

Figure 6-30. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Capture Register) (3/3)

(c) TOC00 = 13H, PRM00 = 00H, CRC00 = 07H, TMC00 = 0AH



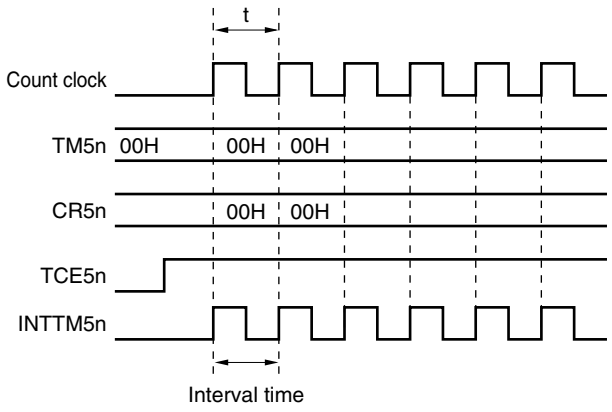
This is an application example where the pulse width of the signal input to the TI000 pin is measured.
By setting CRC00, the count value can be captured to CR000 in the phase reverse to the falling edge of the TI000 pin (i.e., rising edge) and to CR010 at the falling edge of the TI000 pin.
The high- and low-level widths of the input pulse can be calculated by the following expressions.

- High-level width = [CR010 value] – [CR000 value] × [Count clock cycle]
- Low-level width = [CR000 value] × [Count clock cycle]

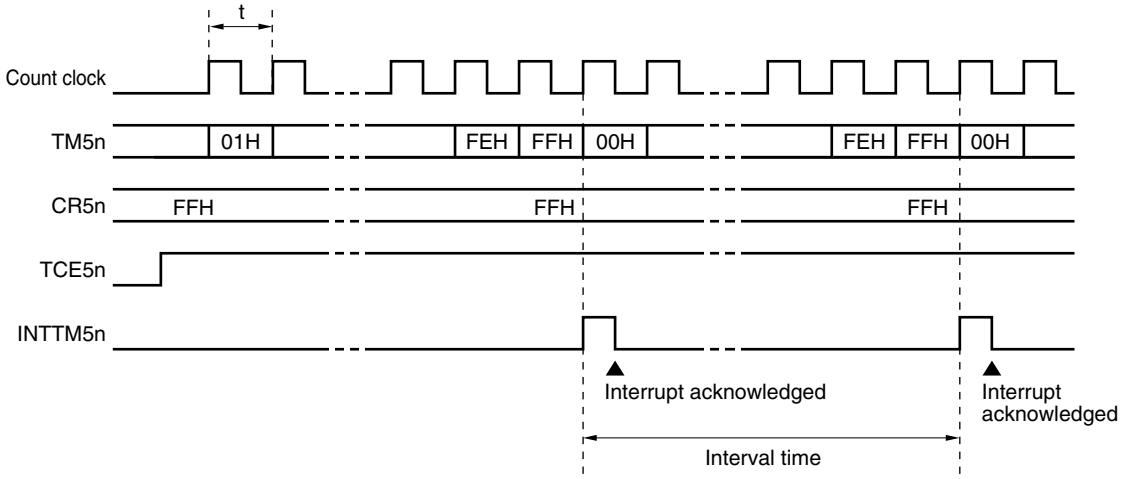
If the reverse phase of the TI000 pin is selected as a trigger to capture the count value to CR000, the INTTM000 signal is not generated. Read the values of CR000 and CR010 to measure the pulse width immediately after the INTTM010 signal is generated.
However, if the valid edge specified by bits 6 and 5 (ES110 and ES100) of prescaler mode register 00 (PRM00) is input to the TI010 pin, the count value is not captured but the INTTM000 signal is generated. To measure the pulse width of the TI000 pin, mask the INTTM000 signal when it is not used.

Figure 7-15. Interval Timer Operation Timing (2/2)

(b) When CR5n = 00H



(c) When CR5n = FFH

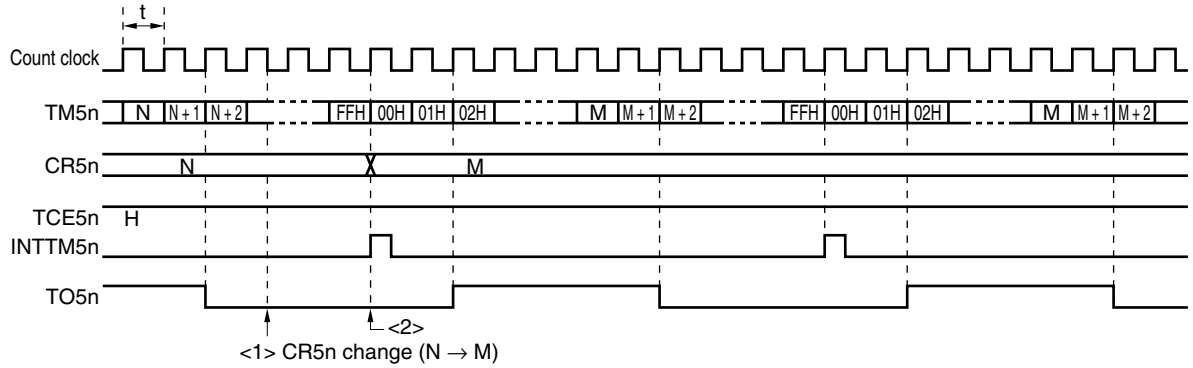


Remark 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

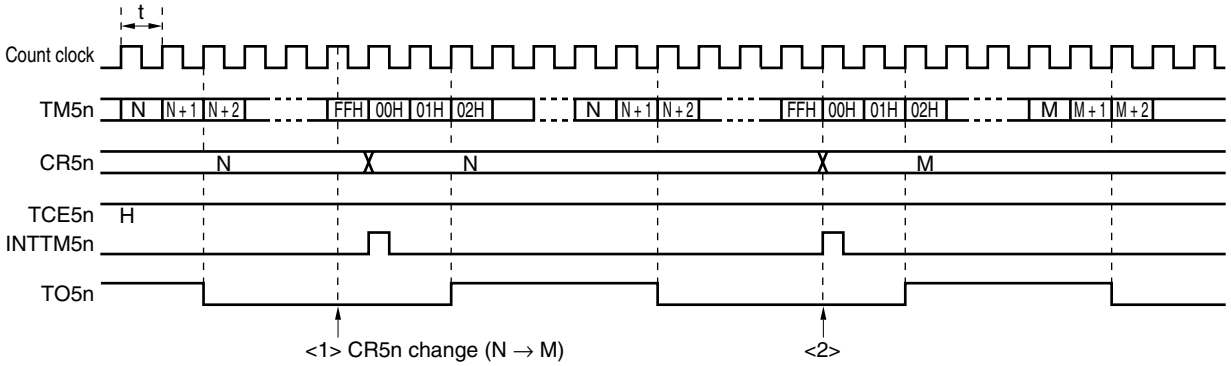
(2) Operation with CR5n changed

Figure 7-19. Timing of Operation with CR5n Changed

(a) CR5n value is changed from N to M before clock rising edge of FFH
→ Value is transferred to CR5n at overflow immediately after change.



(b) CR5n value is changed from N to M after clock rising edge of FFH
→ Value is transferred to CR5n at second overflow.

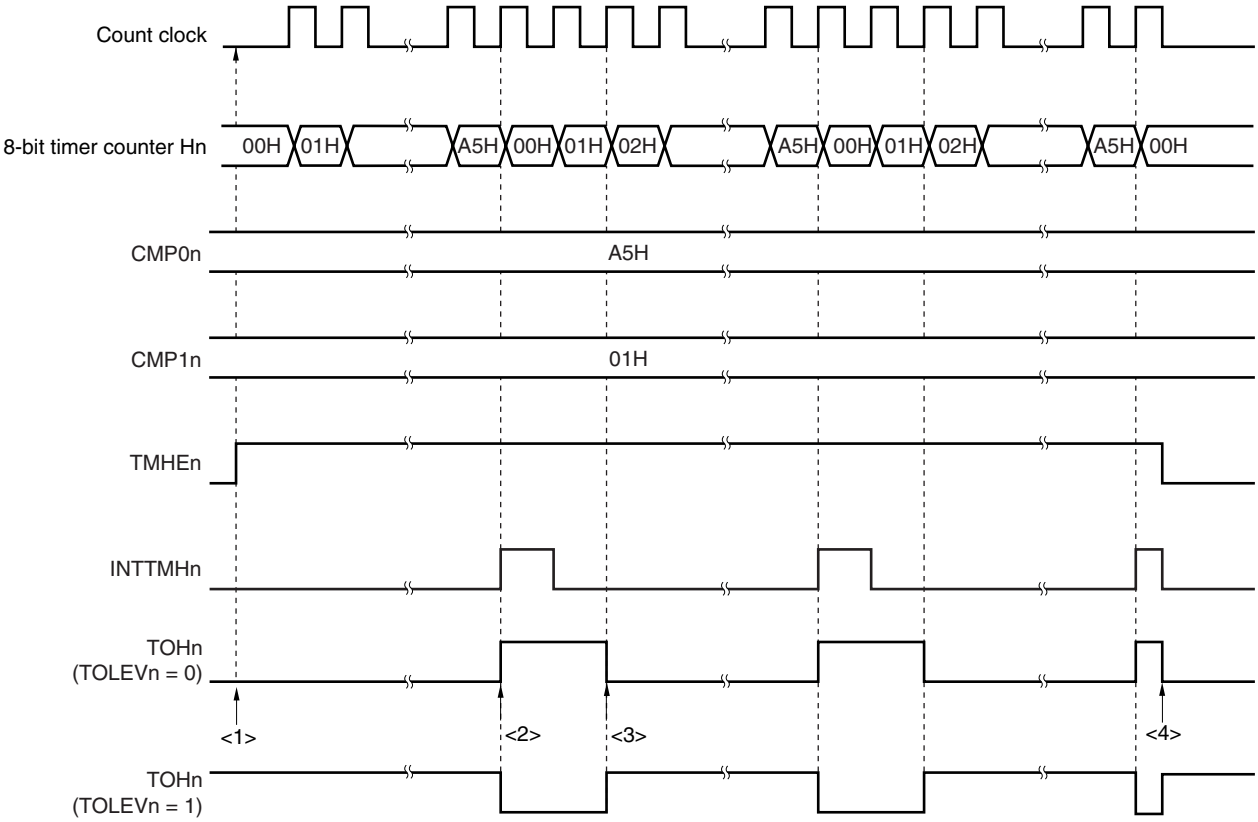


Caution When reading from CR5n between <1> and <2> in Figure 7-19, the value read differs from the actual value (read value: M, actual value of CR5n: N).

Remark 78K0/KB2-L, 78K0/KC2-L: n = 0, 1

Figure 8-15. Operation Timing in PWM Output Mode (1/4)

(a) Basic operation



<1> The count operation is enabled by setting the TMHEn bit to 1. Start the 8-bit timer counter Hn by masking one count clock to count up. At this time, PWM output outputs an inactive level.

<2> When the values of the 8-bit timer counter Hn and the CMP0n register match, an active level is output. At this time, the value of the 8-bit timer counter Hn is cleared, and the INTTMHn signal is output.

<3> When the values of the 8-bit timer counter Hn and the CMP1n register match, an inactive level is output. At this time, the 8-bit timer counter value is not cleared and the INTTMHn signal is not output.

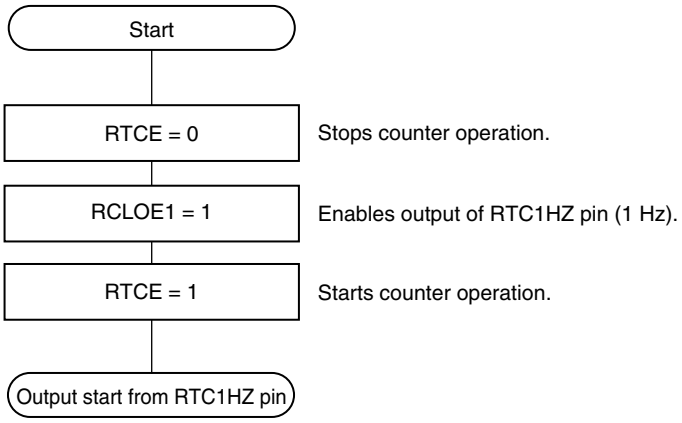
<4> Clearing the TMHEn bit to 0 during timer Hn operation sets the INTTMHn signal to the default and PWM output to an inactive level.

Remark 78K0/KY2-L, 78K0/KA2-L: n = 1
78K0/KB2-L, 78K0/KC2-L: n = 0, 1

10.4.5 1 Hz output of real-time counter

Set 1 Hz output after setting 0 to RTCE first.

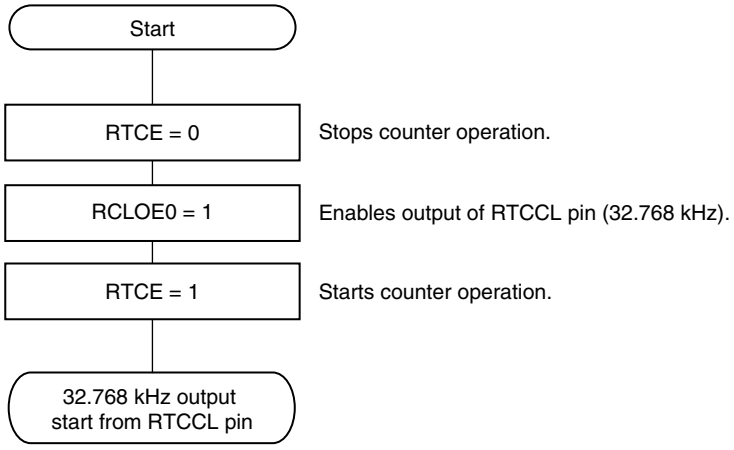
Figure 10-24. 1 Hz Output Setting Procedure



10.4.6 32.768 kHz output of real-time counter

Set 32.768 kHz output after setting 0 to RTCE first.

Figure 10-25. 32.768 kHz Output Setting Procedure



Cautions 1. Be sure to clear bits 4, 5, and 7 to "0".

2. Set a channel to be used for A/D conversion in the input mode by using port mode registers 1, 2, 7 (PM1, PM2, PM7).

3. Set ADS after PGA operation setting when selecting the PGA output signal as analog input. Set ADS after single AMP operation setting when selecting the operational amplifier output signal as analog input (refer to CHAPTER 13 OPERATIONAL AMPLIFIERS).

4. If data is written to ADS, a wait cycle is generated. Do not write data to ADS when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 31 CAUTIONS FOR WAIT.

(6) A/D port configuration registers 0, 1[Note] (ADPC0, ADPC1[Note])

ADPC0 switches the P20/AMP0-/ANI0 to P27/ANI7 pins to digital I/O or analog I/O of port. Each bit of ADPC0 corresponds to a pin of port 2 and can be specified in 1-bit units.

ADPC1 switches the P10/AMP1-/ANI8 to P12/AMP1+/ANI10 or P70/ANI8 to P72/ANI10 pins to digital I/O or analog I/O of port. Each bit of ADPC1 corresponds to a pin of P10 to P12 in port 1 or P70 to P72 in port7 and can be specified in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

<R> Reset signal generation clears ADPC0 to 00H, sets ADPC1 of 78K0/KA2-L (32-pin products) to 00H, and sets ADPC1 of 78K0/KB2-L and 78K0/KC2-L to 07H.

Note 78K0/KA2-L (32-pin products), 78K0/KB2-L, and 78K0/KC2-L only

<R> **Figure 12-9. Format of A/D Port Configuration Registers 0, 1 (ADPC0, ADPC1) (1/3)**

(a) 78K0/KY2-L

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	ADPCS3	ADPCS2	ADPCS1	ADPCS0

(b) 78K0/KA2-L (20-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

(c) 78K0/KA2-L (25-pin products)

Address: FF2EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	ADPCS6	ADPCS5	ADPCS4	ADPCS3	ADPCS2	ADPCS1	ADPCS0

Figure 13-8. Format of Port Mode Register 2 (PM2)

(a) 78K0/KY2-L

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

Caution Be sure to set bits 4 to 7 of PM2 to 1.

<R>**(b) 78K0/KA2-L**

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27 Note 1	PM26 Note 2	PM25	PM24	PM23	PM22	PM21	PM20

Notes 1. 32-pin products only

2. 25-pin and 32-pin products only

(c) 78K0/KB2-L

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

<R>**(d) 78K0/KC2-L**

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27 Note	PM26	PM25	PM24	PM23	PM22	PM21	PM20

Note 44-pin and 48-pin products only

PM2n	P2n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(1) Transmit buffer register 1n (SOTB1n)

This register sets the transmit data.

Transmission/reception is started by writing data to SOTB1n when bit 7 (CSIE1n) and bit 6 (TRMD1n) of serial operation mode register 1n (CSIM1n) is 1.

The data written to SOTB1n is converted from parallel data into serial data by serial I/O shift register 1n, and output to the serial output pin (SO1n).

SOTB1n can be written or read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Cautions 1. Do not access SOTB1n when CSOT1n = 1 (during serial communication).

2. In the slave mode, transmission/reception is started when data is written to SOTB11 with a low level input to the $\overline{\text{SSI11}}$ pin. For details on the transmission/reception operation, refer to 16.4.2 (2) Communication operation.

Remarks 1. 78K0/KA2-L (25, 32-pin products): n = 1
78K0/KB2-L: n = 0
78K0/KC2-L: n = 0, 1

2. The $\overline{\text{SSI11}}$ pin is available only in 78K0/KA2-L (25, 32-pin products) and 78K0/KC2-L (48-pin products).

Table 20-2. Hardware Statuses After Reset Acknowledgment (4/4)

Hardware		Status After Reset Acknowledgment[Note 1]
Reset function	Reset control flag register (RESF)	00H[Note 2]
Low-voltage detector	Low-voltage detection register (LVIM)	00H[Note 2]
	Low-voltage detection level selection register (LVIS)	00H[Note 2]
Interrupt	Request flag registers 0L, 0H, 1L, 1H (IF0L, IF0H, IF1L, IF1H)	00H
	Mask flag registers 0L, 0H, 1L, 1H (MK0L, MK0H, MK1L, MK1H)	FFH
	Priority specification flag registers 0L, 0H, 1L, 1H (PR0L, PR0H, PR1L, PR1H)	FFH
	External interrupt rising edge enable registers 0, 1 (EGPCTL0, EGPCTL1)	00H
	External interrupt falling edge enable registers 0, 1 (EGNCTL0, EGNCTL1)	00H
Regulator	Regulator mode control register (RMC)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. These values vary depending on the reset source.

<R>

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI (Except Reset by LVI Default Start Function)	Reset by LVI Default Start Function
RESF	WDTRF flag	Cleared (0)	Cleared (0)	Set (1)	Held	Cleared (0)
	LVIRF flag			Held	Set (1)	
LVIM		Cleared (00H)	Cleared (00H)	Cleared (00H)	Held	Cleared (00H)
LVIS						

Remark The special function registers (SFRs) mounted depend on the product. Refer to **3.2.3 Special function registers (SFRs)**.

25.8.1 Register controlling self programming mode

The self programming mode is controlled by the self programming mode control register (FPCTL).

FPCTL can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears FPCTL to 00H.

Figure 25-8. Format of Self Programming Mode Control Register (FPCTL)

Address: FF2BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
FPCTL	0	0	0	0	0	0	0	FLMDPUP Note

FLMDPUP Note	Self programming mode control
0	Normal operation mode
1	Self programming mode

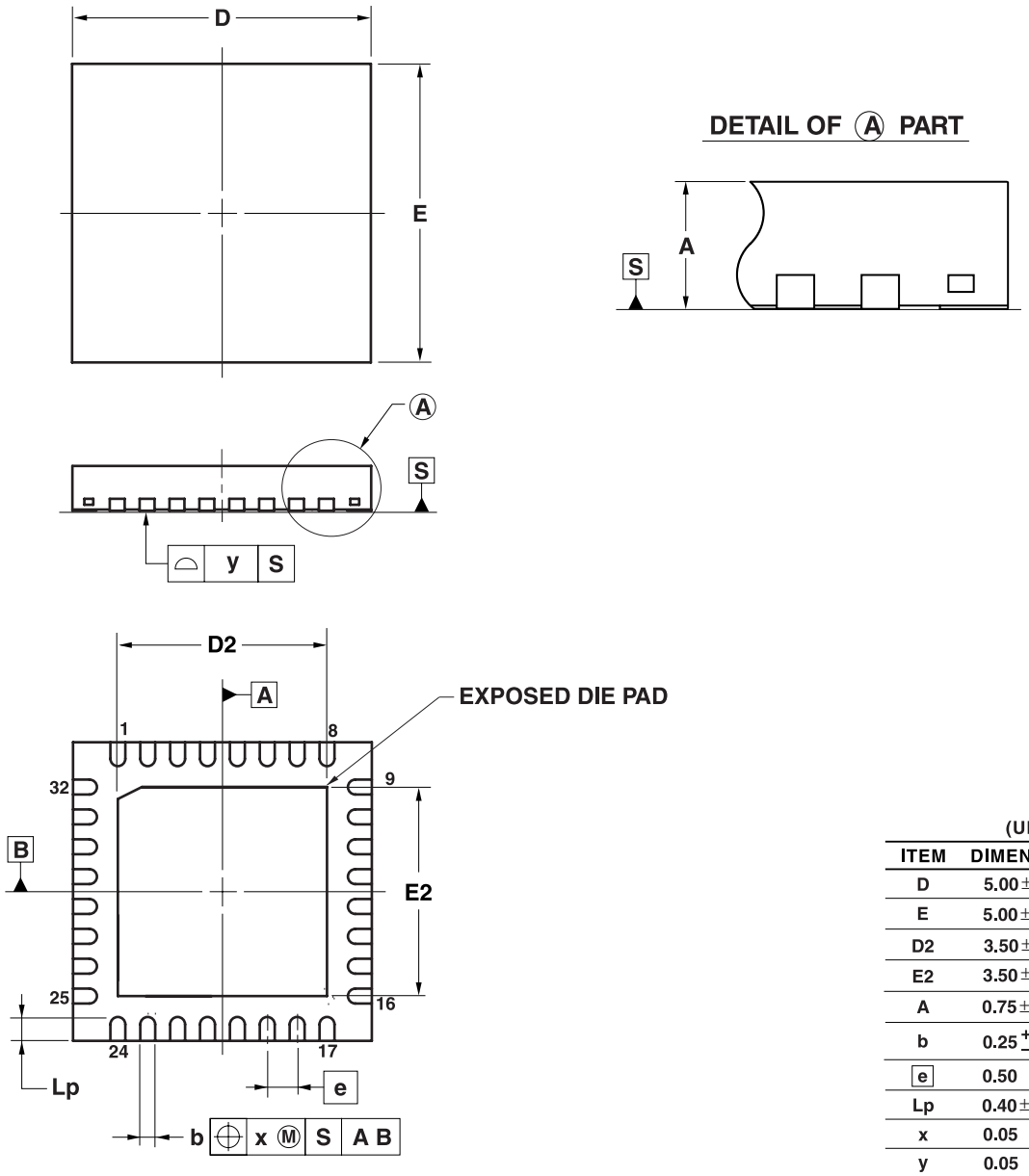
Note The FLMDPUP bit must be set to 0 (normal operation mode) while the regular user program is being executed, and set to 1 (self programming mode) while self programming is being executed. The flash memory rewrite circuit does not operate in normal operation mode, so even though the firmware and software for rewriting will work, no actual rewriting will take place.

25.8.2 Flow of self programming (Rewriting Flash Memory)

The following figure illustrates a flow of rewriting the flash memory by using a self programming library.

<R> • μPD78F0560K8-3B4-AX, 78F0561K8-3B4-AX, 78F0562K8-3B4-AX, 78F0565K8-3B4-AX, 78F0566K8-3B4-AX, 78F0567K8-3B4-AX

32-PIN PLASTIC WQFN(5x5)



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.05
E	5.00±0.05
D2	3.50±0.05
E2	3.50±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

P32K8-50-3B4-1

APPENDIX B REGISTER INDEX

B.1 Register Index (In Alphabetical Order with Respect to Register Names)

(3/4)

Page	Description	Classification
CHAPTER 12 A/D CONVERTER		
p.421	Change of **Table 12-8. Setting Functions of P70/ANI8 to P72/ANI10 Pins**	(d)
p.433	Change of mode name in **Table 12-9. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)**	(c)
CHAPTER 13 OPERATIONAL AMPLIFIERS		
p.435	Change of **Figure 13-1. Block Diagram of Operational Amplifier**	(c)
p.439	Change of **Figure 13-6. Format of Analog Input Channel Specification Register (ADS)**	(c)
p.444	Change of **Table 13-5. Setting Functions of P21/ANI1/AMP0OUT/PGAIN Pin**	(c)
CHAPTER 16 SERIAL INTERFACES CSI10 AND CSI11		
p.573	Change of **(4) Port mode registers 0, 1, 3, 4, 6, 12 (PM0, PM1, PM3, PM4, PM6, PM12)** in **16.3 Registers Controlling Serial Interfaces CSI10 and CSI11**	(d)
p.574	Addition of **Figure 16-9. Format of Port Mode Register 0 (PM0)**	(d)
p.574	Addition of **Figure 16-11. Format of Port Mode Register 3 (PM3)**	(d)
CHAPTER 17 INTERRUPT FUNCTIONS		
pp.592, 593	Change of **Table 17-1. Interrupt Source List**	(d)
CHAPTER 19 STANDBY FUNCTION		
p.649	Addition of **Caution** in **Table 19-3. Operating Statuses in STOP Mode**	(c)
CHAPTER 20 RESET FUNCTION		
pp.662, 663	Change of **Note** in **Table 20-2. Hardware Statuses After Reset Acknowledgment**	(b)
p.664	Change of **Table 20-3. RESF Status When Reset Request Is Generated**	(b)
CHAPTER 21 POWER-ON-CLEAR CIRCUIT		
p.668	Change of **Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2/2)**	(b)
CHAPTER 22 LOW-VOLTAGE DETECTOR		
p.673	Change of **Note 1** in **Figure 22-2. Format of Low-Voltage Detection Register (LVIM)**	(b)
p.675	Change of **Note** in **Figure 22-3. Format of Low-Voltage Detection Level Select Register (LVIS)**	(b)
p.676	Change of **Remark 1** in **22.4 (1) Used as reset (LVIMD = 1)**	(b)
p.680	Change of description in **22.4.1 (1) (b) When LVI default start function enabled is set (LVISTART = 1)**	(b)
p.680	Change of **Figure 22-6. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 0, Option Byte: LVISTART = 1)**	(b)
p.685	Change of description in **22.4.2 (1) (b) When LVI default start function enabled is set (LVISTART = 1)**	(b)
p.685	Change of **Figure 22-9. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 0, Option Byte: LVISTART = 1)**	(b)
CHAPTER 23 REGULATOR		
p.691	Change of **(1) Regulator mode control register (RMC)** in **23.2 Register Controlling Regulator**	(b)
CHAPTER 24 OPTION BYTE		
p.694	Change of **(4) 0083H/1083H** in **24.1 Functions of Option Bytes**	(b)
p.696	Change of description of LVISTART bit in **Figure 24-1. Format of Option Byte (2/3)**	(b)
p.697	Change of **Figure 24-1. Format of Option Byte (3/3)**	(b)
p.698	Change of description example of software in **24.2 Format of Option Byte**	(b)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents